Power Macintosh: Description of Integrated Circuits (3/94)

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TOPIC ---

This article provides an overview of the various controller chips present on the Power Macintosh logic boards.

DISCUSSION ---

Main Processor

The main processor in the Power Macintosh 6100/60, 7100/66, and 8100/80 computers is a PowerPC 601 microprocessor. The principal features of the PowerPC 601 microprocessor include:

- full RISC processing architecture
- parallel integer and floating-point processing units
- a branch manager that can usually implement branches by reloading the incoming instruction queue without using any processing time
- an internal memory management unit (MMU)
- 32 Kbit of on-chip cache memory

ROM

Power Macintosh computers contain 4MB of ROM with 100ns access time. Some of the system software that was on disk in previous Macintosh computers is in ROM in Power Macintosh models.

RAM

RAM for Power Macintosh computers is provided by dynamic random-access memory (DRAM) chips, of which the first 8MB of RAM capacity is soldered to the main logic board. Users may expand RAM capacity by adding 72-pin Single Inline Memory Modules (SIMMs) in pairs. Each SIMM contains two banks of DRAM with up to 16MB of capacity per bank.

High-Speed Memory Controller

The high-speed memory controller (HMC) is an ASIC (application specific integrated circuit) that controls all memory operations in Power Macintosh computers. The HMC has the following features that support data transfers to and from the PowerPC 601 microprocessor:

- support for all basic transfer protocols, including all single cycle accesses
- support for four-cycle 32-byte cache accesses
- translation of misaligned read actions into double-word read actions
- implementation of address-only transactions
- bus arbitration (of the address bus only)

The HMC does not support the following features:

- pipelining of memory bus transactions
- cache snooping
- recovery from transfer error acknowledge signals
- little-endian transfer mode

Apple Memory-Mapped I/O Controller

The Apple Memory-Mapped I/O Controller (AMIC) is a 160-pin gate array chip that performs most I/O logic and control for Power Macintosh computers. It supports the following functions:

- handling interrupts received through Versatile Interface Adapter (VIA) channels
- DMA for Ethernet I/O
- DMA for the SWIM III floppy disk drive controller
- DMA for the Serial Communications Controller (SCC) I/O
- DMA for Small Computer Systems Interface (SCSI) support
- DMA for sound I/O
- monitor support

The AMIC does not support the extended transfer protocols for the PowerPC 601 processor; using these protocols will cause a transfer error exception.

Data Path Chips

Two data path (DP) chips provide buffering between I/O and DRAM accesses and the cached CPU bus. They perform the following functions:

- route byte lanes between 8-bit and 16-bit I/O processes and the 64-bit CPU bus
- provide first-in, first-out (FIFO) buffering for video monitor data, which is fetched from RAM as eight-cycle bursts
- supply the Ariel II video chip with appropriate timing signals for video monitor data

The Ariel II video chip is described in the next section.

Ariel II Video Chip

The Ariel II video chip provides a color lookup table (CLUT) and digital-to-analog converter (DAC) for driving an AudioVision monitor.

SWIM III Floppy Disk Drive Controller

The SWIM III floppy disk drive controller is an extension of the SWIM II circuitry used in models such as the Macintosh Quadra 800 and Macintosh Quadra 650. It includes the following new features:

- support for DMA data transfers, which minimize use of the main processor
- no requirement that interrupts be disabled during floppy disk accesses
- support for GCR and MFM formats on 1.44MB disks
- compatibility with the manual-inject floppy disk drive

Floppy disk drives designed to be compatible with the New Age controller used in the Macintosh Quadra 840AV and Macintosh Quadra 660AV computers can easily be adapted for compatibility with the SWIM III controller.

Curio I/O Chip

The Curio is a multipurpose I/O chip that contains a Media Access Controller for Ethernet (MACE), a SCSI controller, and a Serial Communications Controller (SCC).

The SCC section of the Curio includes 8-byte FIFO buffers for both transmit and receive data streams.

Cuda Microcontroller Chip

The Cuda is a microcontroller chip. Its function is to:

- turn system power on and off
- manage system resets from various commands
- maintain parameter RAM
- manage the Apple Desktop Bus (ADB)
- manage the real-time clock
- let an external signal from either Apple GeoPort serial port control system power

AWAC Sound Chip

The audio waveform amplifier and converter (AWAC) is a 44-pin chip that combines a waveform amplifier with a 16-bit digital sound encoder and decoder (codec). It conforms to the IT&T ASCO 2300 Audio-Stereo Codec Specification and furnishes high quality sound I/O for Power Macintosh computers.

BART NuBus Controller

The BART NuBus controller chip provides the data gateway between NuBus and the CPU bus. It acts as a CPU bus master, transferring one-cycle or four-cycle transactions. It supports all NuBus burst transactions and is compliant with the IEEE Standard 1196.

Squidlet Chip

Squidlet is a 28-pin chip that provides a set of synchronized system clocks for Power Macintosh computers.

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