# Power Macintosh: High-Speed Memory Controller (3/94)

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TOPIC -----------------------------------------------------

This article describes the high-speed memory controller on all Power Macintosh computers.

DISCUSSION -----------------------------------------------

The high-speed memory controller (HMC) is an ASIC chip that controls all memory operations in Power Macintosh computers. The HMC has the following features that support data transfers to and from the PowerPC 601 microprocessor:

- Support for all basic transfer protocols, including all single-cycle accesses
- Support for four-cycle 32-byte cache accesses
- Translation of misaligned read actions into double-word read actions
- Implementation of address-only transactions
- Bus arbitration (of the address bus only)

The HMC does not support the following features:

- Pipelining of memory bus transactions
- Cache snooping
- Recovery from transfer error acknowledge signals
- Little-endian transfer mode

Support Information Services


Keywords: kppc

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This information is from the Apple Technical Information Library.

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