Power Macintosh 9500: Optimizing PCI card performance (7/96)

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TOPIC ---

This article discusses a configuration tip to provide optimal performance in Power Macintosh 9500 computers using more than three PCI cards.

DISCUSSION ---

In the Power Macintosh 9500, there are six PCI slots (A1, B1, C1, D2, E2, F2), which are serviced by two PCI controller chips (Bandit 1 and Bandit 2). Theoretically, each controller chip can handle up to four PCI cards. However, in order to even the data bandwidth load, three PCI slots are distributed to each controller. Specifically, Bandit 1 controls slots A1-C1, and Bandit 2 controls slots D2-F2. This distribution can almost be thought of as two PCI buses with three slots each.

The slots on the logic board are labeled by letter and number. The labelling, which is printed next to the slot, is used only to identify the physical location of the slot on the logic board. Located between the Power Supply and the bottom of the case, the slots look like:

Power Supply

---------- PCI Slot A1
---------- PCI Slot B1
---------- PCI Slot C1
---------- PCI Slot D2
---------- PCI Slot E2
---------- PCI Slot F2
Bottom of Case

Additionally, the I/O circuitry on the logic board, which controls functions such as ADB and Serial I/O, was designed to be accessed through the PCI bus. The I/O circuitry functions as a PCI card built into the logic board. When considering performance of the PCI bus, it can be assumed that I/O functions will consume some of the bandwidth of the PCI bus. Depending on the amount of I/O activity, the PCI bus handling I/O may run slower than the PCI bus that does not.

On the Power Macintosh 9500, the I/O functions are handled by the first PCI

controller (Bandit 1). Because the first PCI controller handles both I/O functionality and slots A1-C1, performance of cards in these slots may be decreased.

In order to achieve optimal performance of PCI cards, slots D2-F2 should be used first. However, when using high-bandwidth cards, which are moving large amounts of data across the PCI bus, it may be beneficial to evenly distribute the cards between the two buses. In such circumstances, it is likely that the I/O bandwidth is much smaller than that of the high-bandwidth card. To distribute data evenly across the entire PCI bus, you may want to use the following order: D2, A1, E2, B1, and so on.

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