Macintosh SE Internal System Expansion Slot: Pinout Information

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Row	Column 1	Column 2	Column 3
32	-12V	-5V	+12V
31	Spare	+12V	+12V
30	Ground	+12V	Ground
29	D15	Ground	C16M
28	D14	Ext.STK/	C8M
27	D13	Reserved	E
26	D12	Reserved	A23
25	D11	Reserved	A22
24	D10	Reserved	A21
23	D9	Reserved	A20
22	D8	Spare	A19
21	D7	BERR/	A18
20	D6	IPL2/	A17
19	D5	IPL1/	A16
18	D4	IPL0/	A15
17	D3	+5V	A14
16	D2	+5V	A13
15	D1	+5V	A12
14	D0	+5V	A11
13	+5V	+5V	A10
12	RESET/	HALT/	A9
11	PMCYC/	Reserved	A8
10	AS/	Reserved	A7
9	UDS/	Ground	A6
8	LDS/	Ground	A5
7	R/W/	Ground	A4
6	DTACK/	Ground	A3
5	BG/	Ground	A2
4	BGACK/	Ground	A1
3	BR/	Ground	FC0
2	VMA/	Ground	FC1
1	VPA/	Ground	FC2

Here is a description of the signals in the system expansion slot.

Signal	Description
FC0-FC2	68000 Function Code lines
A1-A23	68000 Address lines
E	68000 E Clock
C8M	Microprocessor clock = 7.8336 MHz = C16M divided by 2.
C16M	Gate Array Clock = 15.6672 MHz
HALT/	68000 Halt. Wired directly to RESET/
IPL0/-IPL2/	68000 Interrupt Priority Level lines
BERR/	68000 Bus Error. Generated by gate array due to SCSI access timeout.
Ext.DTK/	Pull low to put the gate array generated DTACK/ into a high-impedance state. The expansion board is then responsible for generating the DTACK/signal (as an output to the microprocessor, throught the DTACK/signal line).
VPA/	68000 Valid Peripheral Address. Supplied to 68000. For Macintosh SE, VPA space is $E0 0000 to $FF FFFF.
VMA/	68000 Valid Memory Address
BR/	68000 Bus Request
BGACK/	68000 Bus Grant Acknowledge
BG/	68000 Bus Grant
DTACK/	68000 Data Transfer Acknowledge. Inserts wait states until data bus is available. Normally supplied by the gate array. Gate array generation of DTACK/ can be suppressed (put into a high-impedance state) by pulling the EXT.DTACK/line low; this allows DTACK/ to be externally generated by an add-on device. DTACK/ is not supplied for accesses to VPA space, is held off to separate 2 successive accesses to the SCC and is held off during RAM access by video.
R/W/	68000 Read/Write
LDS/	68000 Lower Data Strobe
UDS/	68000 Upper Data Strobe
AS/	68000 Address Strobe

PMCYC/ Processor-Memory Cycle. Used to synchronize with the gate array for RAM accesses. PMCYC/ is low when RAM is available for microporcessor accesses and is high during video acesses. PMCYC/ is always high during SO.

RESET/ 68000 Reset. Wired directly to HALT/.

D0-D15 68000 Data Bus

Additional information may be found in the the Motorola 68000 manual.

Keywords: <None>

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