



Tech Info Library

Macintosh IIvx: Pinouts

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TOPIC -----

This article describes the external and internal pinouts for the Macintosh IIvx computer system.

DISCUSSION -----

EXTERNAL PORT PINOUTS

The pinouts listed are for the back of the Macintosh IIvx.

DB-19 External Drive Connector

```

10                               1
X X X X X X X X X X
X X X X X X X X X
19                               11
```

Pin	Signal	Description
---	-----	-----
1, 2, 3, 4	GND	Ground
5	-12 V	-12 Volt Supply
6	+5 V	+5 Volt Supply
7	+12 V	+12 Volt Supply
8	12 V	+12 Volt Supply
9	nc	(Not Connected)
10	+5 V	+5 Volt Supply
11	PHASE0	Motor Phase 0 Output
12	PHASE1	Motor Phase 1 Output
13	PHASE2	Motor Phase 2 Output
14	PHASE3	Motor Phase 3 Output
15	W/REQ	Write Request
16	SEL	Register Select Line
17	ENABLE2	Drive Enable
18	RD	Read Data Input
19	WR	Write Data Output

DB-25 External SCSI Connector

```

13                               1
X X X X X X X X X X X X X
X X X X X X X X X X X X
25                               14

```

Pin	Signal	Description
---	-----	-----
1	REQ~	Request
2	MSG~	Message
3	I/O~	Input/Output
4	RST~	SCSI Bus Reset
5	ACK~	Acknowledge
6	BSY~	Busy
7	GND	Ground
8	DB0~	Data bit 0
9	GND	Ground
10	DB3~	Data bit 3
11	DB5~	Data bit 5
12	DB6~	Data bit 6
13	DB7~	Data bit 7
14	GND	Ground
15	C/D~	Command/Data
16	GND	Ground
17	ATN~	Attention
18	GND	Ground
19	SEL~	Select
20	DBP~	Data parity
21	DB1~	Data bit 1
22	DB2~	Data bit 2
23	DB4~	Data bit 4
24	GND	Ground
25	TPWR	Terminator power

DB-15 Monitor Video Connector

```

8                               1
X X X X X X X X X
X X X X X X X X
15                               9

```

Pin	Signal	Description
---	-----	-----
1	RED.GND	Red Video Ground
2	RED.VID	Red Video
3	CSYNC~	Composite Sync.
4	MON.ID1	Monitor ID, Bit 1

5	GRN.VID	Green Video
6	GRN.GND	Green Video Ground
7	MON.ID2	Monitor ID, Bit 2
8	nc	(Not Connected)
9	BLU.VID	Blue Video
10	MON.ID3	Monitor ID, Bit 3
11	C&VSYNC.GND	CSYNC & VSYNC Ground
12	VSYNC~	Vertical Sync.
13	BLU.GND	Blue Ground
14	HSYNC.GND	HSYNC Ground
15	HSYNC~	Horizontal Sync.
Shell	CHASSIS.GND	Chassis Ground

Mini DIN-8 RS-232/RS-422 Serial Connector

```

      |8  |7  |6
-5    -4    -3
      -2  -1

```

Pin	Signal	Description
---	-----	-----
1	HSKo	Handshake Output DTR
2	HSKi	Handshake Input CTS
3	TxD-	Transmit Data (inverted)
4	SG	Signal Ground
5	RxD-	Receive Data (inverted)
6	TxD+	Transmit Data
7	GPi	General Purpose Input DCD
8	RxD+	Receive Data

Miniature Sound Input Jack

Contact	Signal	Description
-----	-----	-----
Sleeve	GND	Signal ground
Ring Mic	PWR	Microphone power, +8 V +/- 5% @ 1 mA
Tip	SND.IN	Sound input signal, 1.6 K W +/- 10 % impedance, 4 mV max signal w/o clipping

Miniature Stereo Sound Output Jack

Contact	Signal	Description
-----	-----	-----
Sleeve	GND	Signal ground
Ring	RIGHT	Right Channel, 1.5 V peak-to-peak audio signal
Tip	LEFT	Left Channel, 1.5 V peak-to-peak audio signal

Mini DIN-4 Apple Desktop Bus Connector

|4 |3
-2 -1

Pin	Signal	Description
---	-----	-----
1	DATA	ADB Data
2	P0	Power On
3	+5 V	+5 Volt
4	GND	Ground

INTERNAL PORT PINOUTS

The pinouts listed are for the internal connectors on the Macintosh IIvx logic board.

ROM SIMM

Pin	Signal	Pin	Signal
---	-----	---	-----
1	VCC	33	A10
2	+12 V VPP	34	A11
3	FLASHWE (IOW)	35	A12
4	A2	36	A13
5	A3	37	A14
6	A4	38	A15
7	A5	39	A16
8	A6	40	A17
9	A7	41	A18
10	GND	42	A19
11	ROM DISABLE (+5 V)	43	A20
12	ROMOE	44	A21
13	VCC	45	A22
14	D0	46	VCC
15	D1	47	D16
16	D2	48	D17
17	D3	49	D18

18	D4	50	D19
19	D5	51	D20
20	D6	52	D21
21	D7	53	D22
22	D8	54	D23
23	D9	55	D24
24	D10	56	D25
25	D11	57	D26
26	D12	58	D27
27	D13	59	D28
28	D14	60	D29
29	D15	61	D30
30	GND	62	D31
31	A8	63	VCC
32	A9	64	GND

Accelerator Slot

Pin	Signal	Pin	Signal	Pin	Signal
---	-----	---	-----	---	-----
A1	A(30)	B1	RESET*	C1	R/W*
A2	HALT*	B2	A(29)	C2	pullup [1]
A3	A(31)	B3	A(25)	C3	A(28)
A4	A(26)	B4	A(27)	C4	+5 V
A5	RMC*	B5	A(24)	C5	pullup[2]
A6	D(31)	B6	GND	C6	+5 V
A7	D(30)	B7	D(29)	C7	N/C
A8	D(28)	B8	D(27)	C8	GND
A9	D(26)	B9	D(25)	C9	+5 V
A10	D(24)	B10	D(23)	C10	GND
A11	D(22)	B11	D(21)	C11	GND
A12	D(20)	B12	D(19)	C12	IPL2*
A13	D(18)	B13	D(17)	C13	pulldown[3]
A14	D(16)	B14	+5 V	C14	+5 V
A15	A(22)	B15	A(21)	C15	+5 V
A16	A(20)	B16	A(19)	C16	GND
A17	A(18)	B17	A(17)	C17	N/C
A18	A(16)	B18	A(15)	C18	GND
A19	A(14)	B19	A(13)	C19	+5 V
A20	A(12)	B20	A(11)	C20	pulldown[4]
A21	A(10)	B21	GND	C21	GND
A22	FC(1)	B22	A(9)	C22	+5 V
A23	A(8)	B23	FPU* [5]	C23	GND
A24	FC(2)	B24	FC(0)	C24	CIOUT*
A25	D(15)	B25	D(14)	C25	IPL1*
A26	D(13)	B26	D(12)	C26	IPL0*
A27	D(11)	B27	D(10)	C27	CBREQ*
A28	D(9)	B28	D(8)	C28	D(7)
A29	D(6)	B29	BGACK*	C29	D(5)
A30	D(4)	B30	D(3)	C30	D(2)
A31	D(1)	B31	D(0)	C31	+5 V

A32	ROM*	B32	A(7)	C32	A(6)
A33	A(5)	B33	A(4)	C33	A(3)
A34	A(2)	B34	A(1)	C34	A(0)
A35	BG*	B35	+5 V	C35	CBACK*
A36	A(23)	B36	CPUDIS	C36	BR*
A37	DSACK0*	B37	AS*	C37	DS*
A38	15.6672MHz [6]	B38	DSACK1*	C38	BERR*
A39	GND	B39	+5 V	C39	SIZ1
A40	GND	B40	N/C [7]	C40	SIZ0

NOTES

Notes and differences between Macintosh IIVx and IIVI and Macintosh IICI:

pullup[1]: This pin was connected to STERM* on the Macintosh IICI cache connector. STERM is not generated by any logic on the motherboard. This signal is pulled up with a 1K resistor.

pullup[2]: This pin was connected to CFLUSH* on the Macintosh IICI cache connector. The cache flush function is different on Macintosh IIVx, so this pin cannot be supported. It is pulled up with a 1K resistor.

pulldown[3]: This pin was connected to CACHEENABLE* on the Macintosh IICI cache connector. The cache enable function is different on Macintosh IIVx, so this pin cannot be supported. It is pulled down with a 100 ohm resistor. NOTE: THIS IS THE CACHE ENABLED STATE.

pulldown[4]: This pin was a no connect on the Macintosh IICI cache connector. It is pulled down with a 100 ohm resistor to allow certain third party accelerator cards to operate correctly.

FPU* [5]: This signal was a no connect on the Macintosh IICI cache connector. It is now connected to the FPU decode logic on the PCB. This logic is active at all times. The logic board FPU, if present is disabled if the CPUDISable signal is asserted.

15.6672 MHz [6]: This signal was the 25 MHz CPU clock on the Macintosh IICI cache connector. It is now the 15.6672 MHz clock generated from the VASP for all systems. It is not the 31.3344 MHz CPU clock for the Macintosh IIVx. This clock was chosen because it must be used to synchronize access to the VASP chip, which always operates at 15.6672 MHz.

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