Macintosh II NuBus Slots: Pinouts and signal descriptions

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TOPIC ---

This article contains the pinouts for Macintosh II NuBus slots.

DISCUSSION --

All NuBus slots in the Macintosh II have the same pinouts:

Pin	Row A	Row B	Row C
1	-12V	-12V	RESET
2	GND	GND	GND
3	SPV	GND	+5V
4	SP	+5V	+5V
5	TM1	+5V	TM0
6	AD1	+5V	AD0
7	AD3	+5V	AD2
8	AD5	GND	AD4
9	AD7	GND	AD6
10	AD9	GND	AD8
11	AD11	GND	AD10
12	AD13	GND	AD12
13	AD15	GND	AD14
14	AD17	GND	AD16
15	AD19	GND	AD18
16	AD21	GND	AD20
17	AD23	GND	AD22
18	AD25	GND	AD24
19	AD27	GND	AD26
20	AD29	GND	AD28
21	AD31	GND	AD30
22	GND	GND	GND
23	GND	GND	PFD
24	ARB1	-5.2V	ARB0
25	ARB3	-5.2V	ARB2
26	ID1	-5.2V	ID0
27	ID3	-5.2V	ID2

28	ACK	+5V	START
29	+5V	+5V	+5V
30	RQST	GND	+5V
31	NMRQ	GND	GND
32	+12V	+12V	CLK

Signal descriptions for these lines are:

- +5V
  Power to slot; 2 amps per slot maximum continuous.

- +12V
  Power to slot; 0.25 amps per slot maximum continuous.

- -12V
  Power to slot; 0.1 amps per slot maximum continuous.

- -5.2V
  Unused

- GND
  Power return for +5V, +12V, and -12V

- RESET
  Open collector signal; card should use to reset circuitry.

- SPV
  Slot Parity Valid; asserted if card provides parity. Never asserted under Apple NuBus.

- SP
  Slot Parity; odd parity of AD0-AD3 if SPV asserted.

- TM0 - TM1
  Transaction modifiers.

- AD<31:0>
  Address/Data bits 31 to 0.

- PFW
  Power Fail Warning given 2ms before AC power is lost.

- ARB<3:0>
  Arbitration bits 3 to 0; arbitrates system mastership.

- ID<3:0>
  Geographical address 3 to 0; hard-coded to slot.

- START
  Asserted to indicate an address on AD lines.

- ACK
  Acknowledge of START cycle.

- RQST
  Request; asserted to request bus mastership.

- NMRQ
  Non-master request; used to signal an interrupt.

- CLK Clock. Asymmetrical 10MHz clock; synchronous
  transactions on NuBus.

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