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Apple II and IIe: Interface I/O Signal Timing (2/97)

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TOPIC	
This article describes how the ${\rm I/O}$ strobe signals on the Apple II periphereconnector are handled.	al
DISCUSSION	
The I/O strobe signals on the Apple II peripheral connector are decoded from appropriate address lines and combined with the phase one clock. This is the treduce the TTL circuitry required to build a simple I/O port.	
CLOCK 1	
I/O SELECT I/O STROBE DEVICE SELECT	

A simple 8 bit output port would be a positive edge triggered latch with the clock tied to I/O select.

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I/O STROBE ----- 11 D0 ----- 3 2 | ---D1 ----- 4 5 | ---D2 ----- 7 6 | ---D3 ----- 8 9 | ---8 bits of D4 -----|13 12 | ---Latched TTL D5 -----|14 15 | ---Output D6 -----|17 16 | ---D7 -----|18 19 | ---

Assumming that this interface is plugged into slot 1, any write operation to \$C090..\$C09F will transfer the data to the output lines. This is a very simple

interface, so any read to \$C090..\$C09F will transfer random data to the output latch and to the Apple.

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