1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
G		396923	PRODUCTION RELEASED	08/26/05	?

SCHEM,MLB,PB17"

08/25/2005

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG		✓
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG		✓
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS	✓	
INT_TMDS		✓
MMM	✓	
INT_CLK	✓	
EXT_CLK		✓

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6694	1	SCHEM,MLB,PB17	SCH1	
820-1688	1	PCBF,MLB,PB17	PCB1	
826-4393	1	LABEL,PCB,28MM X 6MM	EEE:U3Y	LABEL_R15

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER | DESIGN CK | ENG APPD | MFG APPD | QA APPD | DESIGNER | RELEASE | SCALE NONE

MATERIAL/FINISH NOTED AS APPLICABLE

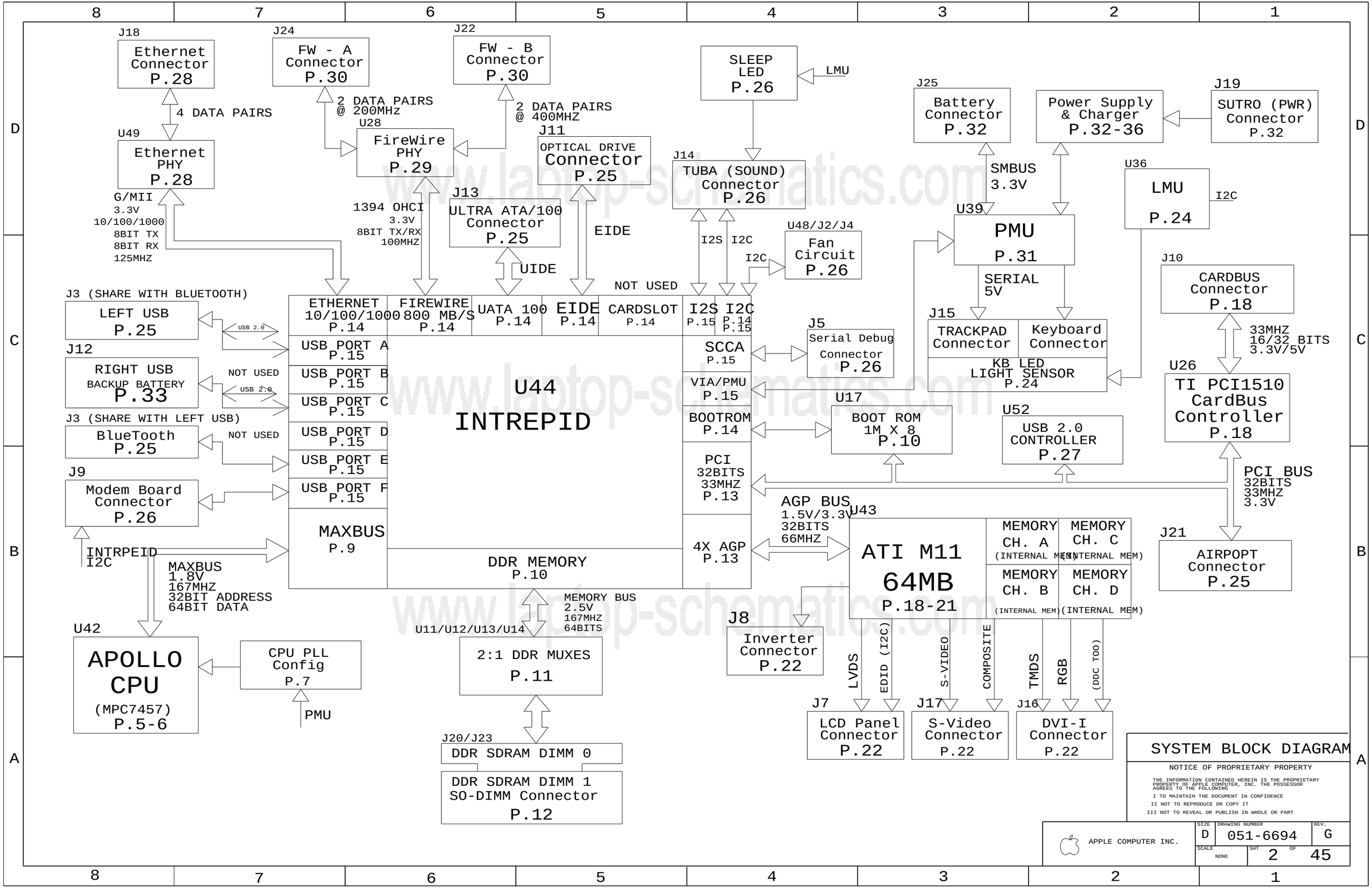
SIZE D

Apple Computer Inc.

TITLE: SCHEM,MLB,PB17"

DRAWING NUMBER 051-6694 REV. G

SHT 1 OF 45



SYSTEM BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 2 OF 45	

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 31

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF

U21 PG 31

>~13.44V TURNS-ON

<~13.44V SHUTS-OFF

RUN/SS

BUCK VCC REGULATOR (LTC1625) PG 32

AC: 12.8V
NO AC: BATTERY VOLTAGE
1625 NOT RUNNING

SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS (12.8V)

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

14V_PBUS

+3V_PMU LDO PG 32

+5V_MAIN

+3V_PMU

+4_6V_BU

+BATT

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V

MAIN 3V/5V DC/DC (LTC3707) PG 33

VCC

STBYMD

PGOOD 3V_5V_OK

HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND

TURNS CONTROL TO RUN/SS WHEN IT'S OPEN

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+3.3V_MAIN

+PBUS

BACKUP BATTERY

12.8V CHARGES BACKUP BATTERY

24V IS OUTPUT ONLY FROM BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT PG 32

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+24V_PBUS

DC/DC (LTC3411) PG 35

+1.8V_MAIN

MAXBUS BROADCOM

SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

BATTERY CHARGER (MAX1772) PG 31

+BATT

3S 3P PRISMATIC CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 31

+PBUS

BACKLIGHT INVERTER

+5V_MAIN

VCC MAIN 2.5V/1.5V DC/DC (MAX1715) PG 35

MAP31 DDR I/O
MAP31 DDR CORE
DDR POWER

+2.5V_MAIN

PGOOD 1_5V_2_5V_OK

+1.5V_MAIN

INTREPID CORE
AGP I/O

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

TURNS ON OUTPUT @ 2.4V ON1/ON2

+5V_MAIN

DCDC_EN_L

AFTER PMU IS UP AND RUNNING DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

+PBUS

DCDC_EN
SLEEP

MAXBUS SEQUENCING

+5V_MAIN

VCC SHDN

DC/DC (MAX1717) PG 34

SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

CPU_VCORE (+1.4V/+1.5V)

+5V_MAIN

+PBUS (12.8V)

EXT_VCC

VCC DC/DC (LTC1778) PG 20

GPU_VCORE +1.2V/+1.0V

SHUTDOWN: STOPPED
SLEEP: D3HOT/D3COLD
RUN: RUNNING

TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE

RUN/SS

DCDC_EN
SLEEP

D3_COLD

GPU_VCORE SEQUENCING

1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER

1_5V_2_5V_OK

D3_HOT

DCDC_EN_L
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON

HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

SHUT-DOWN RUN SLEEP RUN SHUT-DOWN

SLEEP
SLEEP_L_LS5
DCDC_EN
DCDC_EN_L
+5V_MAIN
+5V_SLEEP
+3V_MAIN
+3V_SLEEP
3V_5V_OK
+2_5V_MAIN
+2_5V_SLEEP
+1_5V_MAIN
+1_5V_SLEEP
1_5V_2_5V_OK (MAX1715 OUTPUT)
1_5V_2_5V_OK (AT LTC1778 RUN/SS)
GPU_VCORE (D3HOT)
GPU_VCORE (D3COLD)
+1_8V_MAIN

~11MS
~13.5MS
2.4V - ??? MS
2.6 MS
2.6 MS
~???MS
1.9 MS

POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 3 OF 45	

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

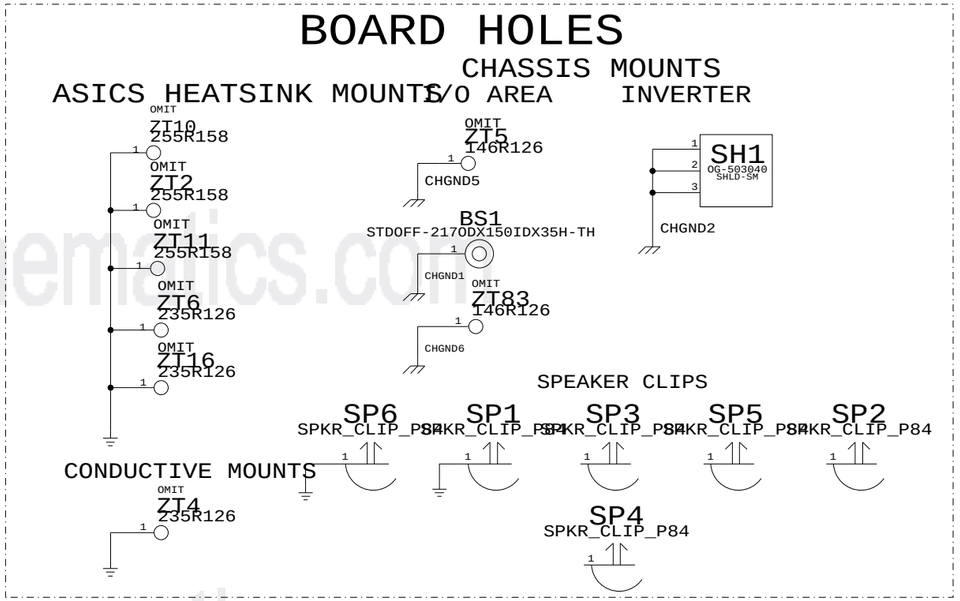
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES



GROUND VIAS

ZT77 ZT35 ZT48 ZT57 ZT22
ZT81 ZT50 ZT56 ZT1 ZT25
ZT24 ZT44 ZT72 ZT80 ZT3
ZT38 ZT66 ZT55 ZT73 ZT32
ZT36 ZT67 ZT29 ZT75 ZT31
ZT27 ZT52 ZT74 ZT63 ZT26
ZT40 ZT53 ZT82 ZT61 ZT23
ZT39 ZT70 ZT79 ZT54 ZT19
ZT37 ZT71 ZT68 ZT51 ZT17
ZT28 ZT78 ZT60 ZT42 ZT15
ZT30 ZT69 ZT58 ZT64 ZT13
ZT34 ZT65 ZT41 ZT76 ZT12
ZT33 ZT47 ZT9 ZT62 ZT14
ZT43 ZT45 ZT7 ZT59 ZT18
ZT46 ZT49 ZT8 ZT21 ZT20

HOLE-VIA-20R10

BOARD INFORMATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 4 OF 45	

CPU_VCORE_SLEEP

R241 470 5% 1/16W MF 402

C25 10UF 20% 6.3V CERM 805
C342 10UF 20% 6.3V CERM 805
C344 10UF 20% 6.3V CERM 805
C346 10UF 20% 6.3V CERM 805
C8 10UF 20% 6.3V CERM 805
C153 0.1UF 20% 10V CERM 402
C12 2.2UF 20% 10V CERM 805
C340 2.2UF 20% 10V CERM 805
C193 0.1UF 20% 10V CERM 402

MORE 0805 10UF CAPS ON VCORE
POWER SUPPLY PAGE (PG 33)

PLCAE SHORT CLOSE TO CENTER OF CPU

XW31 SM OMIT

26 ADT7467 VCORE MON

C195 10UF 20% 6.3V CERM 805
C347 10UF 20% 6.3V CERM 805
C258 10UF 20% 6.3V CERM 805
C345 10UF 20% 6.3V CERM 805
C156 10UF 20% 6.3V CERM 805
C341 10UF 20% 6.3V CERM 805
C225 10UF 20% 6.3V CERM 805
C343 10UF 20% 6.3V CERM 805

PLACE BELOW CPU
IN FORMER L3 AREA

CPU_VCORE DECOUPLING NETWORK

C223 0.1UF 20% 10V CERM 402
C91 0.1UF 20% 10V CERM 402
C114 0.1UF 20% 10V CERM 402
C104 0.1UF 20% 10V CERM 402
C103 0.1UF 20% 10V CERM 402
C110 0.1UF 20% 10V CERM 402
C190 0.1UF 20% 10V CERM 402
C189 0.1UF 20% 10V CERM 402
C138 0.1UF 20% 10V CERM 402
C191 0.1UF 20% 10V CERM 402
C112 0.1UF 20% 10V CERM 402
C168 0.1UF 20% 10V CERM 402
C149 0.1UF 20% 10V CERM 402
C111 0.1UF 20% 10V CERM 402
C150 0.1UF 20% 10V CERM 402
C105 0.1UF 20% 10V CERM 402
C154 0.1UF 20% 10V CERM 402
C115 0.1UF 20% 10V CERM 402
C113 0.1UF 20% 10V CERM 402
C152 0.1UF 20% 10V CERM 402
C151 0.1UF 20% 10V CERM 402
C202 0.1UF 20% 10V CERM 402
C201 0.1UF 20% 10V CERM 402
C192 0.1UF 20% 10V CERM 402

R206 470 5% 1/16W MF 402

MAXBUS_SLEEP 5 6 7 8 15 16 35 39

CPU_OVDD DECOUPLING NETWORK

C72 0.1UF 20% 10V CERM 402
C48 0.1UF 20% 10V CERM 402
C38 0.1UF 20% 10V CERM 402
C74 0.1UF 20% 10V CERM 402
C275 0.1UF 20% 10V CERM 402
C46 0.1UF 20% 10V CERM 402
C47 0.1UF 20% 10V CERM 402
C170 0.1UF 20% 10V CERM 402
C73 0.1UF 20% 10V CERM 402
C39 0.1UF 20% 10V CERM 402
C107 0.1UF 20% 10V CERM 402
C90 0.1UF 20% 10V CERM 402
C257 0.1UF 20% 10V CERM 402
C272 0.1UF 20% 10V CERM 402
C188 0.1UF 20% 10V CERM 402
C155 0.1UF 20% 10V CERM 402
C92 0.1UF 20% 10V CERM 402
C224 0.1UF 20% 10V CERM 402
C40 0.1UF 20% 10V CERM 402
C194 0.1UF 20% 10V CERM 402
C203 0.1UF 20% 10V CERM 402
C273 0.1UF 20% 10V CERM 402
C41 0.1UF 20% 10V CERM 402
C169 0.1UF 20% 10V CERM 402
C139 0.1UF 20% 10V CERM 402
C106 0.1UF 20% 10V CERM 402

+1_5V_SLEEP
R702 0 5% 1/16W MF 603
1_5V_MAXBUS

+1_8V_SLEEP
R693 0 5% 1/16W MF 603
1_8V_MAXBUS

MPC7447 PULL-UPS

39 35 16 15 8 7 6 5 MAXBUS_SLEEP

R58 10K 5% 1/16W MF 402 — 8 5 CPU_TBEN
R160 10K 5% 1/16W MF 402 — 5 CPU_CHKS_L
R73 10K 5% 1/16W MF 402 — 5 CPU_SHD0_L
R87 10K 5% 1/16W MF 402 — 5 CPU_SHD1_L
R139 10K 5% 1/16W MF 402 — 5 CPU_MCP_L
R108 10K 5% 1/16W MF 402 — 5 CPU_LSSD_MODE
R72 10K 5% 1/16W MF 402 — 5 CPU_L2TSTCLK
R57 1K 5% 1/16W MF 402 — 40 5 CPU_CHKSTP_OUT_L
R148 10K 5% 1/16W MF 402 — 5 CPU_SRWX_L
R120 10K 5% 1/16W MF 402 — 5 CPU_PMONIN_L
R109 10K 5% 1/16W MF 402 — 5 CPU_EMODE1_L
R98 1K 5% 1/16W MF 402 — 5 CPU_PULLUP
R107 10K 5% 1/16W MF 402 — 40 7 6 5 CPU_HRESET_L
R129 10K 5% 1/16W MF 402 — 31 5 CPU_SMI_L

470OHM FOR BOOT BANGER
R59 470 5% 1/16W MF 402 — 40 6 5 JTAG_CPU_TMS

470OHM FOR BOOT BANGER
R128 470 5% 1/16W MF 402 — 40 6 5 JTAG_CPU_TDI

R79 10K 5% 1/16W MF 402 — 14 5 MPIC_CPU_INT_L
R65 10K 5% 1/16W MF 402 — 40 5 CPU_SRESET_L
R130 10K 5% 1/16W MF 402 — 5 CPU_L1TSTCLK
R60 10K 5% 1/16W MF 402 — 5 CPU_EDTI
R97 10K 5% 1/16W MF 402 — 40 6 5 JTAG_CPU_TCK
R61 470 5% 1/16W MF 402 — 5 CPU_PULLDOWN

CPU Interface

NC		D2
CPU_BR_L	37 8	M1 BR*
CPU_BG_L	37 8	BG*
CPU_TS_L	37 8	L4 TS*
		E11 A0
		H1 A1
		C11 A2
		G3 A3
CPU_ADDR<0>	37 8	F10 A4
CPU_ADDR<1>	37 8	L2 A5
CPU_ADDR<2>	37 8	D11 A6
CPU_ADDR<3>	37 8	D1 A7
CPU_ADDR<4>	37 8	C10 A8
CPU_ADDR<5>	37 8	G2 A9
CPU_ADDR<6>	37 8	D12 A10
CPU_ADDR<7>	37 8	L3 A11
CPU_ADDR<8>	37 8	G4 A12
CPU_ADDR<9>	37 8	T2 A13
CPU_ADDR<10>	37 8	F4 A14
CPU_ADDR<11>	37 8	V1 A15
CPU_ADDR<12>	37 8	J4 A16
CPU_ADDR<13>	37 8	R2 A17
CPU_ADDR<14>	37 8	K5 A18
CPU_ADDR<15>	37 8	W2 A19
CPU_ADDR<16>	37 8	J2 A20
CPU_ADDR<17>	37 8	K4 A21
CPU_ADDR<18>	37 8	N4 A22
CPU_ADDR<19>	37 8	J3 A23
CPU_ADDR<20>	37 8	M5 A24
CPU_ADDR<21>	37 8	P5 A25
CPU_ADDR<22>	37 8	N3 A26
CPU_ADDR<23>	37 8	T1 A27
CPU_ADDR<24>	37 8	V2 A28
CPU_ADDR<25>	37 8	U1 A29
CPU_ADDR<26>	37 8	N5 A30
CPU_ADDR<27>	37 8	W1 A31
CPU_ADDR<28>	37 8	B12 A32
CPU_ADDR<29>	37 8	C4 A33
CPU_ADDR<30>	37 8	G10 A34
CPU_ADDR<31>	37 8	B11 A35
NC		C1 AP0
NC		E3 AP1
		H6 AP2
		F5 AP3
		G7 AP4
CPU_TT<0>	37 8	E5 TT0
CPU_TT<1>	37 8	E6 TT1
CPU_TT<2>	37 8	F6 TT2
CPU_TT<3>	37 8	E9 TT3
CPU_TT<4>	37 8	C5 TT4
CPU_TBST_L	37 8	F11 TBST*
CPU_TSIZ<0>	37 8	G6 TSIZ0
CPU_TSIZ<1>	37 8	F7 TSIZ1
CPU_TSIZ<2>	37 8	E7 TSIZ2
CPU_GBL_L	37 8	E2 GBL*
CPU_WT_L	37 8	D3 WT*
CPU_CI_L	37 8	J1 CI*
CPU_AACK_L	37 8	R1 AACK*
CPU_ARTRY_L	37 8	N2 ARTRY*
CPU_SHD0_L	5	E4 SHD0*
CPU_SHD1_L	5	H5 SHD1*
CPU_HIT_L	37 8	B2 HIT*

OMIT
CRITICAL
U43
1.50GHZ-1.28V
APOLL7_PM-R1.1
BGA
(1 OF 3)

VDD		H8 H10 H12 J7 J9 J11 J13 K8 K10 K12 K14 L7 L9 L11 L13 M8 M10 M12
OVDD		B4 C2 C12 D5 F2 H3 J5 K2 L5 M3 N6 P2 P8 P11 R4 R13 R16 T9 U2 U12 U16 V4 V7 V10 V14 E18 G18
AVDD		A8
OVDDSENSE		
BVSEL		B7 CPU_BUS_VSEL 7
SYSCLK		A10 SYSCLK_CPU 8 37
CLK_OUT		H2 CPU_CLKOUT_SPN
PLL_CFG0		B8 CPU_PLL_CFG<0> 7
PLL_CFG1		C8 CPU_PLL_CFG<1> 7
PLL_CFG2		C7 CPU_PLL_CFG<2> 7
PLL_CFG3		D7 CPU_PLL_CFG<3> 7
PLL_CFG4		A7 CPU_PLL_CFG<4> 7
DBG*		M2 CPU_DBG_L 8 37
DRDY*		R3 CPU_DRDY_L 8 37
DTI0		G1 CPU_EDTI 5
DTI1		K1 CPU_DTI<0> 8 37
DTI2		P1 CPU_DTI<1> 8 37
DTI3		N1 CPU_DTI<2> 8 37
TDI		B9 JTAG_CPU_TDI 5 6 40
TDO		A4 JTAG_CPU_TDO_TP 40
TMS		F1 JTAG_CPU_TMS 5 6 40
TCK		C6 JTAG_CPU_TCK 5 6 40
TRST*		A5 JTAG_CPU_TRST_L 6 40
LSSD_MODE*		E8 CPU_LSSD_MODE 5
L1_TSTCLK		G8 CPU_L1TSTCLK 5
L2_TSTCLK		B3 CPU_L2TSTCLK 5
TA*		K6 CPU_TA_L 8 37
TEA*		L1 CPU_TEA_L 8 37
TBEN		E1 CPU_TBEN 5
QREQ*		P4 CPU_QREQ_L 8 37
QACK*		G5 CPU_QACK_L 8 37
CKSTP_IN*		A3
CKSTP_OUT*		B1 CPU_CKSTP_OUT_L 5 40
INT*		D4 MPIC_CPU_INT_L 5 14
SMI*		E9 CPU_SMI_L 5 31
MCP*		C9 CPU_MCP_L 5
SRESET*		A2 CPU_SRESET_L 5 40
HRESET*		D8 CPU_HRESET_L 5 6 7 40
NC		
PMON_IN*		D9 CPU_PMONIN_L 5
PMON_OUT*		A9
BMODE0*		G9 CPU_EMODE0_L 7
BMODE1*		F8 CPU_EMODE1_L 5
EXT_QUAL		A11 CPU_PULLDOWN 5
CHKS*		A12 CPU_CHKS_L 5
SRW0*		B10 CPU_PULLUP 5
SRW1*		E10 CPU_SRWX_L 5
IARTRY0*		B6 CPU_PULLUP 5
DX*		D10 CPU_PULLDOWN 5

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2955	1	IC,A7PM,1.67GHZ,1.28V,25W,R1.2.3	U43	CRITICAL	CPU_VCORE128_R123
337S3094	1	IC,A7PM,1.67GHZ,1.3V,25W,R1.2.3	U43	CRITICAL	CPU_VCORE13_R123
337S3131	1	IC,A7PM,1.67GHZ,1.3V,25W,R1.4	U43	CRITICAL	CPU_VCORE13_R14
337S3216	1	IC,A7PM,1.67GHZ,1.3V,25W,R1.5	U43	CRITICAL	CPU_VCORE13_R15

GND

NO STUFF
R106 10 1% 1/16W MF 402
1 2 CPU_VCORE_SLEEP 5 6 35 39 40

CPU_AVDD
R280 10 1% 1/16W MF 402
CPU_AVDD_VOUT
VOUT = 0.59*(1+R1/R2)
PLACE R282 AND R283 CLOSE TO U6X PIN 5 AND 6

C137 0.1UF 20% 10V CERM 402
C136 4.7UF 20% 6.3V CERM 805
+3V_SLEEP
R276 0 5% 1/16W MF-LF 603 2 1
MIN_NECK_WIDTH=10MIL
MIN_LINE_WIDTH=25MIL
CPU_AVDD_VIN

CRITICAL
U6
FAN2558 SOT23-6
1 VIN
4 PG
3 EN
6 VOUT
5 ADJ
2 GND

C283 2.2UF 20% 6.3V CERM1 603
C946 0.001UF 10% 50V CERM 402
R1 R282 118K 1% 1/16W MF 402
VCORE128 R283 100K 1% 1/16W MF 402
R2
C909 1UF 10% 6.3V CERM 402
CPU_AVDD_ADJ

CPU_AVDD_SHDN_L
NO STUFF
D35 SM MBR0530
R275 0 5% 1/16W MF 402
NO STUFF
C945 0.1UF 20% 10V CERM 402
VCORE_SHDN_L 35

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S9764	1	RES,97.6KOHM,1%,1/16W,0402	R283	VCORE13

MPC7447 MAXBUS

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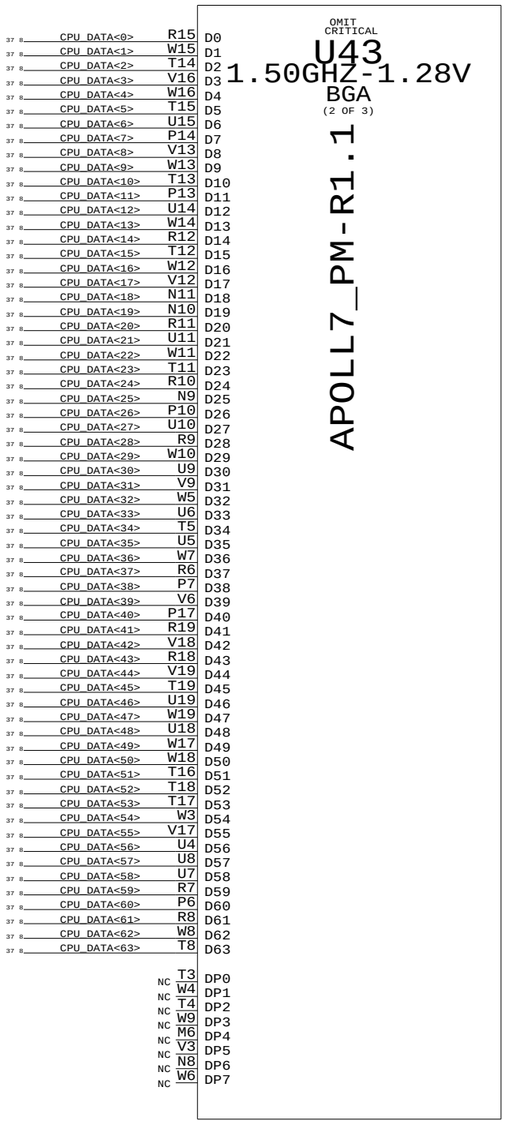
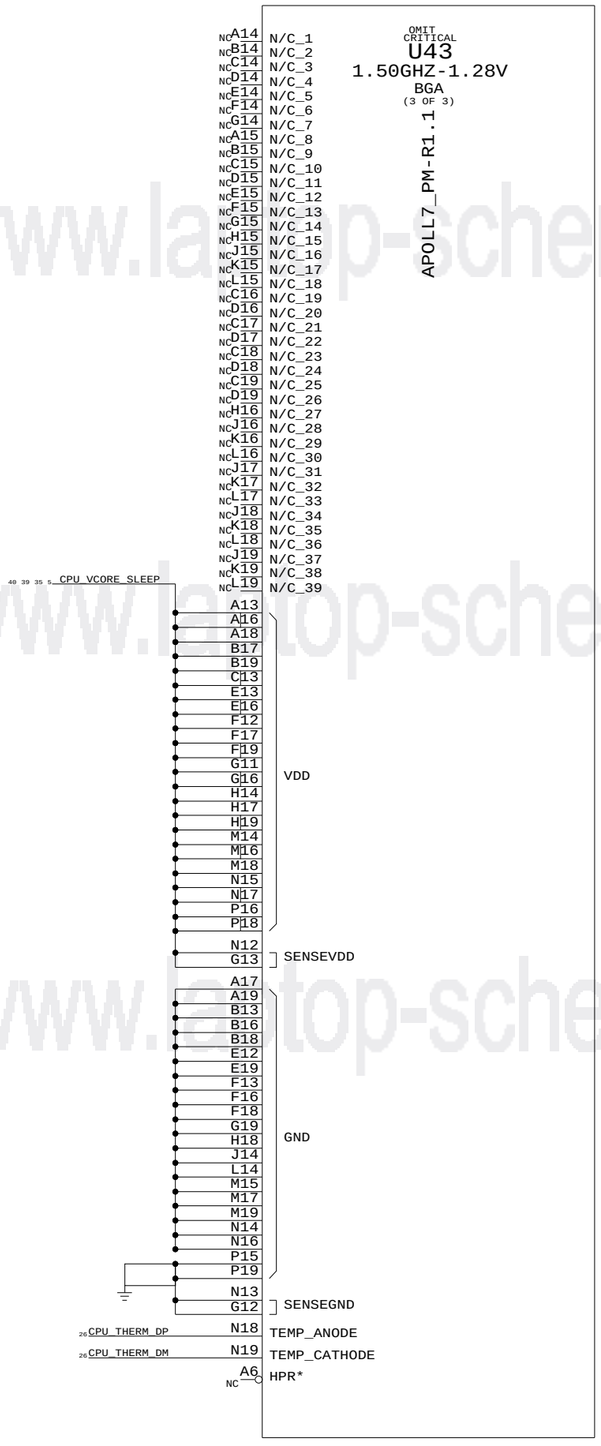
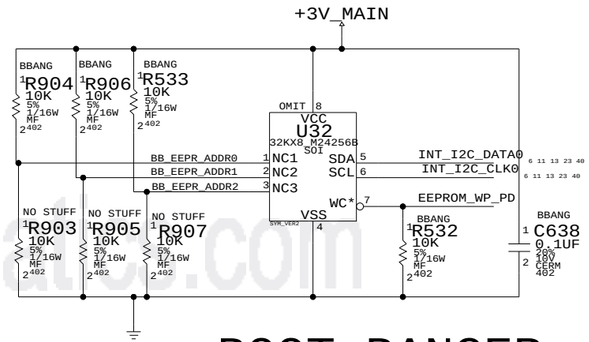
APPLE COMPUTER INC.

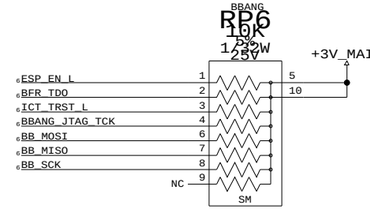
SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 5 OF 45	



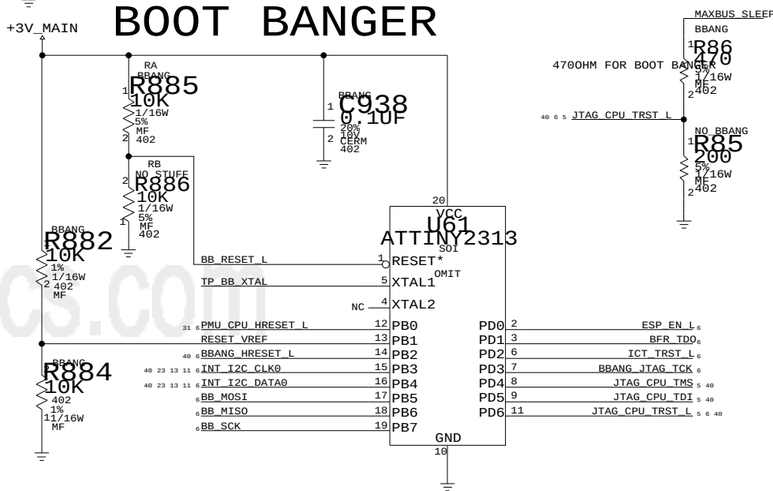


BOOT BANGER E2PROM



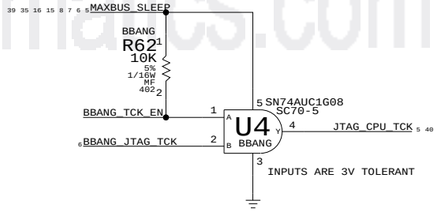


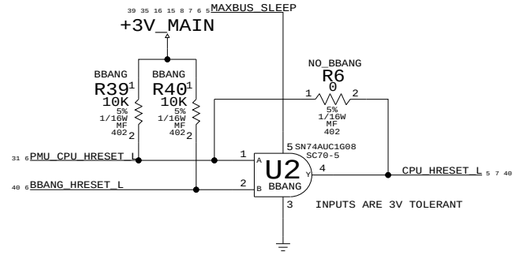
BOOT BANGER



UNSTUFFING RA AND STUFFING RB
WILL DISABLE THE CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1660	1	MCU,PROGRAMMED W/ BANGER	U61	BBANG
341S1661	1	I2C EEPROM,PROGRAMMED W/ BANGER	U32	BBANG





BOOT BANGING SIGNAL DEFINITION

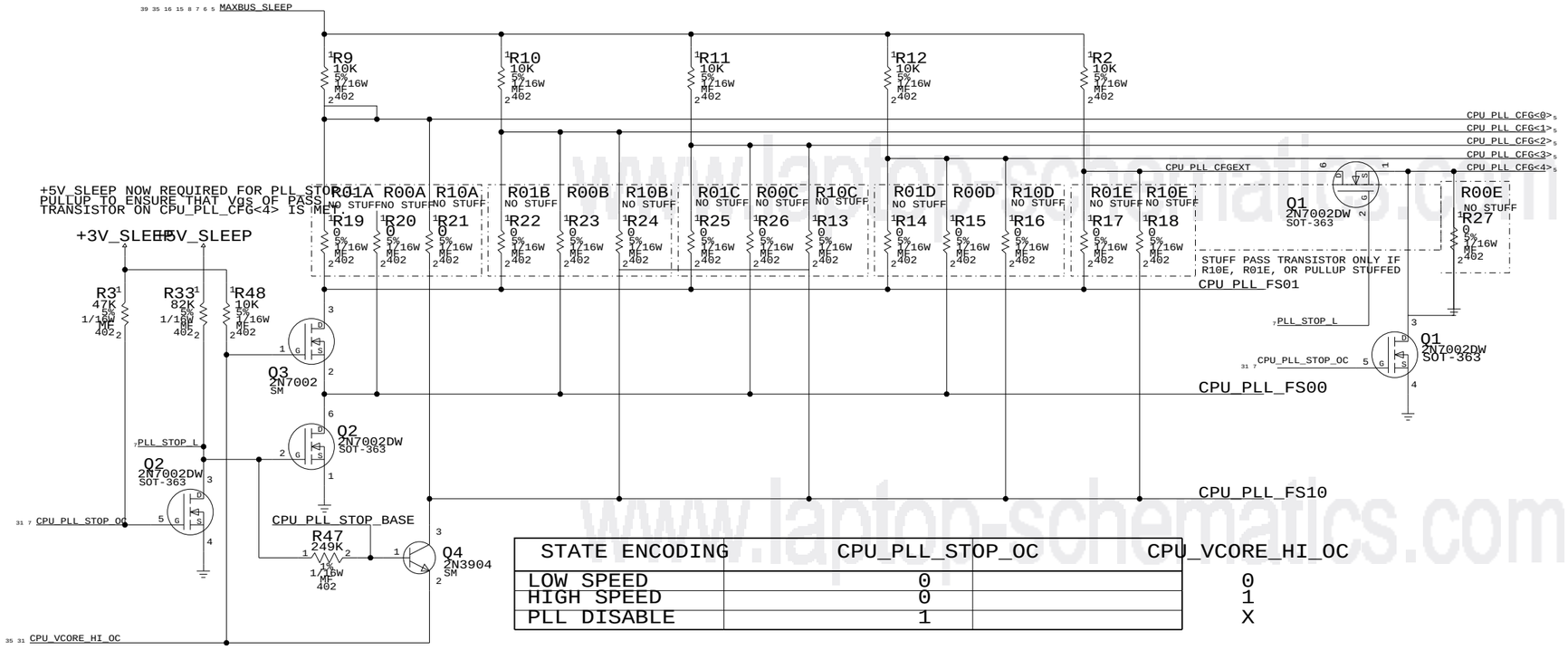
1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)

MPC7447/BBANG

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 6 OF 45	

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC		CPU_VCORE_HI_OC
LOW SPEED	0		0
HIGH SPEED	0		1
PLL DISABLE	1		X

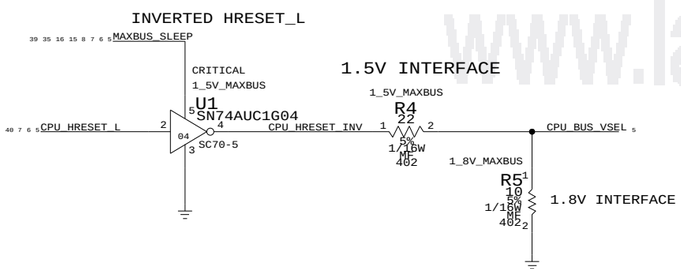
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 0123 E ABCD HEX
0.0X	PLL OFF		0 1111 0F
1.0X	PLL BYPASS		0 0011 03
2.0X	333	267	0 0100 04
3.0X	500	400	0 1000 08
4.0X	667	533	0 1010 0A
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
8.5X	1417	1133	0 0110 06
9.0X	1500	1200	1 0111 17
9.5X	1583	1267	0 0111 07
10.0X	1667	1333	1 1010 1A
10.5X	1750	1400	1 1000 18
11.0X	1833	1467	1 1001 19
11.5X	1917	1533	0 0000 00
12.0X	2000	1600	1 1011 1B
12.5X	2083	1667	1 1111 1F
13.0X	2167	1733	1 0101 15
13.5X	2250	1800	0 1110 0E
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D
17.0X	2833	2267	1 0000 10
18.0X	3000	2400	1 0010 12
20.0X	3333	2667	1 0011 13
21.0X	3500	2800	1 0100 14
24.0X	4000	3200	1 0110 16
28.0X	4667	3733	1 1110 1E

CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT

APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G

SCALE	SHT	OF
NONE	7	45

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF
R642[1]	R135[1]	R123[1]	R153[1]	R166[1]	R179[1]	R651[1]	R178[1]
10K 5% 1/16W MF 402[2]							
CPU_DATA<32>	CPU_DATA<33>	CPU_DATA<34>	CPU_DATA<35>	CPU_DATA<36>	CPU_DATA<37>	CPU_DATA<38>	CPU_DATA<39>

NO STUFF

R136[1]	R643[1]	R639[1]	R657[1]	R664[1]	R673[1]	R143[1]	R674[1]
10K 5% 1/16W MF 402[2]							
Bit 39 Power Up Output Tristate Control	Bit 38 Output Clock Driver Tristate Control	Bit 37 Alternate PLL Configuration	Bit 36 Alternate VCO Range	Extra Slow Pull Down	Spare	Spare	Spare

BIT 40 TO 47

MAXBUS_SLEEP

NO STUFF	NO STUFF	NO STUFF	EXT_CLK	NO STUFF	INT_CLK	INT_CLK	INT_CLK
R122[1]	R142[1]	R164[1]	R134[1]	R184[1]	R177[1]	R152[1]	R165[1]
10K 5% 1/16W MF 402[2]							
CPU_DATA<40>	CPU_DATA<41>	CPU_DATA<42>	CPU_DATA<43>	CPU_DATA<44>	CPU_DATA<45>	CPU_DATA<46>	CPU_DATA<47>

R640[1]	R652[1]	R665[1]	R644[1]	R683[1]	R675[1]	R658[1]	R666[1]
10K 5% 1/16W MF 402[2]							
Spare	Spare	BIT2	BIT1	BIT0	PCI1 Source Clock 1: PLL3 (SPREAD) 0: PLL3 (NO SPREAD)	PCI0 Source Clock 1: PLL3 (SPREAD) 0: PLL3 (NO SPREAD)	

INT_CLK EXT_CLK EXT_CLK EXT_CLK

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

MAXBUS_SLEEP

EXT_CLK	EXT_CLK	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	
R133[1]	R121[1]	R163[1]	R151[1]	R162[1]	R141[1]	R183[1]	R176[1]
10K 5% 1/16W MF 402[2]							
CPU_DATA<48>	CPU_DATA<49>	CPU_DATA<50>	CPU_DATA<51>	CPU_DATA<52>	CPU_DATA<53>	CPU_DATA<54>	CPU_DATA<55>

INT_CLK	INT_CLK	NO STUFF	NO STUFF				
R645[1]	R641[1]	R668[1]	R659[1]	R667[1]	R653[1]	R684[1]	R676[1]
10K 5% 1/16W MF 402[2]							
BUF_REF_CLK_OUTEnable_h: Active	Select PLL4ExtSrc 1: External source	Spare	BIT2	BIT1	BIT0	Spare	

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

+1 5V INTREPID PLL → R227 4.7 5% 1/16W MF 402 → +1 5V INTREPID PLL7

C308 0.22UF 20% 6.3V CERM 402

H26 VDD15A_7 (PLL6) OMIT CRITICAL

U45 INTREPID-REV2.1 BGA

CPU_BR_L	E29	BR	INPUT - PU
CPU_BG_L	E26	BG	NO BUS KEEPER
CPU_TS_L	B27	TS	NO BUS KEEPER

(1 OF 9)

CPU_ADDR<0>	D24	A_0
CPU_ADDR<1>	D25	A_1
CPU_ADDR<2>	A27	A_2
CPU_ADDR<3>	E24	A_3
CPU_ADDR<4>	G23	A_4
CPU_ADDR<5>	B26	A_5
CPU_ADDR<6>	A26	A_6
CPU_ADDR<7>	D23	A_7
CPU_ADDR<8>	A25	A_8
CPU_ADDR<9>	E23	A_9
CPU_ADDR<10>	J22	A_10
CPU_ADDR<11>	B25	A_11
CPU_ADDR<12>	H22	A_12
CPU_ADDR<13>	G22	A_13
CPU_ADDR<14>	D22	A_14
CPU_ADDR<15>	B24	A_15
CPU_ADDR<16>	B23	A_16
CPU_ADDR<17>	E22	A_17
CPU_ADDR<18>	J21	A_18
CPU_ADDR<19>	G21	A_19
CPU_ADDR<20>	E21	A_20
CPU_ADDR<21>	A24	A_21
CPU_ADDR<22>	D21	A_22
CPU_ADDR<23>	A23	A_23
CPU_ADDR<24>	H20	A_24
CPU_ADDR<25>	B22	A_25
CPU_ADDR<26>	H21	A_26
CPU_ADDR<27>	A22	A_27
CPU_ADDR<28>	E20	A_28
CPU_ADDR<29>	B21	A_29
CPU_ADDR<30>	D20	A_30
CPU_ADDR<31>	A21	A_31

MAXBUS INTERFACE

CPU_CI_L	G26	CI
CPU_GBL_L	A29	GBL
CPU_TBST_L	A28	TBST
CPU_TSIZ<0>	G24	TSIZ_0
CPU_TSIZ<1>	H24	TSIZ_1
CPU_TSIZ<2>	D26	TSIZ_2
CPU_TT<0>	E25	TT_0
CPU_TT<1>	G25	TT_1
CPU_TT<2>	B28	TT_2
CPU_TT<3>	D27	TT_3
CPU_TT<4>	J25	TT_4
CPU_WT_L	D28	WT
CPU_AACK_L	B29	AACK NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT INPUT - PU
CPU_QREQ_L	A32	QREQ INPUT - PD
CPU_QACK_L	G27	QACK NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ
INT_SUSPEND_ACK_L	AM8	SUSPENDACK

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

INT_CPUFB_IN	J24	CPU_FB_IN	
INT_CPUFB_OUT	H16	CPU_FB_OUT	NO BUS KEEPER - PU
SYSCLK_LA_TP	G8	ANALYZER_CLK	
CPU_CLK_EN	AH9	STOPCPUCLK	INPUT - PU
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - ?
SYSCLK_CPU_UF	J15	CPU_CLK	NO BUS KEEPER - PU
CPU_TBEN	A31	TBEN	NO BUS KEEPER - PU

R197[1] 511 1% 1/16W MF 402

R144 0 5% 1/16W MF 402 ← SYSCLK_CPU1

R137[1] 1K 1% 1/16W MF 402

INTREPID OUTPUTS HIGH BY DEFAULT

VSSA_7 (PLL6) H25

DBG	A30	CPU_DBG_L
DRDY	G28	CPU_DRDY_L
DTI_0	K25	CPU_DTI<0>
DTI_1	D29	CPU_DTI<1>
DTI_2	B30	CPU_DTI<2>
TA	E27	CPU_TA_L
TEA	E28	CPU_TEA_L

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

INT_CPUFB_OUT → R167 0 5% 1/16W MF 402 → INT_CPUFB_OUT_SHORT → R215 0 5% 1/16W MF 402 → INT_CPUFB_OUT_NORM → R207 NO STUFF 0 5% 1/16W MF 402 → INT_CPUFB_LONG

R225[1] NO STUFF 0 5% 1/16W MF 402[2]

R208[1] 0 5% 1/16W MF 402[2] NO STUFF

R226 0 5% 1/16W MF 402

R196 NO STUFF 0 5% 1/16W MF 402

INT_CPUFB_IN → INT_CPUFB_IN_NORM

MAXBUS PULL-UPS

MAXBUS_SLEEP

CPU_TS_L	RP21 10K 5% 1/16W SM1	2 7
CPU_TA_L	RP21 10K 5% 1/16W SM1	1 8
CPU_ARTRY_L	RP21 10K 5% 1/16W SM1	4 5
CPU_BR_L	RP23 10K 5% 1/16W SM1	1 8
CPU_HIT_L	RP24 10K 5% 1/16W SM1	3 6
CPU_DRDY_L	RP23 10K 5% 1/16W SM1	3 6
CPU_TEA_L	RP23 10K 5% 1/16W SM1	4 5
CPU_AACK_L	RP23 10K 5% 1/16W SM1	2 7
CPU_DBG_L	RP24 10K 5% 1/16W SM1	4 5
CPU_BG_L	RP21 10K 5% 1/16W SM1	3 6
CPU_QREQ_L	RP24 10K 5% 1/16W SM1	2 7

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF		NO STUFF
R140[1]	R161[1]	R175[1]	R132[1]	R131[1]	R150[1]	R174[1]	R182[1]
10K 5% 1/16W MF 402[2]							
CPU_DATA<56>	CPU_DATA<57>	CPU_DATA<58>	CPU_DATA<59>	CPU_DATA<60>	CPU_DATA<61>	CPU_DATA<62>	CPU_DATA<63>

NO STUFF

R654[1]	R669[1]	R677[1]	R646[1]	R647[1]	R660[1]	R678[1]	R685[1]
10K 5% 1/16W MF 402[2]							
Spare	Spare	Spare	PCI1_REQ2_L / PCI1_GNT2_L 1: GPIO5	PCI1_REQ1_L / PCI1_GNT1_L 1: GPIO4	PCI1_REQ0_L / PCI1_GNT0_L 1: GPIO3	Ethernet PHY interface 1: B-mode interface	Processor Bus Mode 1: 60X Bus (64)

Intrepid MaxBus

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 8 OF 45	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

U45
INTREPID-REV2.1
BGA
(2 OF 9)
OMIT
CRITICAL

DDR_DATA_0 AK32 MEM_DATA<0>
DDR_DATA_1 AK33 MEM_DATA<1>
DDR_DATA_2 AK31 MEM_DATA<2>
DDR_DATA_3 AK35 MEM_DATA<3>
DDR_DATA_4 AK36 MEM_DATA<4>
DDR_DATA_5 AJ32 MEM_DATA<5>
DDR_DATA_6 AJ35 MEM_DATA<6>
DDR_DATA_7 AJ36 MEM_DATA<7>
DDR_DATA_8 AG33 MEM_DATA<8>
DDR_DATA_9 AG35 MEM_DATA<9>
DDR_DATA_10 AH35 MEM_DATA<10>
DDR_DATA_11 AG36 MEM_DATA<11>
DDR_DATA_12 AH36 MEM_DATA<12>
DDR_DATA_13 AH32 MEM_DATA<13>
DDR_DATA_14 AG32 MEM_DATA<14>
DDR_DATA_15 AG31 MEM_DATA<15>
DDR_DATA_16 AE32 MEM_DATA<16>
DDR_DATA_17 AF35 MEM_DATA<17>
DDR_DATA_18 AF36 MEM_DATA<18>
DDR_DATA_19 AE36 MEM_DATA<19>
DDR_DATA_20 AE35 MEM_DATA<20>
DDR_DATA_21 AE33 MEM_DATA<21>
DDR_DATA_22 AD36 MEM_DATA<22>
DDR_DATA_23 AD35 MEM_DATA<23>
DDR_DATA_24 AA36 MEM_DATA<24>
DDR_DATA_25 AA35 MEM_DATA<25>
DDR_DATA_26 AA33 MEM_DATA<26>
DDR_DATA_27 AB36 MEM_DATA<27>
DDR_DATA_28 AB35 MEM_DATA<28>
DDR_DATA_29 AC36 MEM_DATA<29>
DDR_DATA_30 AA32 MEM_DATA<30>
DDR_DATA_31 AB33 MEM_DATA<31>
DDR_DATA_32 V36 MEM_DATA<32>
DDR_DATA_33 U33 MEM_DATA<33>
DDR_DATA_34 U32 MEM_DATA<34>
DDR_DATA_35 V35 MEM_DATA<35>
DDR_DATA_36 T30 MEM_DATA<36>
DDR_DATA_37 U36 MEM_DATA<37>
DDR_DATA_38 U35 MEM_DATA<38>
DDR_DATA_39 T36 MEM_DATA<39>
DDR_DATA_40 P33 MEM_DATA<40>
DDR_DATA_41 R30 MEM_DATA<41>
DDR_DATA_42 P35 MEM_DATA<42>
DDR_DATA_43 P36 MEM_DATA<43>
DDR_DATA_44 R36 MEM_DATA<44>
DDR_DATA_45 R35 MEM_DATA<45>
DDR_DATA_46 R33 MEM_DATA<46>
DDR_DATA_47 R32 MEM_DATA<47>
DDR_DATA_48 N35 MEM_DATA<48>
DDR_DATA_49 M36 MEM_DATA<49>
DDR_DATA_50 L35 MEM_DATA<50>
DDR_DATA_51 M35 MEM_DATA<51>
DDR_DATA_52 M33 MEM_DATA<52>
DDR_DATA_53 L36 MEM_DATA<53>
DDR_DATA_54 N33 MEM_DATA<54>
DDR_DATA_55 M30 MEM_DATA<55>
DDR_DATA_56 J32 MEM_DATA<56>
DDR_DATA_57 J33 MEM_DATA<57>
DDR_DATA_58 J35 MEM_DATA<58>
DDR_DATA_59 K32 MEM_DATA<59>
DDR_DATA_60 K33 MEM_DATA<60>
DDR_DATA_61 J36 MEM_DATA<61>
DDR_DATA_62 K36 MEM_DATA<62>
DDR_DATA_63 K35 MEM_DATA<63>

DDR MEMORY INTERFACE

DDR_A_0 H35 MEM_ADDR<0>
DDR_A_1 G35 MEM_ADDR<1>
DDR_A_2 G36 MEM_ADDR<2>
DDR_A_3 F36 MEM_ADDR<3>
DDR_A_4 F35 MEM_ADDR<4>
DDR_A_5 E35 MEM_ADDR<5>
DDR_A_6 E36 MEM_ADDR<6>
DDR_A_7 G32 MEM_ADDR<7>
DDR_A_8 D36 MEM_ADDR<8>
DDR_A_9 H36 MEM_ADDR<9>
DDR_A_10 G33 MEM_ADDR<10>
DDR_A_11 H33 MEM_ADDR<11>
DDR_A_12 D35 MEM_ADDR<12>
DDR_BA_0 L30 MEM_BA<0>
DDR_BA_1 M29 MEM_BA<1>

DDRCS_0 AN34 MEM_CS_L<0>
DDRCS_1 AN36 MEM_CS_L<1>
DDRCS_2 AL35 MEM_CS_L<2>
DDRCS_3 AL33 MEM_CS_L<3>
'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

DDR_DQS_0 AJ31 MEM_DQS<0>
DDR_DQS_1 AH31 MEM_DQS<1>
DDR_DQS_2 AD32 MEM_DQS<2>
DDR_DQS_3 AB30 MEM_DQS<3>
DDR_DQS_4 V30 MEM_DQS<4>
DDR_DQS_5 P32 MEM_DQS<5>
DDR_DQS_6 N29 MEM_DQS<6>
DDR_DQS_7 L32 MEM_DQS<7>

DDR_DM_0 AJ33 MEM_DQM<0>
DDR_DM_1 AH33 MEM_DQM<1>
DDR_DM_2 AD33 MEM_DQM<2>
DDR_DM_3 AC35 MEM_DQM<3>
DDR_DM_4 T35 MEM_DQM<4>
DDR_DM_5 T33 MEM_DQM<5>
DDR_DM_6 N32 MEM_DQM<6>
DDR_DM_7 L33 MEM_DQM<7>

DDRRAS L29 MEM_RAS_L
DDRCAS H32 MEM_CAS_L
DDRWE K30 MEM_WE_L

DDRCKE0 AN35 MEM_CKE<0>
DDRCKE1 AM35 MEM_CKE<1>
DDRCKE2 AM36 MEM_CKE<2>
DDRCKE3 AL36 MEM_CKE<3>
'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

DDR_SELHI_0 AB32 MEM_MUXSEL_H<0>
DDR_SELHI_1 AE29 MEM_MUXSEL_H<1>
DDR_SELLO_0 N30 MEM_MUXSEL_L<0>
DDR_SELLO_1 T32 MEM_MUXSEL_L<1>
'0'S ARE SAME POLARITY (ACTIVE-LO)
'1'S ARE SAME POLARITY (ACTIVE-HI)

DDR_MCLK_0_P Y32 SYSCLK_DDRCLK_A0_UF
DDR_MCLK_0_N Y33 SYSCLK_DDRCLK_A0_L_UF
DDR_MCLK_1_P Y35 SYSCLK_DDRCLK_A1_UF
DDR_MCLK_1_N Y36 SYSCLK_DDRCLK_A1_L_UF
DDR_MCLK_2_P Y30 INT_DDRCLK2_P_TP
DDR_MCLK_2_N W30 INT_DDRCLK2_N_TP
DDR_MCLK_3_P W32 SYSCLK_DDRCLK_B0_UF
DDR_MCLK_3_N W33 SYSCLK_DDRCLK_B0_L_UF
DDR_MCLK_4_P V33 SYSCLK_DDRCLK_B1_UF
DDR_MCLK_4_N V32 SYSCLK_DDRCLK_B1_L_UF
DDR_MCLK_5_P W35 INT_DDRCLK5_P_TP
DDR_MCLK_5_N W36 INT_DDRCLK5_N_TP

DDR_REF AA22 INT_MEM_REF_H
DDR_VREF_0 Y22 INT_MEM_VREF
DDR_VREF_1 T22

R199 1K 1% 1/16W MF 402

MEM_VREF

+2_5V_INTREPID
R198 10K 1% 1/16W MF 402
R191 10K 1% 1/16W MF 402
C245 0.1UF 20% 10V CERM 402
INT_MEM_VREF

CLOCKS
SYSCLK_DDRCLK_A1_UF — RP33 22 — SYSCLK_DDRCLK_A1
SYSCLK_DDRCLK_A1_L_UF — RP33 22 — SYSCLK_DDRCLK_A1_L
SYSCLK_DDRCLK_A0_UF — RP34 22 — SYSCLK_DDRCLK_A0
SYSCLK_DDRCLK_A0_L_UF — RP34 22 — SYSCLK_DDRCLK_A0_L
SYSCLK_DDRCLK_B1_UF — RP33 22 — SYSCLK_DDRCLK_B1
SYSCLK_DDRCLK_B1_L_UF — RP33 22 — SYSCLK_DDRCLK_B1_L
SYSCLK_DDRCLK_B0_UF — RP34 22 — SYSCLK_DDRCLK_B0
SYSCLK_DDRCLK_B0_L_UF — RP34 22 — SYSCLK_DDRCLK_B0_L

CS
MEM_CS_L<0> — RP36 22 — RAM_CS_L<0>
MEM_CS_L<1> — RP36 22 — RAM_CS_L<1>
MEM_CS_L<2> — RP35 22 — RAM_CS_L<2>
MEM_CS_L<3> — RP35 22 — RAM_CS_L<3>

CKE
MEM_CKE<0> — RP36 22 — RAM_CKE<0>
MEM_CKE<1> — RP36 22 — RAM_CKE<1>
MEM_CKE<2> — RP35 22 — RAM_CKE<2>
MEM_CKE<3> — RP35 22 — RAM_CKE<3>

ADDR
MEM_ADDR<0> — RP31 22 — RAM_ADDR<0>
MEM_ADDR<1> — RP25 22 — RAM_ADDR<1>
MEM_ADDR<2> — RP25 22 — RAM_ADDR<2>
MEM_ADDR<3> — RP25 22 — RAM_ADDR<3>
MEM_ADDR<4> — RP25 22 — RAM_ADDR<4>
MEM_ADDR<5> — RP30 22 — RAM_ADDR<5>
MEM_ADDR<6> — RP30 22 — RAM_ADDR<6>
MEM_ADDR<7> — RP31 22 — RAM_ADDR<7>
MEM_ADDR<8> — RP30 22 — RAM_ADDR<8>
MEM_ADDR<9> — RP31 22 — RAM_ADDR<9>
MEM_ADDR<10> — RP31 22 — RAM_ADDR<10>
MEM_ADDR<11> — RP26 22 — RAM_ADDR<11>
MEM_ADDR<12> — RP30 22 — RAM_ADDR<12>

BA
MEM_BA<0> — RP26 22 — RAM_BA<0>
MEM_BA<1> — RP26 22 — RAM_BA<1>

CNTL
MEM_WE_L — RP26 22 — RAM_WE_L
MEM_CAS_L — R250 22 — RAM_CAS_L
MEM_RAS_L — R238 22 — RAM_RAS_L

1MB BOOT ROM

+3V_MAIN
C460 2.2UF 20% 10V CERM 805
C470 0.1UF 20% 10V CERM 402
C479 0.1UF 20% 10V CERM 402

U17
3.3V
TSOP
VPP 11
VCC 30, 31
OMIT
GND 23, 39

A0 21 PCI_AD<0>
A1 20 PCI_AD<1>
A2 19 PCI_AD<2>
A3 18 PCI_AD<3>
A4 17 PCI_AD<4>
A5 16 PCI_AD<5>
A6 15 PCI_AD<6>
A7 14 PCI_AD<7>
A8 8 PCI_AD<8>
A9 7 PCI_AD<9>
A10 36 PCI_AD<10>
A11 6 PCI_AD<11>
A12 5 PCI_AD<12>
A13 4 PCI_AD<13>
A14 3 PCI_AD<14>
A15 2 PCI_AD<15>
A16 1 PCI_AD<16>
A17 40 PCI_AD<17>
A18 13 PCI_AD<18>
A19 37 PCI_AD<19>
A20 38 PCI_AD<20>

DQ0 25 PCI_AD<24>
DQ1 26 PCI_AD<25>
DQ2 27 PCI_AD<26>
DQ3 28 PCI_AD<27>
DQ4 32 PCI_AD<28>
DQ5 33 PCI_AD<29>
DQ6 34 PCI_AD<30>
DQ7 35 PCI_AD<31>

CE 22 ROM_ONBOARD_CS_L
OE 24 ROM_OE_L
WE 9 ROM_RW_L
WP 12 ROM_WP_L
PWD 10 INT_RESET_L

+3V_MAIN
R338 10K 5% 1/16W MF 402
R386 10K 5% 1/16W MF 402
R357 1K 5% 1/16W MF 402
ROM_CS_L

OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1793	1	IC,BOOTROM,4.9.1F3,Q41B	U17	CRITICAL	?

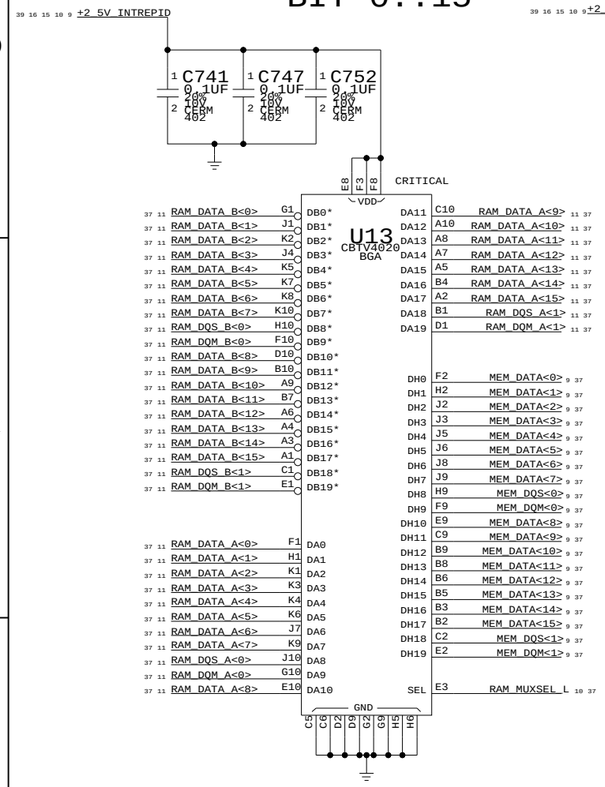
PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF

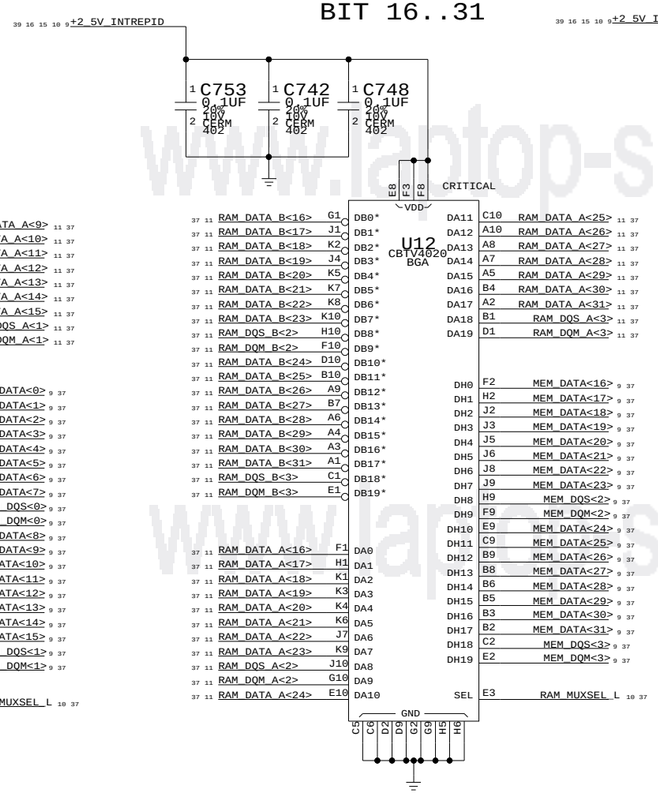
RAM_CKE<0>
RAM_CKE<1>
RAM_CKE<2>
RAM_CKE<3>
R500 10K 5% 1/16W MF 402
R439 10K 5% 1/16W MF 402
R409 10K 5% 1/16W MF 402
R387 10K 5% 1/16W MF 402

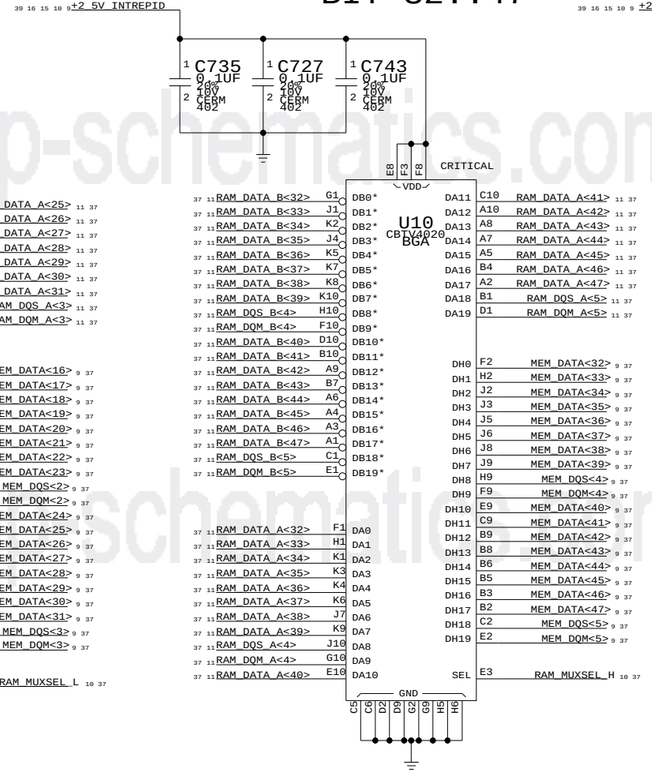
INT - DDR/BOOTROM

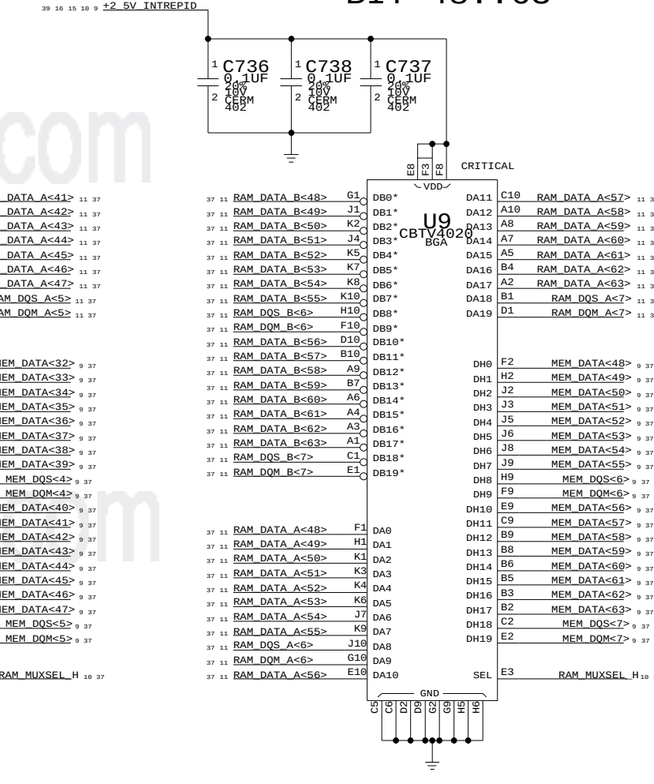
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 9 OF 45	



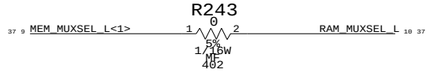






SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG



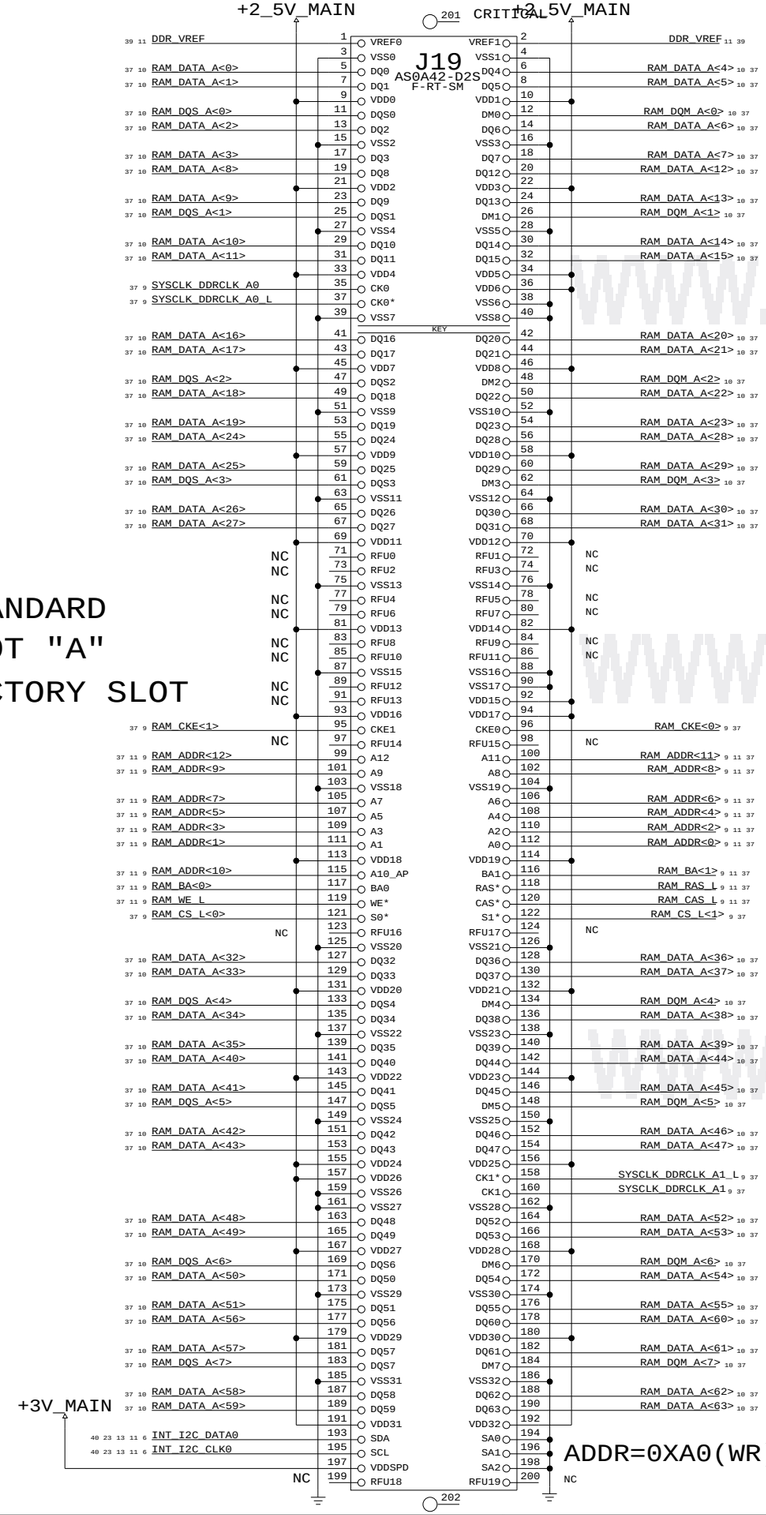
16BIT 2:1 DDR MUXES

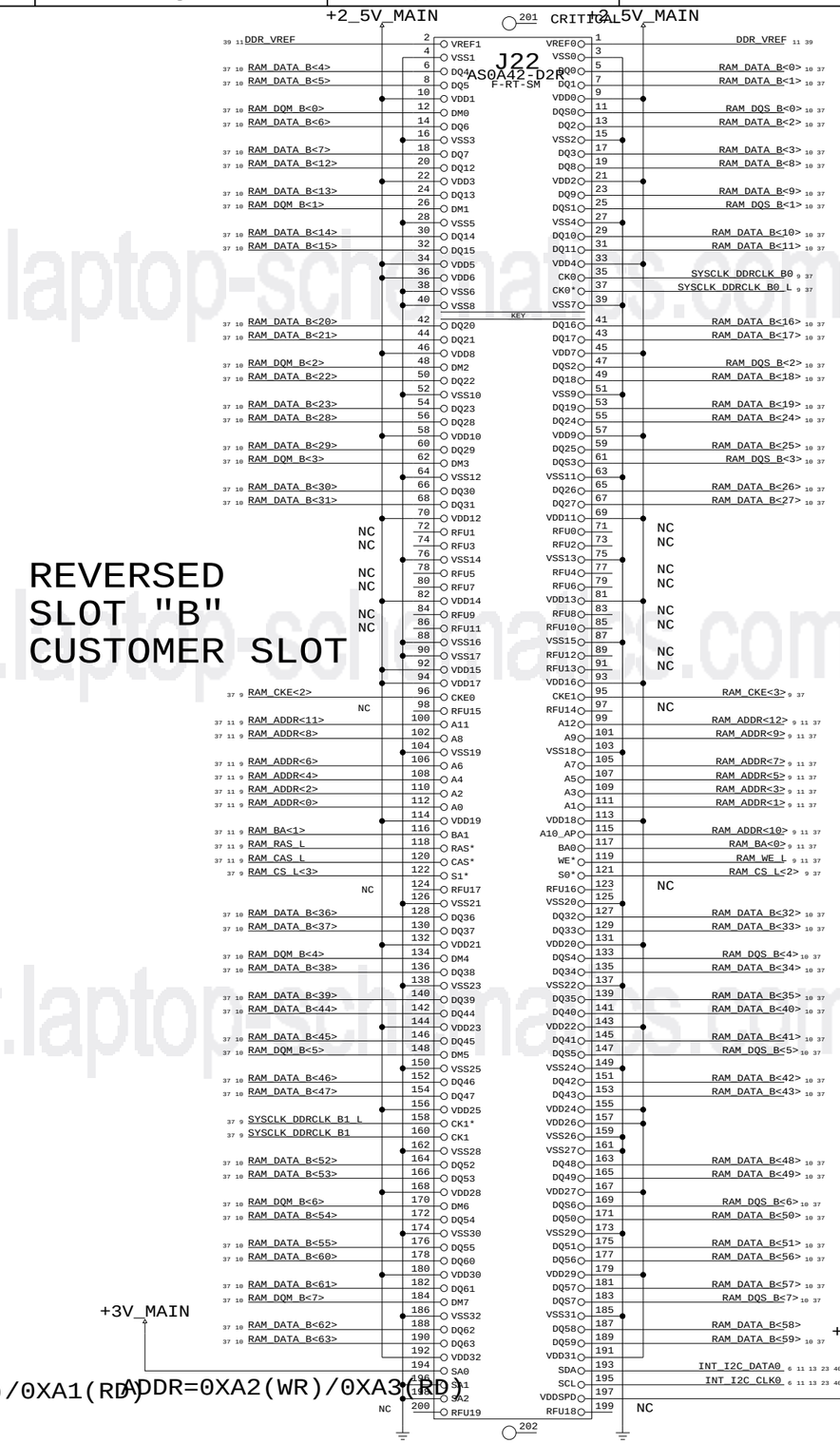
APPLE COMPUTER INC.

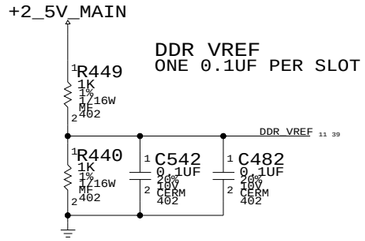
SIZE	DRAWING NUMBER	REV.
D	051-6694	G

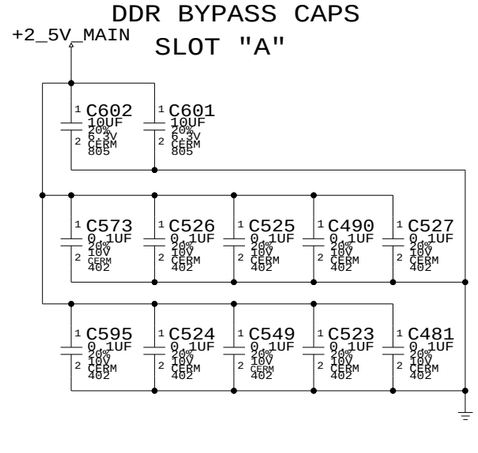
SCALE: NONE

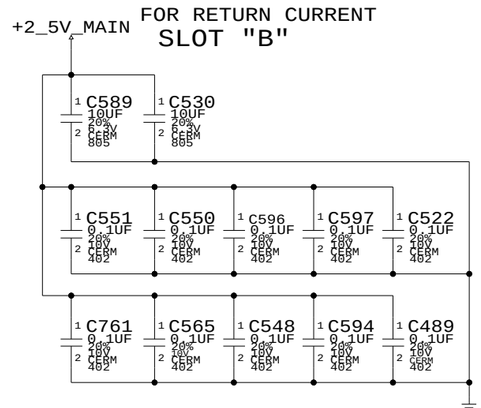
SHT 10 OF 45











DDR SODIMM CONNS

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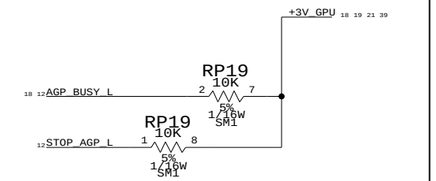
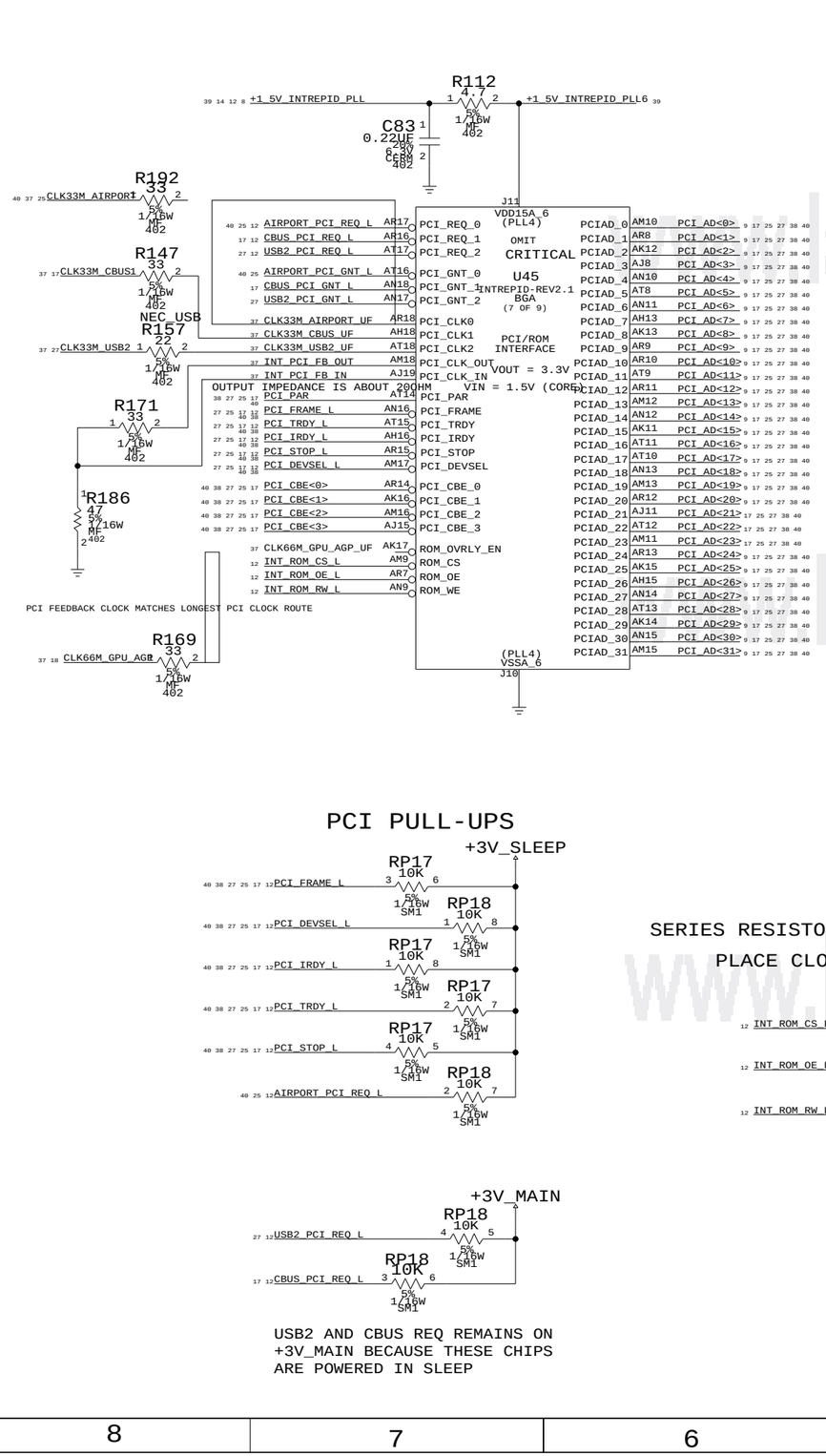
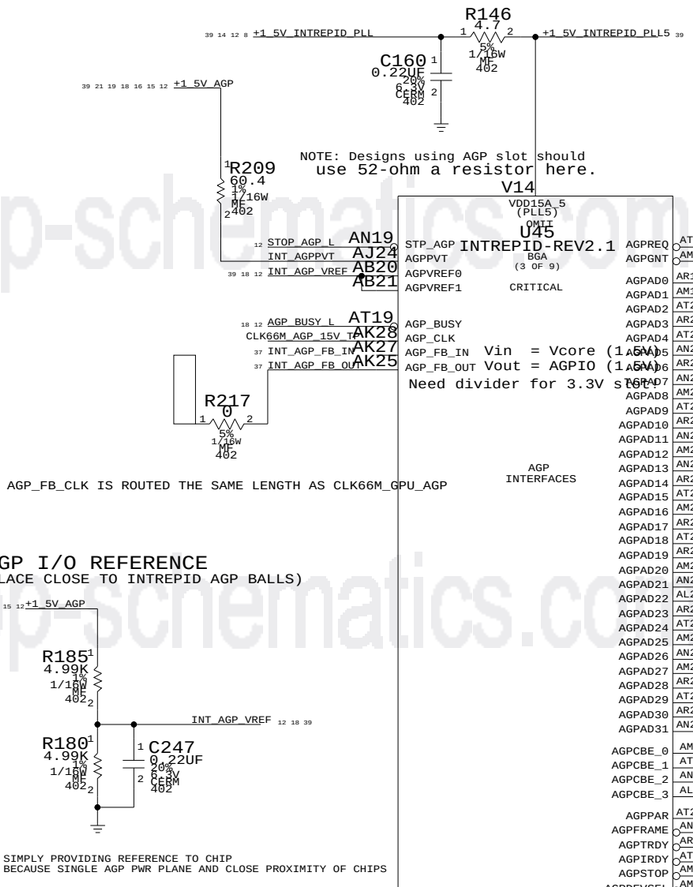
D	051-6694	G
SCALE: NONE	SHT 11 OF 45	

AGP PULL-UPS/PULL DOWNS





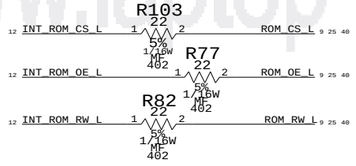


AGP I/O REFERENCE
(PLACE CLOSE TO INTREPID AGP BALLS)

SIMPLY PROVIDING REFERENCE TO CHIP
BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS

PCI PULL-UPS

SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS
PLACE CLOSE TO INTREPID SIDE

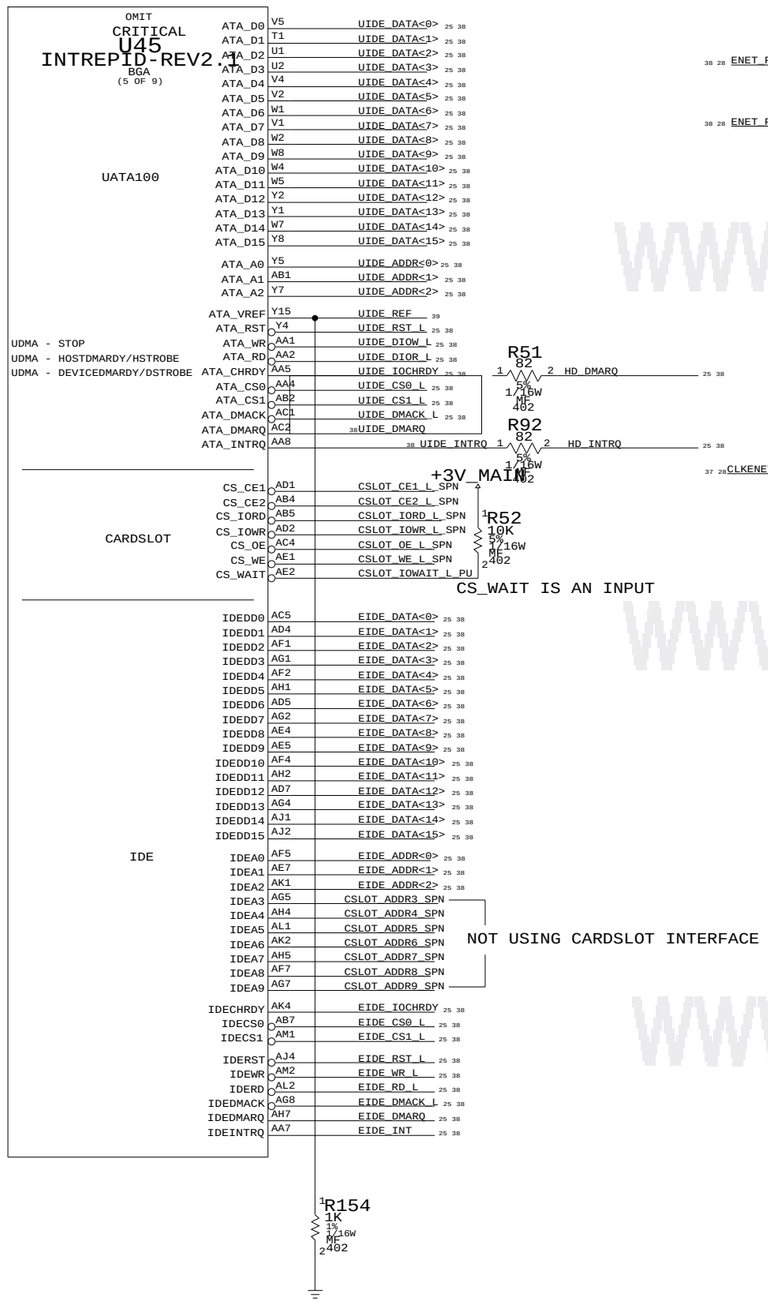


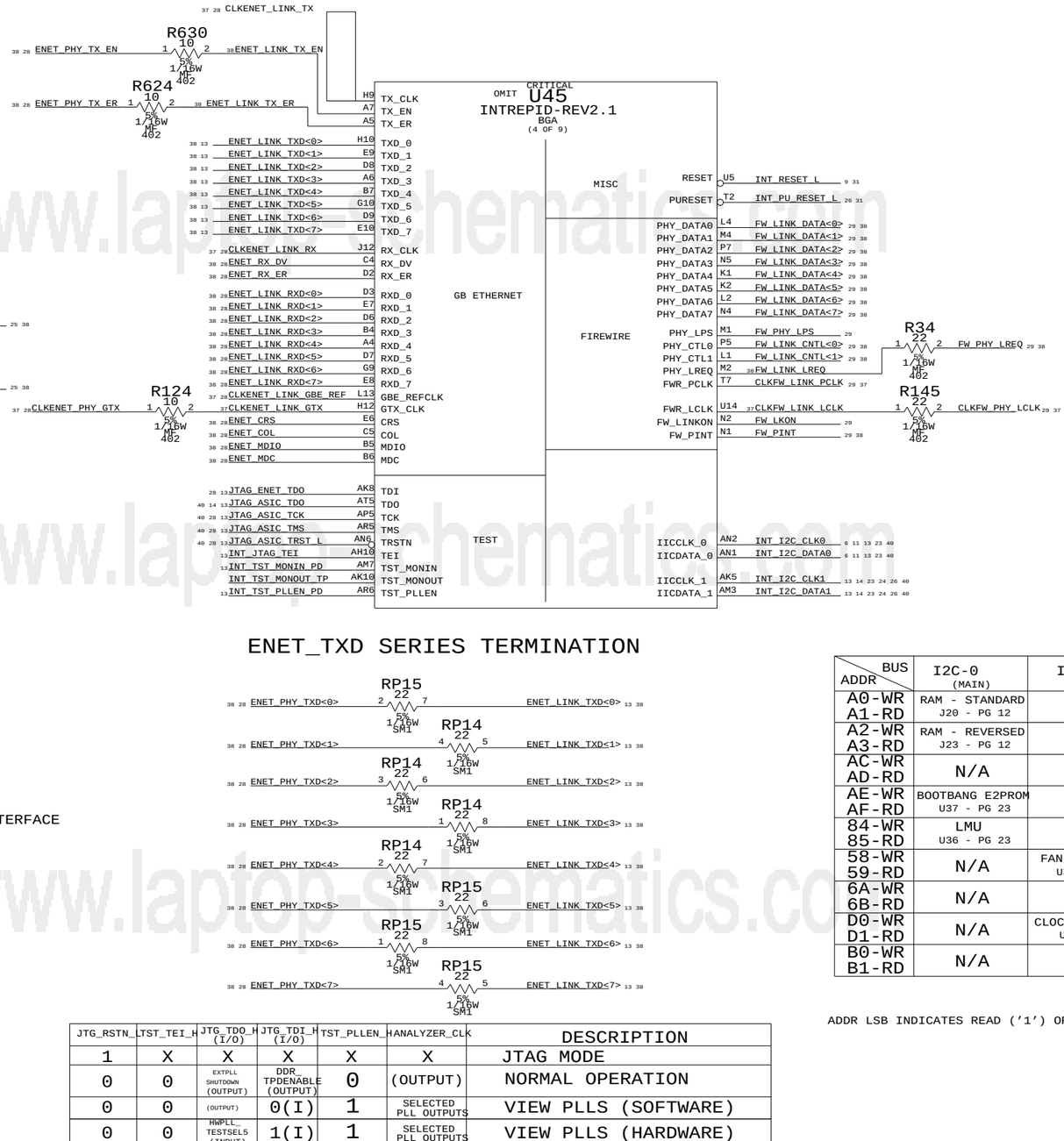
USB2 AND CBUS REQ REMAINS ON
+3V_MAIN BECAUSE THESE CHIPS
ARE POWERED IN SLEEP

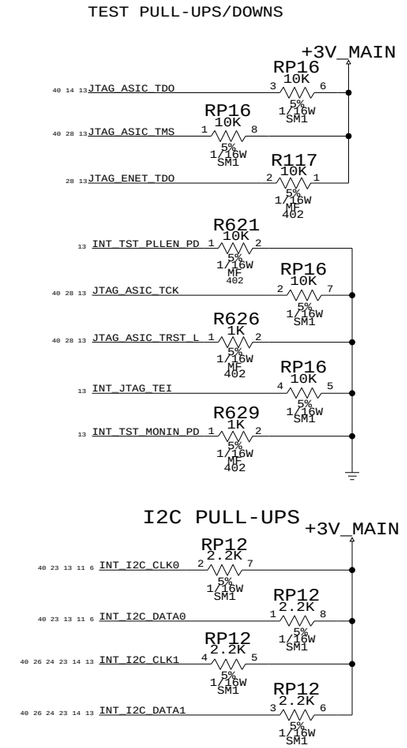
INTREPID AGP/PCI

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 12 OF 45	







ENET_TXD SERIES TERMINATION

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U3 - PG 24	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J12 - PG 24	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A
B0-WR B1-RD	N/A	MMM	N/A	N/A

ADDR LSB INDICATES READ (‘1’) OR WRITE (‘0’) MODES

INT - ENET/FW/UATA EIDE/I2C

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G

SCALE: NONE

SHT 13 OF 45

USB POWER FAULT SIGNALS

USB PORT ASSIGNMENTS

PORT A - RIGHT USB 1

PORT B - UNUSE

PORT C - LEFT USB

PORT D - MODEM

PORT E - BLUETOOTH

PORT F - TPAD

R89,R80 NEED PLACE NEAR TPAD CONNECTOR

PLACE R88 CLOSE TO INTREPID SIDE
OTHERWISE A LOT OF OVERSHOOT/UNDERSHOOT

CRYSTAL LOAD CAPACITANCE IS 16PF

HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
359S0074	359S0086	SSCG	U42	ALT FOR CY28512-2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0090	1	XTAL,CER,LOW PROF,18,432MHZ,8X4.5MM,SMD	Y1	CRITICAL	?

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R100	NO_SSCG

INT - USB/GPIOS/I2S

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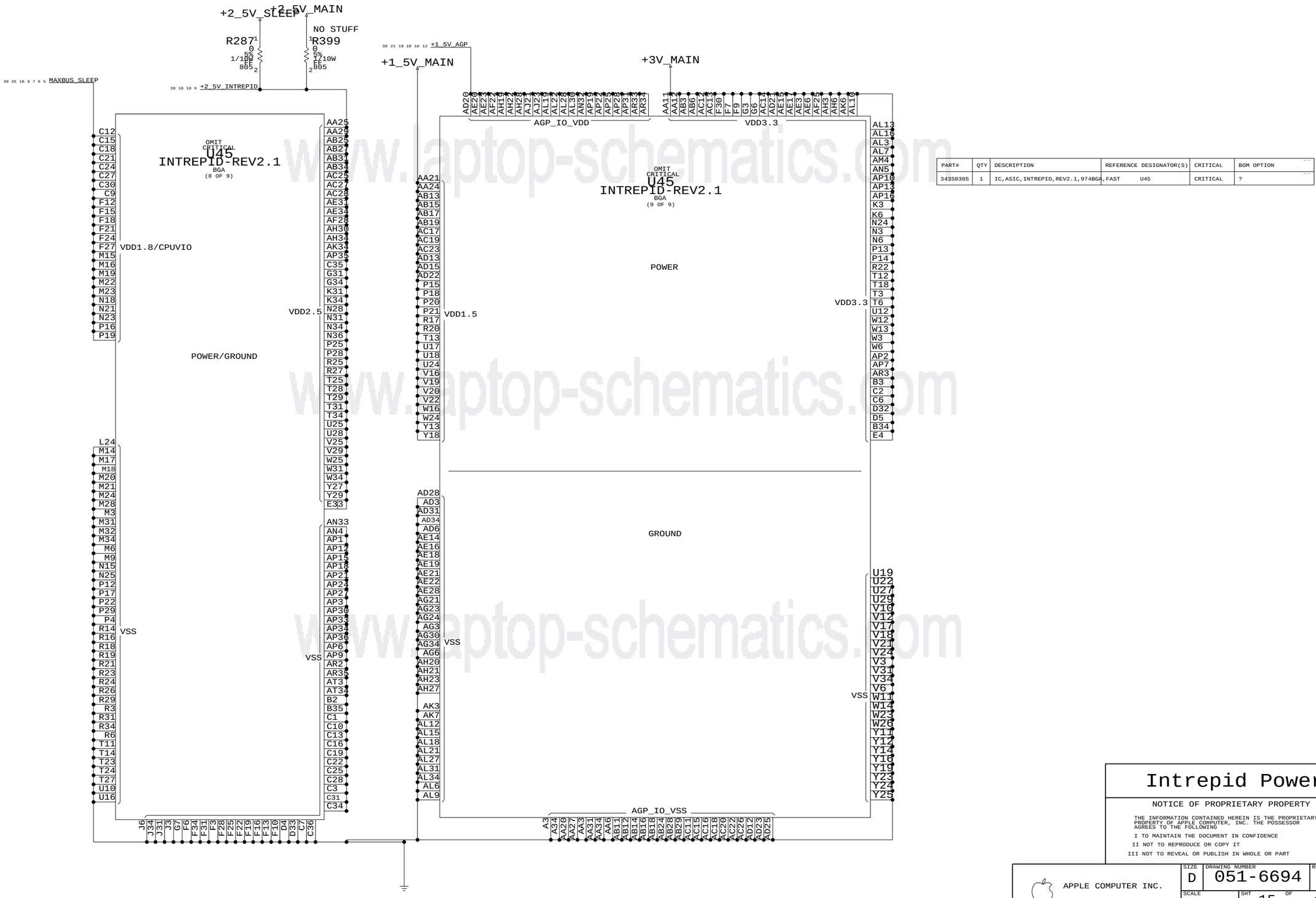
D	051-6694	G
SCALE: NONE	SHT 14 OF 45	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0305	1	IC,ASIC,INTREPID,REV2.1,974BGA,FAST	U45	CRITICAL	?

Intrepid Power

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G

SCALE	SHT	OF
NONE	15	45

INTREPID MAXBUS DECOUPLING

35 15 8 7 6 3 MAXBUS_SLEEP

24 Balls
4 X 10UF (0805)
32 X 0.22UF (0402)

C204 10uF 20% 6.3V CERM 805 2
C348 10uF 20% 6.3V CERM 805 2
C236 10uF 20% 6.3V CERM 805 2
C196 10uF 20% 6.3V CERM 805 2
C239 C240 C350 C312 C176 C288 C313 C94 C286 C158 0.22uF 20% 6.3V CERM 402
C174 C206 C259 C237 C238 C95 C117 C241 C260 C314 0.22uF 20% 6.3V CERM 402
C173 C171 C175 C226 C172 C207 C118 C287 C119 C349 0.22uF 20% 6.3V CERM 402
C205 C209 0.22uF 20% 6.3V CERM 402

INTREPID AGP I/O DECOUPLING

39 21 19 18 15 12 +1_5V_AGP

21 Balls
4 X 10UF (0805)
24 X 0.22UF (0402)

C371 C231 C281 C394 10uF 20% 6.3V CERM 805 2
C356 C297 C268 C217 C355 C267 C250 C298 C377 C216 C228 C230 C265 C378 C357 C229 C325 C393 C324 C323 0.22uF 20% 6.3V CERM 402
C251 C266 C249 0.22uF 20% 6.3V CERM 402

INTREPID DDR DECOUPLING

39 15 10 9 +2_5V_INTREPID

44 Balls
4 X 10UF (0805)
51 X 0.22UF (0402)

C422 C417 C418 C423 10uF 20% 6.3V CERM 805 2
C407 C391 C310 C317 C480 C390 C370 C320 C365 C366 C367 C292 C295 C403 C291 C352 C322 C392 C385 C376 C321 C318 C399 C410 C335 C369 C384 C294 C406 C405 C404 C400 C386 C289 C387 C401 C354 C389 C309 C398 C337 C290 C402 C397 C368 C334 C388 C293 C319 C336 0.22uF 20% 6.3V CERM 402
C316 0.22uF 20% 6.3V CERM 402

INTREPID CORE DECOUPLING

+1_5V_MAIN

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

C128 C101 C157 C315 10uF 20% 6.3V CERM 805 2
C147 C243 C262 C242 C227 C181 C142 C215 C278 C264 C244 C212 C178 C179 C177 C159 C161 C162 C280 C279 C144 C246 C211 C263 C180 C213 C197 C208 C214 0.22uF 20% 6.3V CERM 402

INTREPID 3.3V DECOUPLING

+3V_MAIN

57 Balls
4 X 10UF (0805)
72 X 0.22UF (0402)

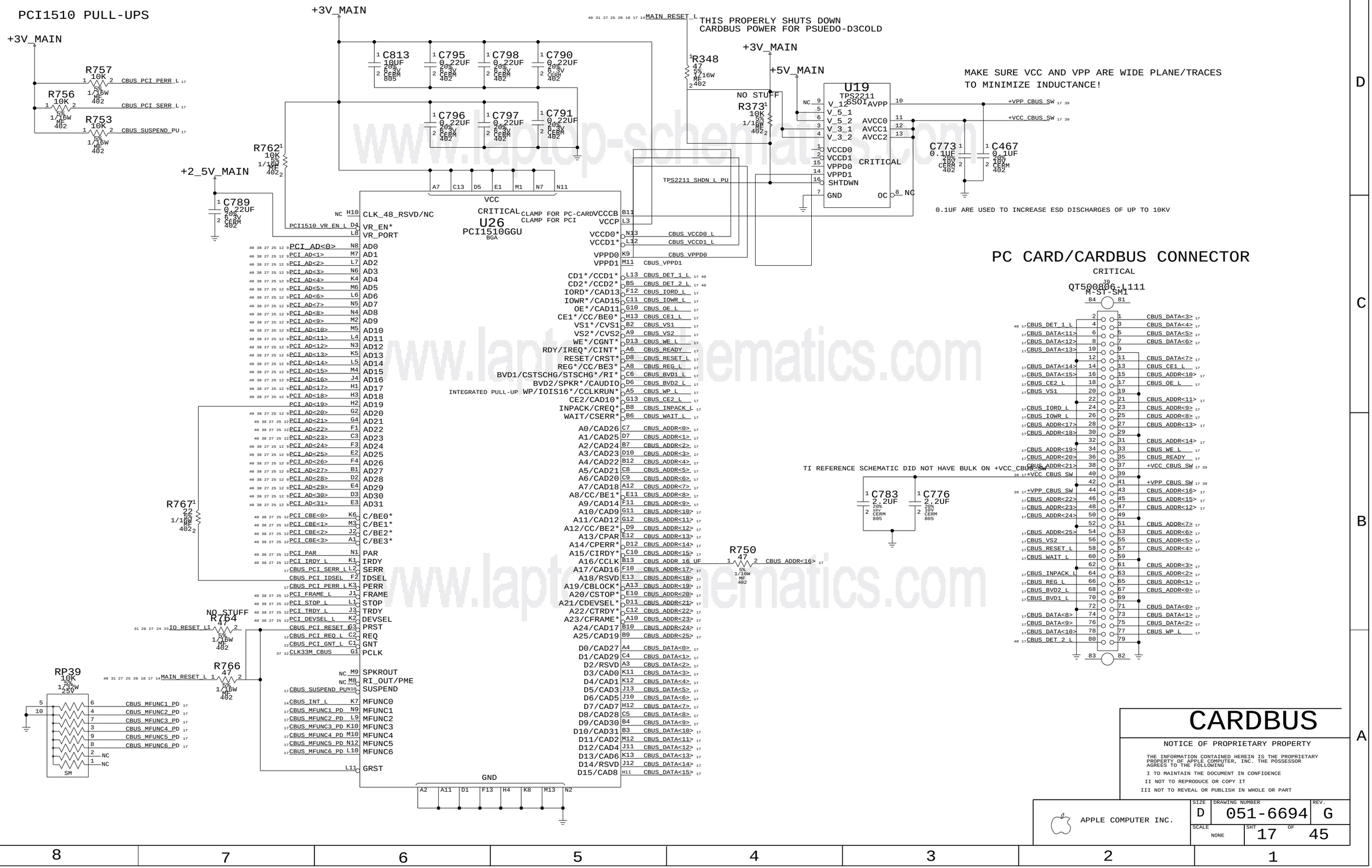
C164 C395 C10 C9 10uF 20% 6.3V CERM 805 2
C375 C351 C53 C42 C21 C185 C31 C143 C123 C121 C33 C184 C43 C35 C261 C60 C52 C199 C57 C19 C16 C108 C55 C32 C125 C45 C76 C277 C28 C26 C34 C23 C120 C146 C141 C30 C145 C96 C54 C50 C75 C122 C51 C59 C163 C126 C98 C109 C56 C27 C296 C248 C210 C58 C22 C20 C61 C44 C29 C24 C183 C18 C49 C36 C17 C99 C396 C124 C127 C100 0.22uF 20% 6.3V CERM 402

Intrepid Decoupling

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G

SCALE	SHT	OF
NONE	16	45



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0214	1	IC,ATI,M11-CSP128,GRPHCTLR,667BGA,HYNIX GDDR	U44	CRITICAL	M11_CSP128

27M OSC

(PLACE THE OSCILLATOR AND R189 AND R195 CLOSE TO ATI PIN AJ29)

+3V_SLEEP — L4 FERR-EMI-100-OHM (SM) — +3V ATI OSC SLEEP

C77 0.1uF 20% 10V CERM 402 — C78 4.7uF 20% 6.3V CERM 805

NO STUFF R188 100K 5% 1/16W MF 402 — CRITICAL — G2 27.0000M OSC SM-1 (VCC, OE, OUT, GND) — ATI OSC OE — ATI CLK27M OSC

(PLACE R200 CLOSE TO OSC) GPU_SS R200 0 5% 1/16W MF 402 — ATI CLK27M OSC SS

R189 287 1% 1/16W MF 402 — ATI CLK27M IN

R195 162 1% 1/16W MF 402

S0=1;S1=M => -1.5% DOWN-SPREAD
SPREAD SPECTRUM SUPPORT

+3V_SLEEP — L3 FERR-EMI-100-OHM (SM) — +3V ATI SS

C70 10uF 20% 6.3V CERM 805 — C71 0.1uF 20% 10V CERM 402

NO STUFF R173 0 5% 1/16W MF 402 — R181 0 5% 1/16W MF 402 — CRITICAL — U47 CY25811 SOI (VDD, XIN/CLKIN, XOUT, NC, NC, FRSEL, CY25811_S1, CY25811_S0, VSS, SSCLK) — ATI CLK27M OSC SS — ATI SSCLK UF — R201 33 5% 1/16W MF 402 — ATI SSCLK IN

NO STUFF R37 0 5% 1/16W MF 402 — NO STUFF R38 0 5% 1/16W MF 402

U44 RAGE MOBILITY M11-CSP64 64MB BGA (1 OF 6)

AGP_AD<31:0> — AD_STB0 N29 — AD_STB1 W29 — AD_STBB0 M28 — AD_STBB1 Y29 — AGP_BUSY# AG28 — AGPREF K30 — AGPTEST K29 — AGP8X_DETB U25 — SUS_STAT# AJ28 — ST0 AF30 — ST1 AF28 — ST2 AE29 — SBA7 AC28 — SBA6 AB29 — SBA5 AC27 — SBA4 AC30 — SBA3 AD27 — SBA2 AD30 — SBA1 AE28 — SBA0 AD29 — RBF# AE30 — STP_AGP# AG29 — SB_STB AC29 — SB_STB# AD28 — RSTB_MSK AD24 — DBI_LO Y25 — DBI_HI Y27

AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0

AGP_CBE<3> W28 — AGP_CBE<2> U29 — AGP_CBE<1> R30 — AGP_CBE<0> N27 — CLK66M_GPU_AGP AG30 — AGP_FRAME_L U27 — AGP_IRDY_L T30 — AGP_TRDY_L T28 — AGP_STOP_L T27 — AGP_DEVSEL_L T29 — AGP_PAR R28 — AGP_REQ_L AF29 — AGP_GNT_L AF27 — AGP_INT_L AH29 — AGP_ATI_RESET AH30 — AGP_WBF_L AE27 — AGP_ATI_VREFG AK3 — AGP_ATI_VREF D8

CBEB3 CBEB2 CBEB1 CBEB0 PCICLK FRAMEB IRDYB TRDYB STOPB DEVSELB PAR REQB GNTB INTAB RSTB WBF VREFG MVREF

C19 P2 B18 P4 A19 R3 A18 R4 D19 P1 G29 G27 B29 C26 C16 A15 C11 — VSS

A10 C5 A3 G4 E2 V4 U2 AB2 AC4 B23 K2 A23 K1 B22 L2 A22 L1 — VSS

AC10 GPU_THERM_DP_TP — AC11 GPU_THERM_DM_TP — E8 +GPU_MEM — J6 (PULL-UP to GPU_MEM_IO) — C8 ATI_MEMTEST — AC22 NC

TEST_YCLK — TEST_MLCK — MEMTEST — PLLTEST

B7 MEMVMODE0 — B6 MEMVMODE1

INT_AGP_VREF — OMIT

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (6 OF 6)

M2 P3 A21 B19 M15 N15 P15 R15 T15 T14 W16 V16 U16 T16 R16 R17 R18 R19 — U6 — AE15 F18 P25 — VDDCI

OMIT — VSS

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (2 OF 6)

B26 A26 B25 A25 C22 D21 C21 D20 C20 D22 C23 D23 A27 B27 — H2 H1 J2 J1 K4 K3 L4 M3 L3 M4 N2 N1 N4 N3 G30 G28 B30 D26 D16 B15 D11 B10 D5 B3 G3 E1 U1 V3 AB1 AC3 J30 J29 H30 H29 F30 F29 E30 E29 J28 J27 H28 H27 F28 F27 E28 E27 D30 B29 C30 C29 A30 A29 A28 B28 D28 C28 D27 C27 D25 C25 D24 C24 D18 C18 — D17 C17 D15 C15 D14 C14 B17 — VSS

A17 B16 A16 B14 A14 B13 A13 D13 C13 D12 C12 D10 C10 D9 — C9 B12 A12 B11 A11 B9 A9 B8 A8 C7 D7 C6 D6 C4 D4 C3 D3 A5 B5 A4 B4 A2 B2 A1 B1 E4 E3 F3 F4 H3 H4 J3 J4 C1 C2 D1 D2 F1 F2 G1 G2 R1 R2 T1 T2 V1 V2 W1 W2 T3 T4 U3 U4 W3 W4 Y3 Y4 Y1 Y2 AA1 AA2 AC1 AC2 AD1 AD2 AA3 AA4 AB3 AB4 AD3 AD4 AE3 AE4 — VSS

OMIT

+3V GPU — R54 10K 5% 1/16W MF 402 — MAIN_RESET_L IS TOGGLED FOR SLEEP — R53 47 5% 1/16W MF 402 — MAIN_RESET_L

+3V GPU — R43 1K 1% 1/16W MF 402 — R44 1K 1% 1/16W MF 402 — +GPU_MEM — R45 1K 1% 1/16W MF 402

PLACE VERF VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN

R46 1K 1% 1/16W MF 402 — C11 0.1uF 20% 10V CERM 402 — C37 10uF 20% 6.3V CERM 805

+1.8V GPU — ATI_MEMIO_LO — R55 4.7K 5% 1/16W MF 402 — ATI_MEMIO_HI — R104 4.7K 5% 1/16W MF 402

ATI_MEMVMODE0 — ATI_MEMVMODE1

ATI_MEMIO_HI — R70 4.7K 5% 1/16W MF 402 — ATI_MEMIO_LO — R105 4.7K 5% 1/16W MF 402

FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V

+3V GPU — R119 47 5% 1/16W MF 402 — R127 10K 5% 1/16W MF 402 — R159 20K 5% 1/16W MF 402

+1.5V AGP — R126 47K 5% 1/16W MF 402 — R138 47K 5% 1/16W MF 402

+3V GPU — R172 20K 5% 1/16W MF 402

R158 0 5% 1/16W MF 402

C62 0.1uF 20% 10V CERM 402 — C63 0.01uF 20% 16V CERM 402 — (PLACE C1002 CLOSE TO AGPREF PIN)

R118 45.3 1% 1/16W MF 402

GPU_VCORE — L2 60-OHM-EMI (SM) — GPU_VCORE_VDDCI

C64 0.01uF 20% 16V CERM 402 — C67 10uF 20% 6.3V CERM 805

C65 0.01uF 20% 16V CERM 402 — C68 0.01uF 20% 16V CERM 402

C66 0.01uF 20% 16V CERM 402 — C69 0.01uF 20% 16V CERM 402

M11 AGP INTERFACE

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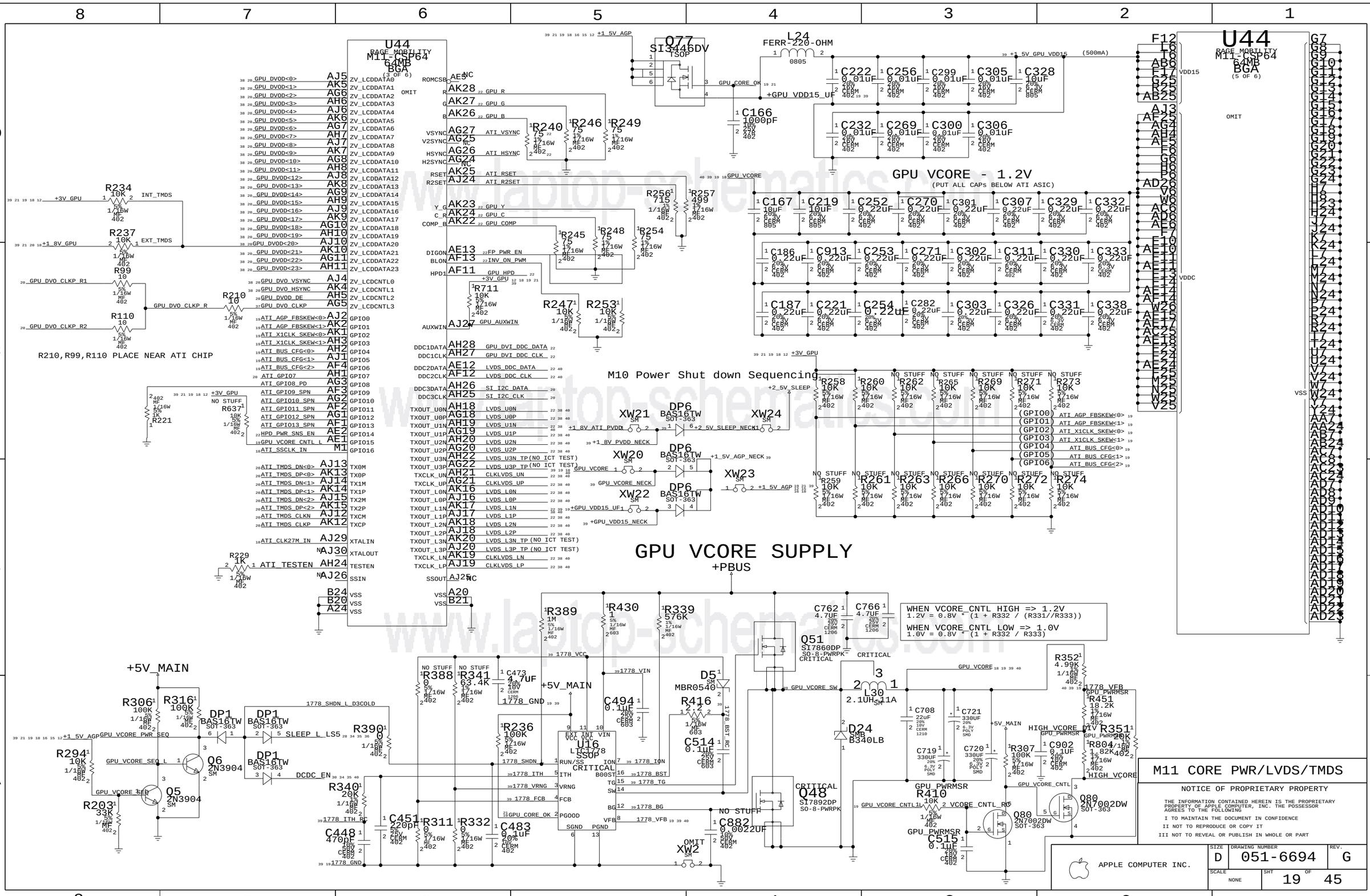
SCALE: NONE	SHT 18 OF 45	


U44
M11-CSP64
64MB
BGA
(3 OF 6)
RAGE MOBILITY
OMIT
GPU_DVOD<0> AJ5
GPU_DVOD<1> AK5
GPU_DVOD<2> AG6
GPU_DVOD<3> AH6
GPU_DVOD<4> AJ6
GPU_DVOD<5> AK6
GPU_DVOD<6> AG7
GPU_DVOD<7> AH7
GPU_DVOD<8> AJ7
GPU_DVOD<9> AK7
GPU_DVOD<10> AG8
GPU_DVOD<11> AH8
GPU_DVOD<12> AJ8
GPU_DVOD<13> AK8
GPU_DVOD<14> AG9
GPU_DVOD<15> AH9
GPU_DVOD<16> AJ9
GPU_DVOD<17> AK9
GPU_DVOD<18> AG10
GPU_DVOD<19> AH10
GPU_DVOD<20> AJ10
GPU_DVOD<21> AK10
GPU_DVOD<22> AG11
GPU_DVOD<23> AH11
GPU_DVO_VSYNC AJ4
GPU_DVO_HSYNC AK4
GPU_DVOD_DE AH5
GPU_DVO_CLKP AG5
ATI_AGP_FBSKEW<0> AJ2
ATI_AGP_FBSKEW<1> AK2
ATI_X1CLK_SKEW<0> AK1
ATI_X1CLK_SKEW<1> AH3
ATI_BUS_CFG<0> AH2
ATI_BUS_CFG<1> AJ1
ATI_BUS_CFG<2> AF4
ATI_GPIO7 AH1
ATI_GPIO8_PD AG3
ATI_GPIO9_SPN AF3
ATI_GPIO10_SPN AG2
ATI_GPIO11_SPN AF2
ATI_GPIO12_SPN AG1
ATI_GPIO13_SPN AF1
HPD_PWR_SNS_EN AE2
GPU_VCORE_CNTL_L AE1
ATI_SSCLK_IN M1
ATI_TMDS_DN<0> AJ13
ATI_TMDS_DP<0> AK13
ATI_TMDS_DN<1> AJ14
ATI_TMDS_DP<1> AK14
ATI_TMDS_DN<2> AJ15
ATI_TMDS_DP<2> AK15
ATI_TMDS_CLKN AJ12
ATI_TMDS_CLKP AK12
ATI_CLK27M_IN AJ29
AJ30
ATI_TESTEN AH24
AJ26
B24
B20
A24
ZV_LCDDATA0
ZV_LCDDATA1
ZV_LCDDATA2
ZV_LCDDATA3
ZV_LCDDATA4
ZV_LCDDATA5
ZV_LCDDATA6
ZV_LCDDATA7
ZV_LCDDATA8
ZV_LCDDATA9
ZV_LCDDATA10
ZV_LCDDATA11
ZV_LCDDATA12
ZV_LCDDATA13
ZV_LCDDATA14
ZV_LCDDATA15
ZV_LCDDATA16
ZV_LCDDATA17
ZV_LCDDATA18
ZV_LCDDATA19
ZV_LCDDATA20
ZV_LCDDATA21
ZV_LCDDATA22
ZV_LCDDATA23
ZV_LCDCNTL0
ZV_LCDCNTL1
ZV_LCDCNTL2
ZV_LCDCNTL3
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
TX0M
TX0P
TX1M
TX1P
TX2M
TX2P
TXCM
TXCP
XTALIN
XTALOUT
TESTEN
SSIN
VSS
VSS
VSS
R234 10K 5% 1/16W MF 402
+3V_GPU
INT_TMDS
R237 10K 5% 1/16W MF 402
+1.8V_GPU
EXT_TMDS
R99 10 5% 1/16W MF 402
GPU_DVO_CLKP_R1
R210 10 5% 1/16W MF 402
GPU_DVO_CLKP_R
R110 10 5% 1/16W MF 402
GPU_DVO_CLKP_R2
R210,R99,R110 PLACE NEAR ATI CHIP
R221 2K 5% 1/16W MF 402
R637 10K 5% 1/16W MF 402
NO STUFF
R229 1K 5% 1/16W MF 402
ROMCSB AE5 NC
R AK28 GPU_R
G AK27 GPU_G
B AK26 GPU_B
VSYNC AG27 ATI_VSYNC
V2SYNC AG25 NC
HSYNC AG26 ATI_HSYNC
H2SYNC AG24 NC
RSET AK25 ATI_RSET
R2SET AJ24 ATI_R2SET
Y_G AK23 GPU_Y
C_R AK24 GPU_C
COMP_B AK22 GPU_COMP
DIGON AE13 FP_PWR_EN
BLON AF13 INV_ON_PWM
HPD1 AF11 GPU_HPD
AUXWIN AJ27 GPU_AUXWIN
DDC1DATA AH28 GPU_DVI_DDC_DATA
DDC1CLK AH27 GPU_DVI_DDC_CLK
DDC2DATA AE12 LVDS_DDC_DATA
DDC2CLK AF12 LVDS_DDC_CLK
DDC3DATA AH26 SI_I2C_DATA
DDC3CLK AH25 SI_I2C_CLK
TXOUT_U0N AH18 LVDS_U0N
TXOUT_U0P AG18 LVDS_U0P
TXOUT_U1N AH19 LVDS_U1N
TXOUT_U1P AG19 LVDS_U1P
TXOUT_U2N AH20 LVDS_U2N
TXOUT_U2P AG20 LVDS_U2P
TXOUT_U3N AH22 LVDS_U3N_TP(NO_ICT_TEST)
TXOUT_U3P AG22 LVDS_U3P_TP(NO_ICT_TEST)
TXCLK_UN AH21 CLKLVDS_UN
TXCLK_UP AG21 CLKLVDS_UP
TXOUT_L0N AK16 LVDS_L0N
TXOUT_L0P AJ16 LVDS_L0P
TXOUT_L1N AK17 LVDS_L1N
TXOUT_L1P AJ17 LVDS_L1P
TXOUT_L2N AK18 LVDS_L2N
TXOUT_L2P AJ18 LVDS_L2P
TXOUT_L3N AK20 LVDS_L3N_TP(NO_ICT_TEST)
TXOUT_L3P AJ20 LVDS_L3P_TP(NO_ICT_TEST)
TXCLK_LN AK19 CLKLVDS_LN
TXCLK_LP AJ19 CLKLVDS_LP
SSOUT AJ25 NC
VSS A20
VSS B21
R240 75 1% 1/16W MF 402
R246 75 1% 1/16W MF 402
R249 75 1% 1/16W MF 402
R245 75 1% 1/16W MF 402
R248 75 1% 1/16W MF 402
R254 75 1% 1/16W MF 402
R256 715 1% 1/16W MF 402
R257 499 1% 1/16W MF 402
R711 10K 5% 1/16W MF 402
R247 10K 5% 1/16W MF 402
R253 10K 5% 1/16W MF 402
Q77
SI3446DV
TSOP
GPU_CORE_OK
+GPU_VDD15_UF
C166 1000pF 10% 25V X7R 402
L24
FERR-220-OHM
0805
+1.5V_GPU_VDD15 (500mA)
C222 0.01uF 20% 16V CERM 402
C256 0.01uF 20% 16V CERM 402
C299 0.01uF 20% 16V CERM 402
C305 0.01uF 20% 16V CERM 402
C328 10uF 20% 6.3V CERM 805
C232 0.01uF 20% 16V CERM 402
C269 0.01uF 20% 16V CERM 402
C300 0.01uF 20% 16V CERM 402
C306 0.01uF 20% 16V CERM 402
GPU VCORE - 1.2V
(PUT ALL CAPS BELOW ATI ASIC)
GPU_VCORE
C167 10uF 20% 6.3V CERM 805
C219 10uF 20% 6.3V CERM 805
C252 0.22uF 20% 6.3V CERM 402
C270 0.22uF 20% 6.3V CERM 402
C301 0.22uF 20% 6.3V CERM 402
C307 0.22uF 20% 6.3V CERM 402
C329 0.22uF 20% 6.3V CERM 402
C332 0.22uF 20% 6.3V CERM 402
C186 0.22uF 20% 6.3V CERM 402
C913 0.22uF 20% 6.3V CERM 402
C253 0.22uF 20% 6.3V CERM 402
C271 0.22uF 20% 6.3V CERM 402
C302 0.22uF 20% 6.3V CERM 402
C311 0.22uF 20% 6.3V CERM 402
C330 0.22uF 20% 6.3V CERM 402
C333 0.22uF 20% 6.3V CERM 402
C187 0.22uF 20% 6.3V CERM 402
C221 0.22uF 20% 6.3V CERM 402
C254 0.22uF 20% 6.3V CERM 402
C282 0.22uF 20% 6.3V CERM 402
C303 0.22uF 20% 6.3V CERM 402
C326 0.22uF 20% 6.3V CERM 402
C331 0.22uF 20% 6.3V CERM 402
C338 0.22uF 20% 6.3V CERM 402
M10 Power Shut down Sequencing
+3V_GPU
+2_5V_SLEEP
R258 10K 5% 1/16W MF 402
R260 10K 5% 1/16W MF 402
R262 10K 5% 1/16W MF 402
R265 10K 5% 1/16W MF 402
R269 10K 5% 1/16W MF 402
R271 10K 5% 1/16W MF 402
R273 10K 5% 1/16W MF 402
NO STUFF
(GPIO0) ATI_AGP_FBSKEW<0>
(GPIO1) ATI_AGP_FBSKEW<1>
(GPIO2) ATI_X1CLK_SKEW<0>
(GPIO3) ATI_X1CLK_SKEW<1>
(GPIO4) ATI_BUS_CFG<0>
(GPIO5) ATI_BUS_CFG<1>
(GPIO6) ATI_BUS_CFG<2>
XW21
XW24
XW20
XW23
XW22
DP6 BAS16TW SOT-363
+1.8V_ATI_PVDD
+1.8V_PVDD_NECK
+2.5V_SLEEP_NECK
GPU_VCORE
GPU_VCORE_NECK
+1.5V_AGP_NECK
+1.5V_AGP
+GPU_VDD15_UF1
+GPU_VDD15_NECK
R259 10K 5% 1/16W MF 402
R261 10K 5% 1/16W MF 402
R263 10K 5% 1/16W MF 402
R266 10K 5% 1/16W MF 402
R270 10K 5% 1/16W MF 402
R272 10K 5% 1/16W MF 402
R274 10K 5% 1/16W MF 402
GPU VCORE SUPPLY
+PBUS
WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R332 / (R331//R333))
WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R332 / R333)
R389 1M 5% 1/16W MF 402
R430 1 5% 1/16W MF 603
R339 576K 1% 1/16W MF 402
C762 4.7UF 20% 25V CERM 1206
C766 4.7UF 20% 25V CERM 1206
Q51
SI7860DP
SO-8-PWRPK
CRITICAL
+5V_MAIN
R306 100K 5% 1/16W MF 402
R316 100K 5% 1/16W MF 402
DP1 BAS16TW SOT-363
+1.5V_AGP
GPU_VCORE_PWR_SEQ
SLEEP_L_LS5
DCDC_EN
Q6 2N3904 SM
Q5 2N3904 SM
R294 10K 5% 1/16W MF 402
R203 33K 5% 1/16W MF 402
R390 0 5% 1/16W MF 402
R340 20K 1% 1/16W MF 402
C451 220pF 5% 25V CERM 402
C448 470pF 10% 50V CERM 402
R311 0 5% 1/16W MF 402
R332 0 5% 1/16W MF 402
C483 0.1uF 10% 16V CERM 402
1778_SHDN_L_D3COLD
1778_GND
1778_ITH_RC
R388 0 5% 1/16W MF 402
R341 63.4K 1% 1/16W MF 402
C473 4.7UF 20% 10V CERM 1206
R236 100K 5% 1/16W MF 402
C494 0.1uF 20% 25V CERM 603
C514 0.1uF 20% 25V CERM 603
R416 2.2 5% 1/16W MF 603
D5 SM MBR0540
L30 2.1UH-11A SM
D24 SMB B340LB
U16
LTC1778
SSOP
CRITICAL
1778_VCC
1778_VIN
1778_ION
1778_BST
1778_TG
1778_BG
1778_VFB
1778_SHDN
1778_ITH
1778_VRNG
1778_FCB
GPU_CORE_OK
1778_BST_RC
R410 10K 5% 1/16W MF 402
GPU_PWRMSR
C515 0.1uF 10% 16V CERM 402
Q80 2N7002DW SOT-363
C882 0.0022UF 10% 50V CERM 402
OMIT
XW2
Q48
SI7892DP
SO-8-PWRPK
CRITICAL
GPU_VCORE_SW
GPU_VCORE_CNTL
VCORE_CNTL_RC
C708 22uF 20% 10V CERM 1210
C719 330UF 20% 6.3V POLY SMD
C721 330UF 20% 6.3V POLY SMD
C720 330UF 20% 6.3V POLY SMD
R307 100K 5% 1/16W MF 402
C902 0.1UF 20% 16V CERM 402
R352 4.99K 1% 1/16W MF 402
R451 18.2K 1% 1/16W MF 402
R804 1.82K 1% 1/16W MF 402
R351 20K 1% 1/16W MF 402
HIGH_VCORE
HIGH VCORE DIV
M11 CORE PWR/LVDS/TMDS
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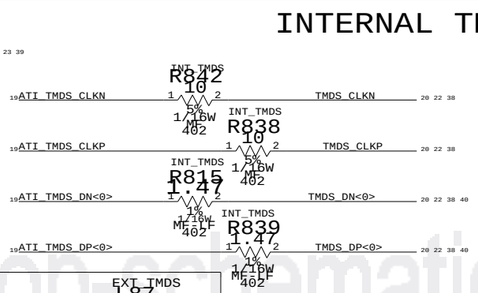
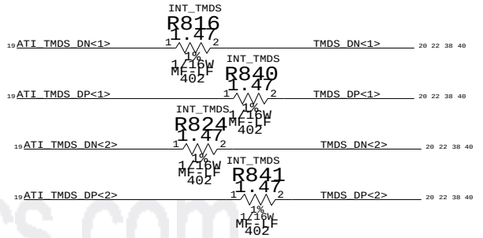
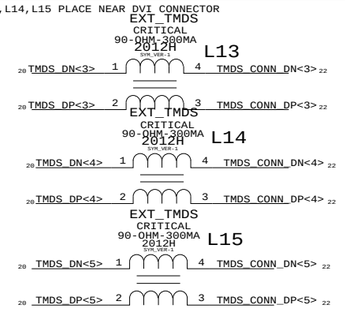
REV. G
SCALE NONE
SHT 19 OF 45

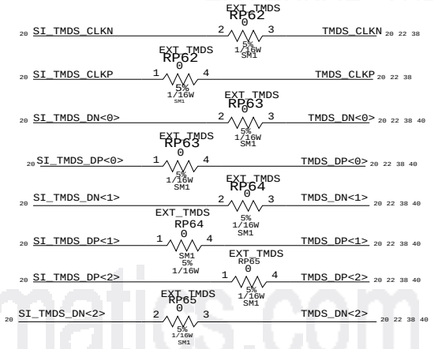
INTERNAL TMDS SERIES TERMINATION

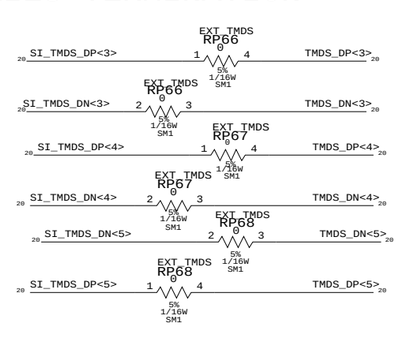




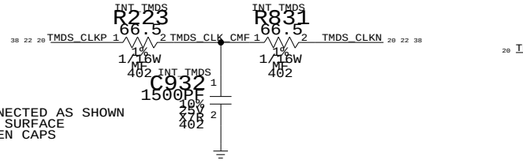


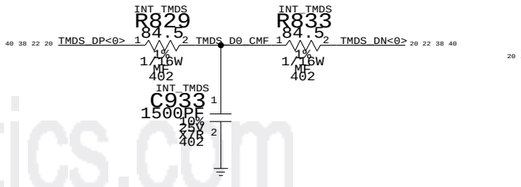
EXTERNAL TMDS SERIES TERMINATION

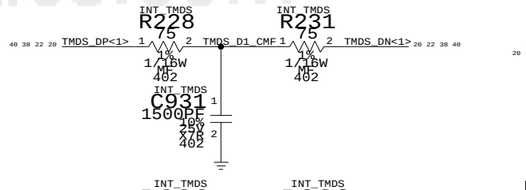


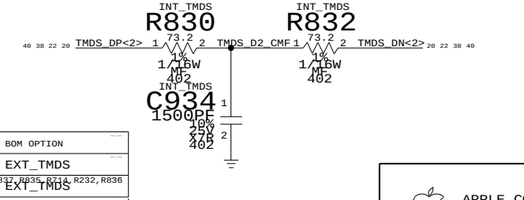


INT/EXT TMDS CLK & D<0:2> TERMINATION

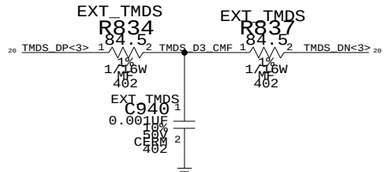


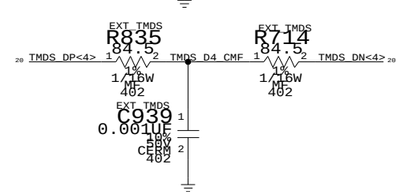


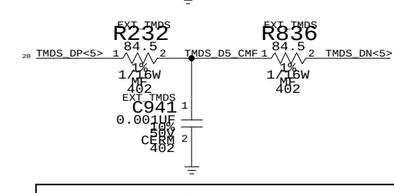




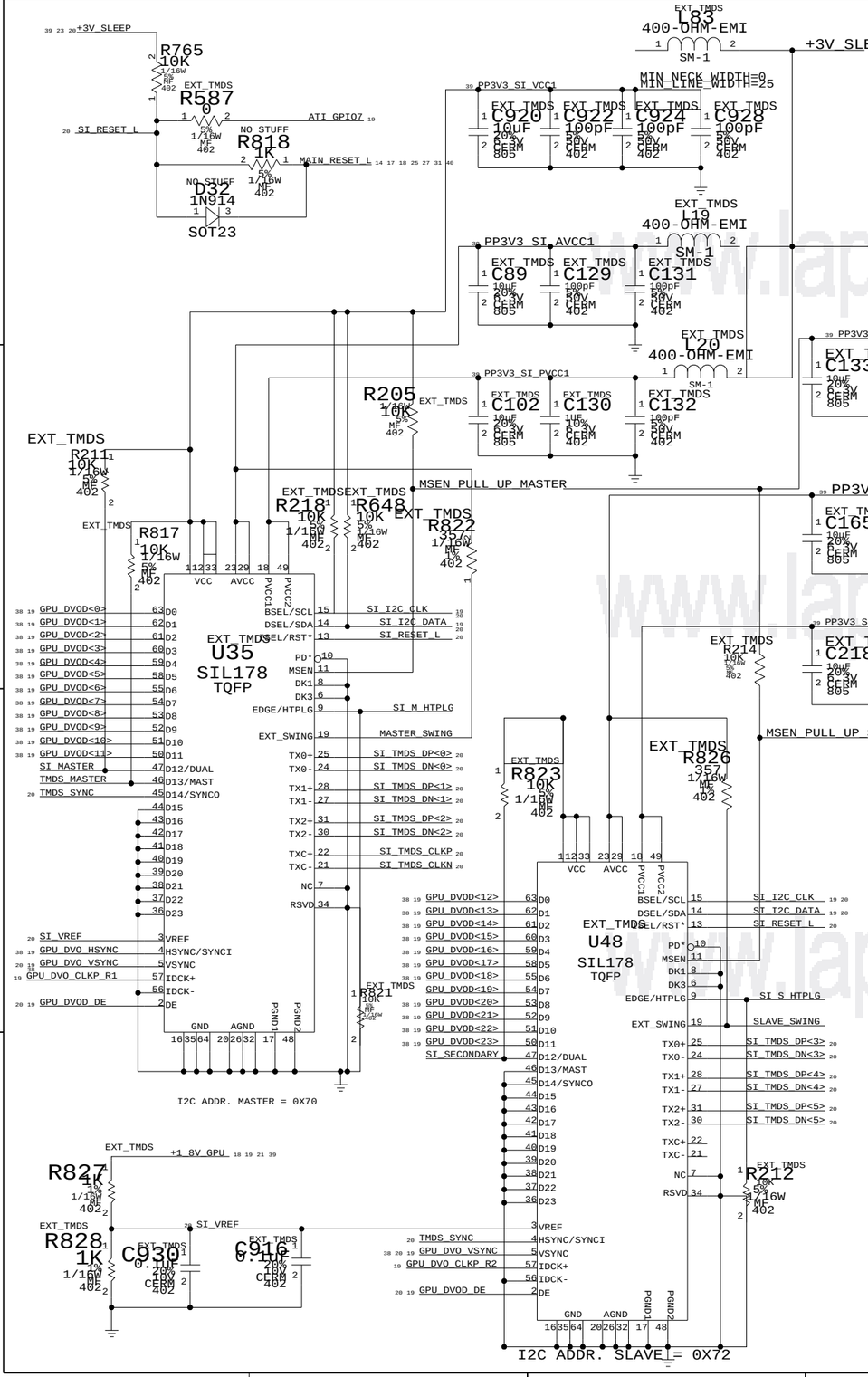
EXT. TMDS D<3:5> TERMINATION







TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS



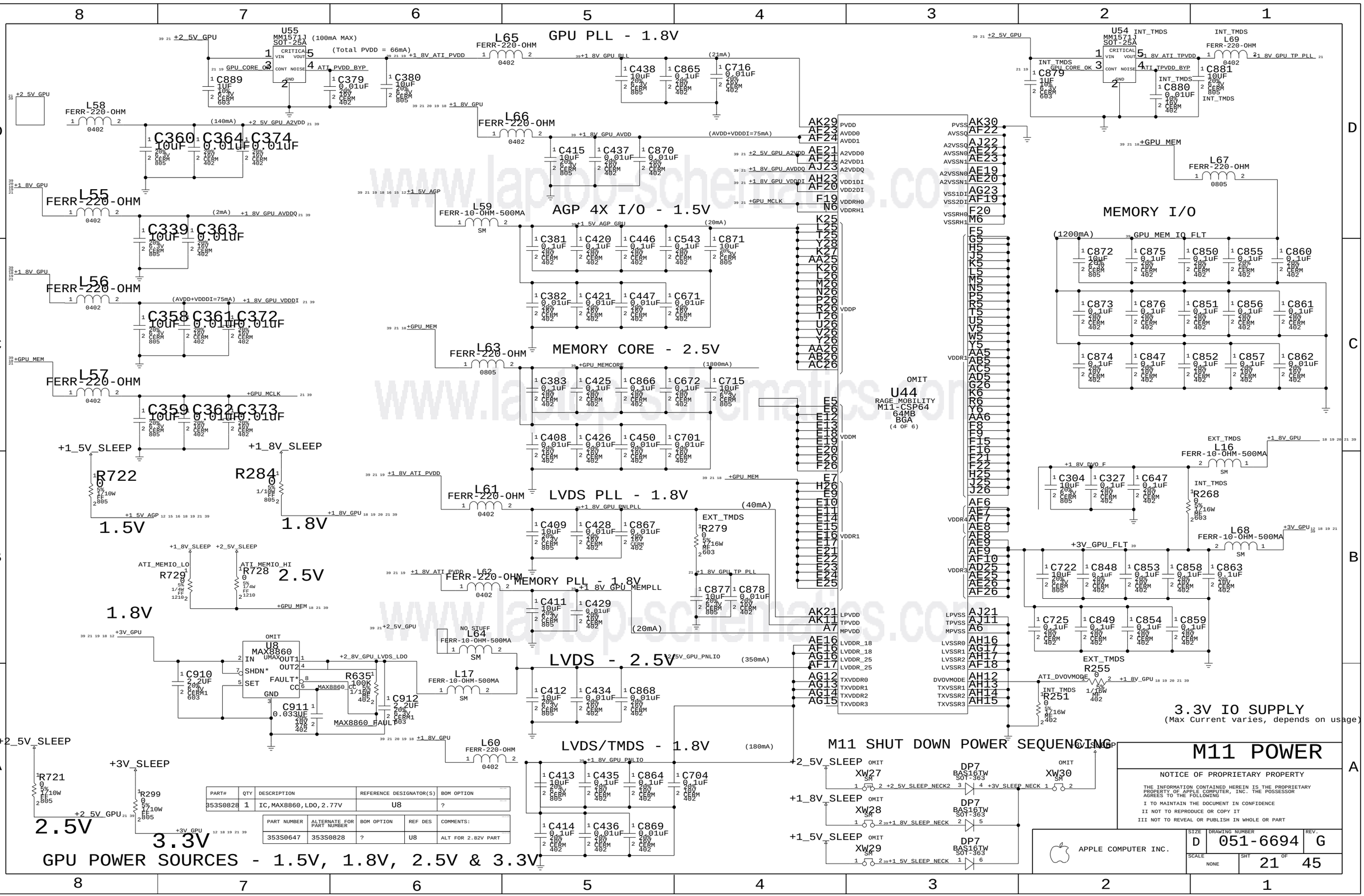
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S7501	2	RES, 75, 1%, 1/16W, 0402	R223,R831	EXT_TMDS
114S8451	12	RES, 84.5, 1%, 1/16W, 0402	R829,R833,R228,R231,R830,R832,R834,R837,R835,R714,R232,R836	EXT_TMDS
132S0045	4	CAP CER .001UF,10%,50V,0402,SMT	C931,C932,C933,C934	EXT_TMDS

INT/EXT TMDS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G

SCALE	SHT	OF
NONE	20	45



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0828	1	IC,MAX8860,LDO,2.77V	U8	?

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0647	353S0828	?	U8	ALT FOR 2.82V PART

EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

FL2 CRITICAL LCFILTER SM-220MHZ — GPU_B → VGA_B
FL1 CRITICAL LCFILTER SM-220MHZ — GPU_G → VGA_G
FL3 CRITICAL LCFILTER SM-220MHZ — GPU_R → VGA_R
C685 3.3PF 0.25% 50V CERM 402
C676 3.3PF 0.25% 50V CERM 402
C684 3.3PF 0.25% 50V CERM 402

+3V_MAIN

CRITICAL 74AHC1G32 SM U56
ATI_HSYNC → R718 33 5% 1/16W MF 402 → VGA_HSYNC_BUF → VGA_HSYNC

CRITICAL 74AHC1G32 SM U57
ATI_VSYNC → R687 33 5% 1/16W MF 402 → VGA_VSYNC_BUF → VGA_VSYNC

VGA VSYNC BUFFERS

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

+5V_SLEEP → F1 0.5AMP-13.2V SM → +5V_DDC_SLEEP_UF → L23 400-OHM-EMI SM-1 → +5V_DDC_SLEEP

Isolation required for DVI power switch

D21 SM MBR0530

DDC_CLK_ISO → R655 4.7K 5% 1/16W MF 402
DDC_DAT_ISO → R654 4.7K 5% 1/16W MF 402

CRITICAL J14 QH1112 F-RT-TH

TMDS_CONN_DN<0>	17	0	TMDS_CONN_DN<2>
TMDS_CONN_DP<0>	18	1	TMDS_CONN_DN<1>
	19	2	TMDS_CONN_DP<2>
TMDS_CONN_DN<5>	20	3	TMDS_CONN_DP<1>
TMDS_CONN_DP<5>	21	4	TMDS_CONN_DN<4>
	22	5	TMDS_CONN_DN<3>
	23	6	TMDS_CONN_DP<4>
TMDS_CONN_CLKP	24	7	TMDS_CONN_DP<3>
TMDS_CONN_CLKN		8	DVI_DDC_CLK_UF
VGA_B		9	(+5V_DDC_SLEEP)
VGA_HSYNC		10	DVI_DDC_DATA_UF
		11	VGA_VSYNC
		12	DVI_HPD_UF
		13	VGA_R
		14	VGA_G
		15	
		16	
	33	17	
	34	18	
	35	19	
	36	20	

C706 100PF 5% 50V CERM 402
C669 100PF 5% 50V CERM 402
C1 100PF 5% 50V CERM 402
C710 0.01UF 20% 50V CERM 603
C3 C5B C4 C1 C5A C2

R649 100 5% 1/16W MF 402
R650 100 5% 1/16W MF 402
R706 0 5% 1/16W MF 402
R1 0 5% 1/16W MF 402

PLACE NEAR 3, 11 & 19
PLACE NEAR C5A & C5B
CHGND1
CHGND5

3V LEVEL_SHIFTERS

+3V_SLEEP

Q38 2N7002DW SOT-363 — DVI_DDC_CLK → GPU_DVI_DDC_CLK
Q38 2N7002DW SOT-363 — DVI_DDC_DATA → GPU_DVI_DDC_DATA
Q35 2N7002DW SOT-363 — DVI_HPD → GPU_HPD

R662 10K 5% 1/16W MF 402
R671 10K 5% 1/16W MF 402
R694 100K 5% 1/16W MF 402

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed ,5V will be driven into DDC_CLK. SINCE POST rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As post rails rise, TP0610 will turn off, as will remote device. Isolation will be disabled as well.

Q40 TP0610 SM — DVI_DDC_CLK_UP → DVI_TURN_ON

R690 0 5% 1/16W MF 402 — DVI_TRUN_ON_ILIM
R688 330 5% 1/16W MF 402 — Pulldown prevents 3904 from turning on when DVI monitor has active self-powered DDC clock pullup.
R691 10K 5% 1/16W MF 402

Q42 2N3904 SM — DVI_TURN_ON_BASE → SOFT_PWR_ON_L

+5V_DDC_SLEEP

Power key detect path when system is running. HPD normally driven to 3.3V. When power key or remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

R680 68.1K 1% 1/16W MF 402
C696 0.1UF 20% 10V CERM 402
HPD_4V_REF

U46 LMC7211 SM CRITICAL — HPD_PWR_SW → HPD_ON

DVI_HPD_UF1 → R663 10K 1% 1/16W MF 402 → DVI_HPD_DIV
R686 10K 1% 1/16W MF 402
R681 100K 1% 1/16W MF 402

Q41 2N7002DW SOT-363 — HPD_ON → R703 330 5% 1/16W MF 402

+PBUS

Q45 TP0610 SM — COMP_ENABLE → HPD_ON_RC → R700 20K 5% 1/16W MF 402 → HPD_BASE → Q44 2N3904 SM

R696 100K 1% 1/16W MF 402
R704 100K 5% 1/16W MF 402
COMP_DISABLE

NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY

HPD_PWR_SNS_EN → Q41 2N7002DW SOT-363
R213 100K 5% 1/16W MF 402
C703 47UF 20% 6.3V CERM 1210
R705 68K 5% 1/16W MF 402

LCD INTERFACE

LVDS INTERFACE

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

+3V_SLEEP
R342 100K 5% 1/16W MF 402
R320 100K 5% 1/16W MF 402
LVDS_DDC_CLK
LVDS_DDC_DATA

C416 0.001UF 20% 50V CERM 402 → CHGND4

CRITICAL J6 G-501973 F-RT-SM

	1	
	2	
+3V_LCD	3	(LVDS DDC POWER)
	4	NC
	5	
	6	
	7	
LVDS_L0N	8	
LVDS_L0P	9	
	10	
LVDS_L1N	11	
LVDS_L1P	12	
	13	
LVDS_L2N	14	
LVDS_L2P	15	
	16	
CLKLVDS_LN	17	
CLKLVDS_LP	18	
	19	
LVDS_U0N	20	
LVDS_U0P	21	
	22	
LVDS_U1N	23	
LVDS_U1P	24	
	25	
LVDS_U2N	26	
LVDS_U2P	27	
	28	
CLKLVDS_UN	29	
CLKLVDS_UP	30	
	33	

NO STUFF
C449 0.001UF 20% 50V CERM 402
C452 0.001UF 20% 50V CERM 402
CHGND4

C500 0.001UF 20% 50V CERM 402 → CHGND4

INVERTER INTERFACE

+PBUS
L33 FERR-1K-OHM-EMI SM — +12_8V_INV
+5V_MAIN
+5V_INV_UF_SW
Q7 FDG6324L SC70-6
L32 400-OHM-EMI SM-1
R317 100K 5% 1/16W MF 402
C440 10UF 20% 25V CERM 805
FP_PWR_EN
Q7 FDG6324L SC70-6
L31 400-OHM-EMI SM-1 — BRIGHT_PWM
+5V_INV_SW
C746 0.001UF 20% 50V CERM 402
C749 0.001UF 20% 50V CERM 402
C739 0.001UF 20% 50V CERM 402
J7 SM-2MT CRITICAL
+3V_PMU
C552 0.1UF 20% 25V CERM 402
INV_ON_PWM → U24 74LVC32 TSSOP 32 → BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL
CHGND2

SHARES LOGIC WITH KB RESET SIGNALS (PG 28)
R724 0 5% 1/16W MF 402
C744 0.01UF 20% 50V CERM 603
CHGND2

TMDS FILTERING PLACE CLOSE TO CONNECTOR

L72 CRITICAL 90-OHM-300MA 2012H SYM_VER-1
TMDS_DN<0> → TMDS_CONN_DN<0>
TMDS_DP<0> → TMDS_CONN_DP<0>

L21 CRITICAL 165-OHM SM SYM_VER-1
TMDS_CLKP → TMDS_CONN_CLKP
TMDS_CLKN → TMDS_CONN_CLKN

L73 CRITICAL 90-OHM-300MA 2012H SYM_VER-1
TMDS_DN<1> → TMDS_CONN_DN<1>
TMDS_DP<1> → TMDS_CONN_DP<1>

L74 CRITICAL 90-OHM-300MA 2012H SYM_VER-1
TMDS_DN<2> → TMDS_CONN_DN<2>
TMDS_DP<2> → TMDS_CONN_DP<2>

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW12 SM — GPU_TV_GND1 → L26 FERR-10-OHM-500MA SM → TV_GND1
L25 3.3UH 0603 — GPU_Y → TV_C
L29 3.3UH 0603 — GPU_C → TV_Y
L27 3.3UH 0603 — GPU_COMP → TV_COMP
XW13 SM — GPU_TV_GND2 → L28 FERR-10-OHM-500MA SM → TV_GND2

C712 0.01UF 20% 50V CERM 603
C702 560PF 10% 50V CERM 402
C707 560PF 10% 50V CERM 402
C718 560PF 10% 50V CERM 402
C724 560PF 10% 50V CERM 402
C714 560PF 10% 50V CERM 402
C713 560PF 10% 50V CERM 402
C717 0.01UF 20% 50V CERM 603

CRITICAL J15 MINIDIN 4T-TH MH1177
CHGND1

Place GND shorts at graphics controller

LCD POWER SWITCHES

+3V_MAIN
R400 100K 5% 1/16W MF 402
C484 2200pF 5% 50V CERM 603
R391 100K 5% 1/16W MF 402
LCD_DIGON_L
LCD_PWREN_L
Q08 2N7002 SM — FP_PWR_EN
SI3443DV TSOP Q11

+3V_LCD_SW
L6 FERR-250-OHM SM
C474 0.001UF 20% 50V CERM 402
CHGND4

VIDEO CONNECTORS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 22 OF 45	

MLB - ALS SENSOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
385-0044	385-0053		PD1	ALT FOR BS520EOF

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0856	353S0504	?	U40	ALT FOR SUPPLY PROBLEM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0091	1	XTAL,CER,LOW PROF,8.000MHZ,8X4.5MM,SMD	Y4	CRITICAL	?

LMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?

SLEEP LED

KEYBOARD PULLUPS

USB Trackpad Connector

Keyboard LED Driver

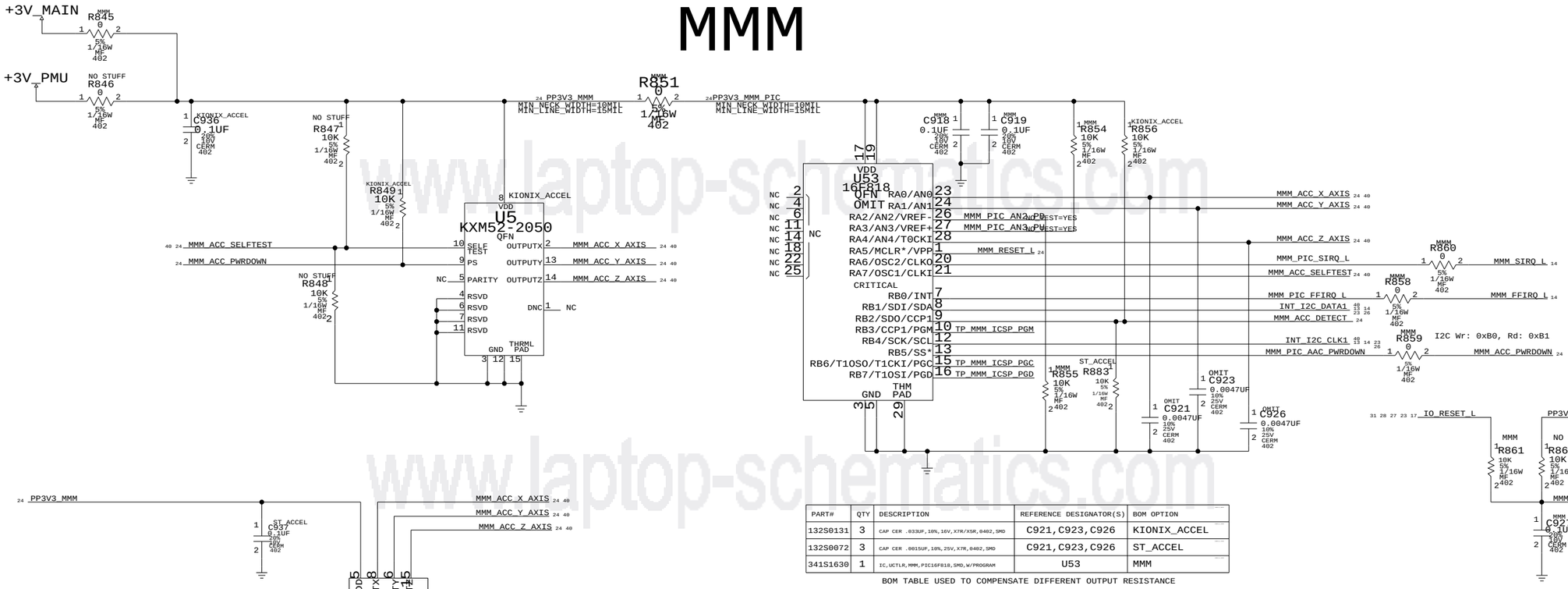
LMU PULL-DOWNS

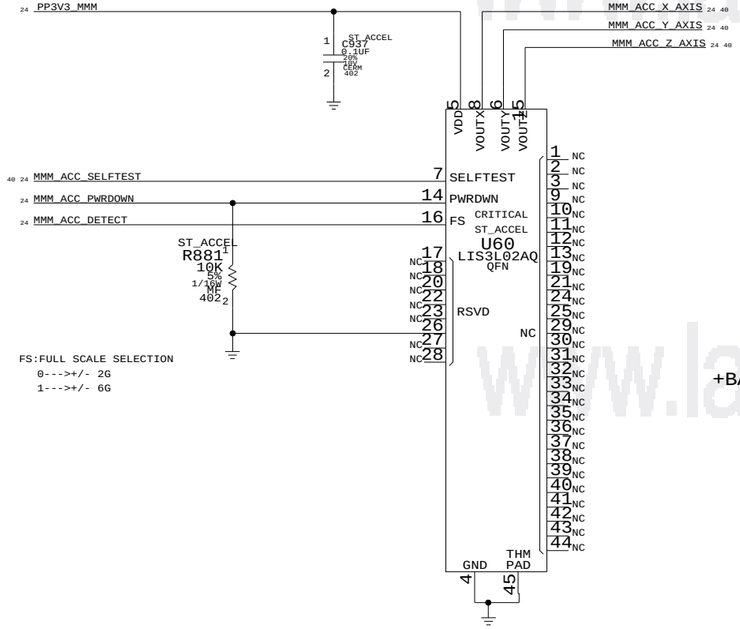
LMU/BOOTBANGER/SPIDEY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 23 OF 45	

MMM

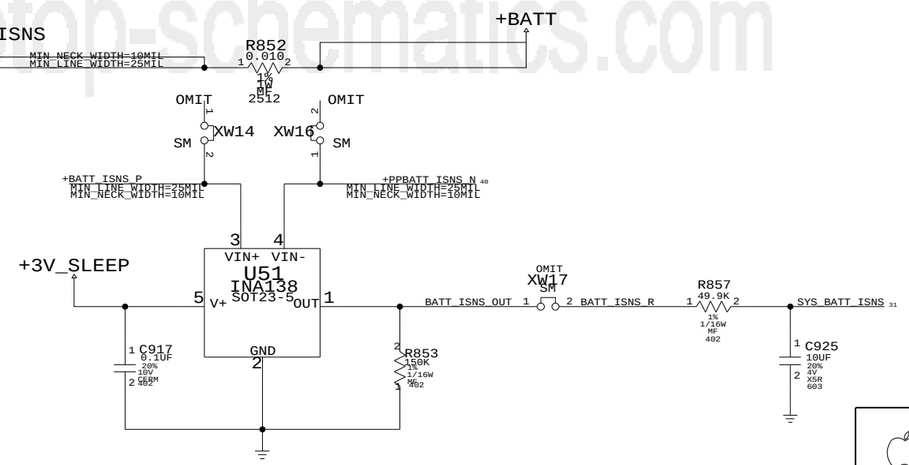




PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0131	3	CAP CER .033UF,10%,16V,X7R/X5R,0402,SMD	C921,C923,C926	KIONIX_ACCEL
132S0072	3	CAP CER .0015UF,10%,25V,X7R,0402,SMD	C921,C923,C926	ST_ACCEL
341S1630	1	IC,UCTLR,MMM,PIC16F818,SMD,W/PROGRAM	U53	MMM

BOM TABLE USED TO COMPENSATE DIFFERENT OUTPUT RESISTANCE

BATTERY CURRENT SENSE



MMM, BATTERY CURRENT SENSE

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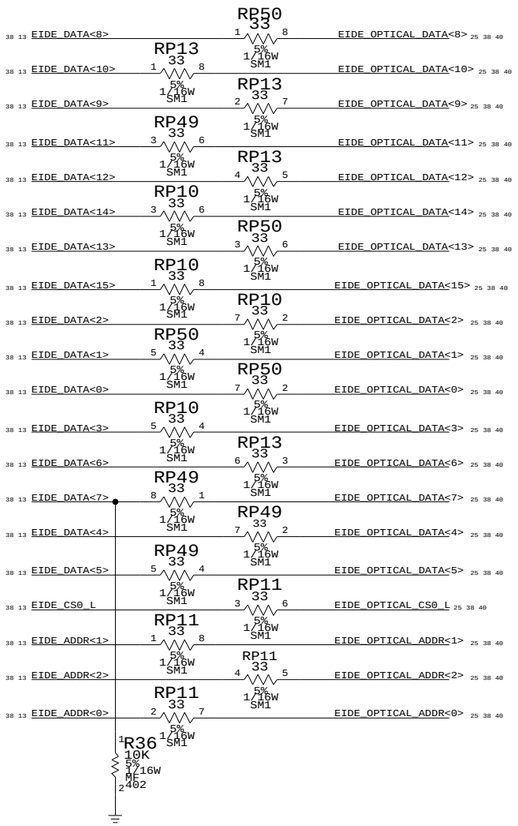
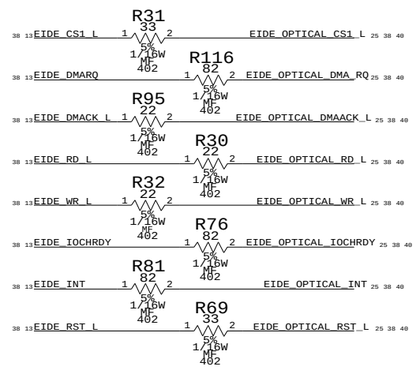
D	051-6694	G
SCALE: NONE	SHT 24 OF 45	

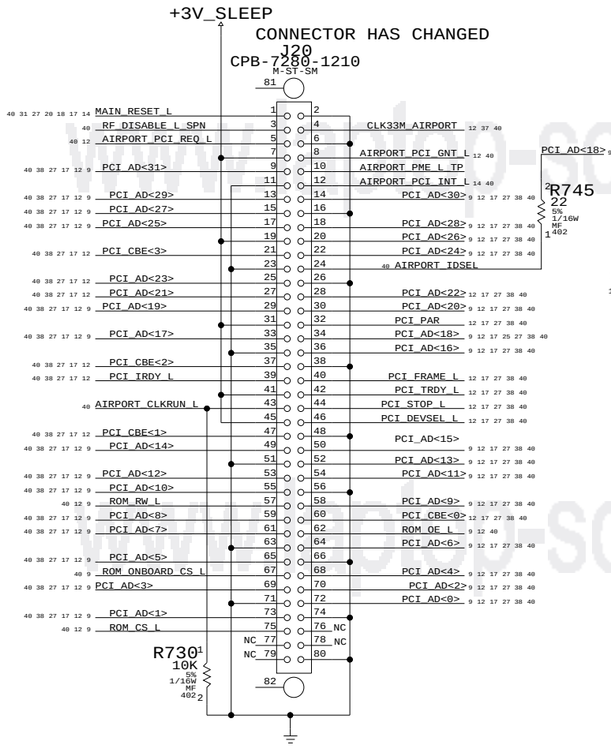
EIDE SERIES TERMINATION

PLACE TERMINATORS NEAR INTREPID

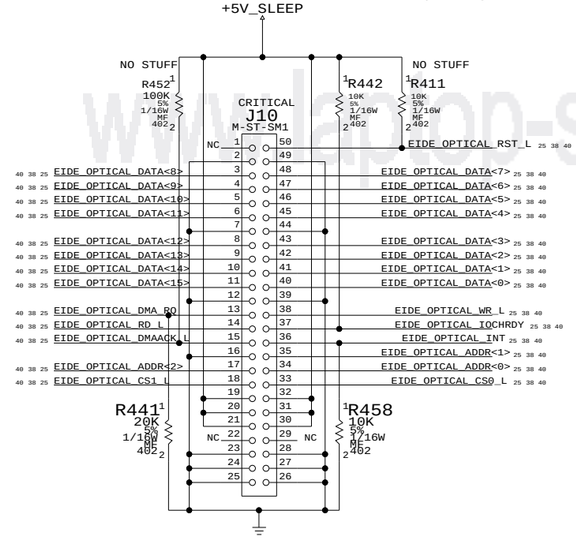




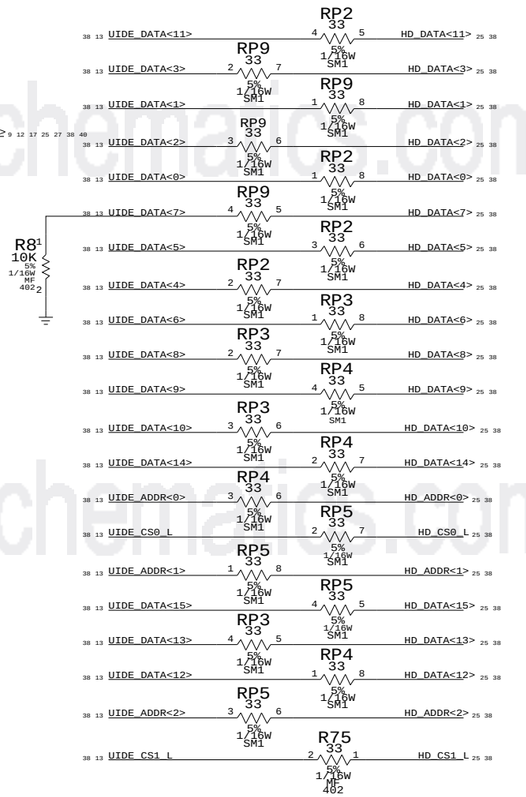
WIRELESS INTERFACE



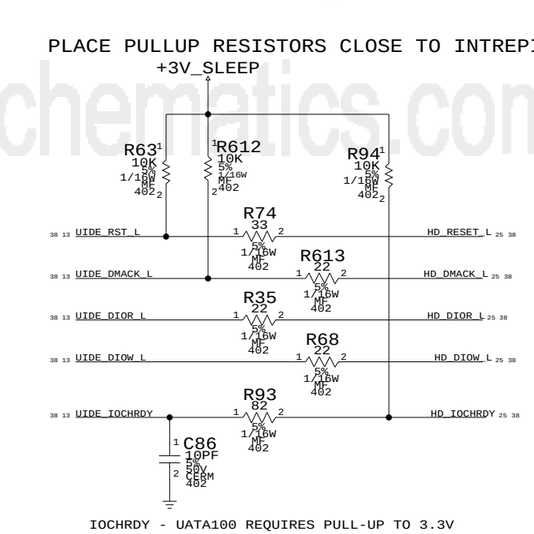
OPTICAL DRIVE INTERFACE (EIDE)



PLACE SERIES R CLOSE TO INTERPID

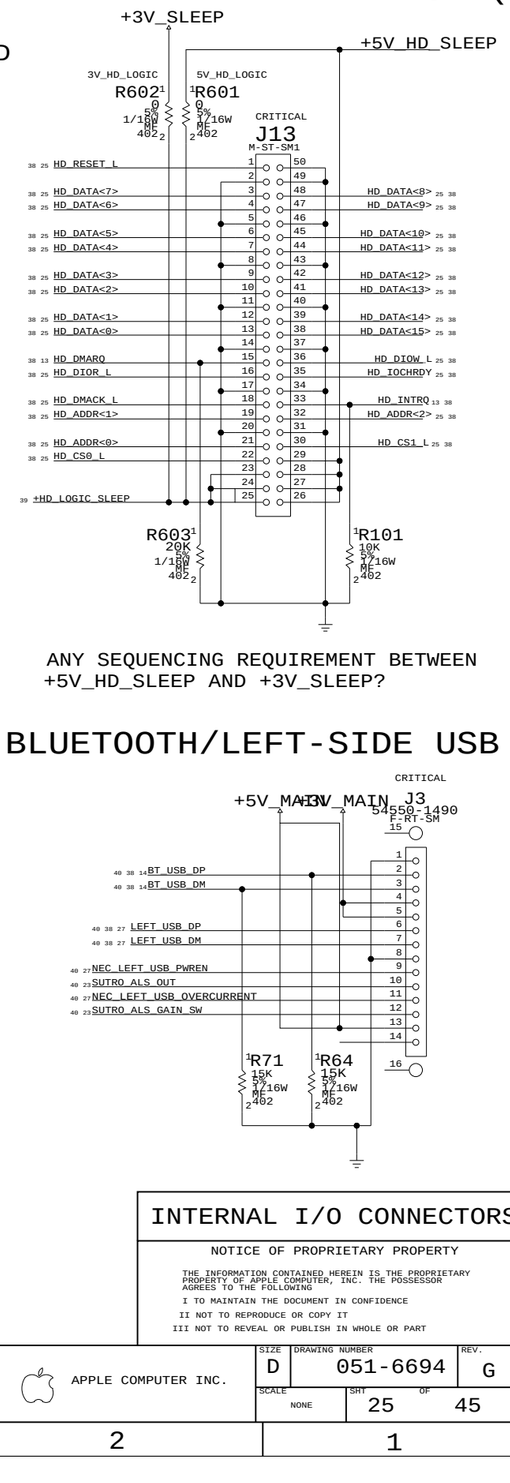


PLACE PULLUP RESISTORS CLOSE TO INTREPID



IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V

HARD DRIVE INTERFACE (UATA100)



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB

INTERNAL I/O CONNECTORS

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SOUND BOARD (SOUSAPHONE)

AUDIO - CRYSTAL SND - INTREPID

Sound Board Connector

Place shorts at 3.3V and 5V regulators

This is an internal board short

This is an internal board short

This is an internal board short

CAPS FOR EMI EXPERIMENTATION ONLY

KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER

KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER

PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE

PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

PLACE CLOSE TO CPU

PLACE UNDERNEATH UPPER RAM

ALTERNATE1

PLACE CLOSE TO BATTERY CHARGER/VCORE

ALTERNATE2

MODEM

SUPPORTS BOTH THE LAST DASH AND Q52 SOFT MODEM

This is an internal board short

DEBUG POWER BUTTON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0608	1	IC,ADT7460,FAN,CTLR,16P,QSOP	U3	ADT7460

FAN CONTROLLER

FAN INTERFACE

THERM ISOLATION

LEFT FAN (CPU)

RIGHT FAN (GPU)

SERIAL DEBUG INTERFACE

DEBUG JUMPERS

FAN/MODEM/SOUND/SLEEP LED/DEBUG

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SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 26 OF 45	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0087	1	XTAL,CER,LW PROF,30.0000MHZ,8X4.5MM,SMD	Y5	CRITICAL	NEC_USB

Y7 LOAD CAPACITANCE IS 16PF

CRITICAL
OMIT
Y5
30.0000M
8X4.5MM-SM

NEC_USB
U39
NEC_UPD720101_USB2
FBGA

Low/Full/High Speed (External)

SERR_L AND PERR_L
HAS DEDICATED PULL-UP
FOR BOTH CBUS AND USB2

Series Rpaks required to
facilitate NAND-tree test

NEED PULL-UP RESISTORS IN CASE USB 1.0 IS USED FOR PORT POWER

PLACE NEAR J3

SUTRO CONNECTOR

PLACE NEAR J12

BUBBA CONNECTOR

INTREPID USB CONSTRAINTS

USB_DAM	USB_DA	5 MIL SPACING	14
USB_DAP	USB_DA	5 MIL SPACING	14
USB_DCM	USB_DC	5 MIL SPACING	14
USB_DCP	USB_DC	5 MIL SPACING	14
USB_D1M	USB_D1	5 MIL SPACING	14 27
USB_D1P	USB_D1	5 MIL SPACING	14 27
USB_D2M	USB_D2	5 MIL SPACING	
USB_D2P	USB_D2	5 MIL SPACING	

USB 2.0

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 27 OF 45	

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0079	338S0223	?	U49	ALT FOR 88E1111-BDIE

PLACE ALL SERIES RES CLOSE TO PHY

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

PUT CRYSTAL CIRCUIT CLOSE TO PHY

Y3'S LOAD CAPACITANCE IS 20PF

VOUT = 0.8V*(1+R2EQV/R1)
R2EQV = R2A||R2B

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

PLACE RESISTORS CLOSE TO PHY

SEE CONFIG TABLES (BELOW)

PLACE CAPS AT TRANSFORMER PINS 1, 4, 7 & 10

PLACE CLOSE TO ETHERNET CONNECTOR

Short shielded RJ-45

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0086	1	XTAL,CER,25MHZ,.005%,20PF,8X4.5MM,SMD	Y3	CRITICAL	?

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111 10/100/1000 ETHERNET

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 28 OF 45	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052	?	G1	SIWARD ALT FOR FW OSC

DSX STRAP OPTIONS

0 -> BILINGUAL PORT

1 -> A-ONLY PORT

PLACE NEAR PHY

PLACE NEAR PHY

CAPACITOR IN CONJUCTION WITH INTERNAL PULLUP PROVIDES RESET PULSE WHEN PHY FIRST RECEIVES POWER

VOUT = 1.22*(1+R2/R1)+ IADJ*R2

IADJ = 30NA AT 25C

PWR CLASS = 100

(MAY PROVIDE POWER, OR MAY REQUIRE UP TO 3W)

(PC0 IS MSB, PC2 IS LSB)

1MA(MAX) BUS HOLDER EACH

FIREWIRE

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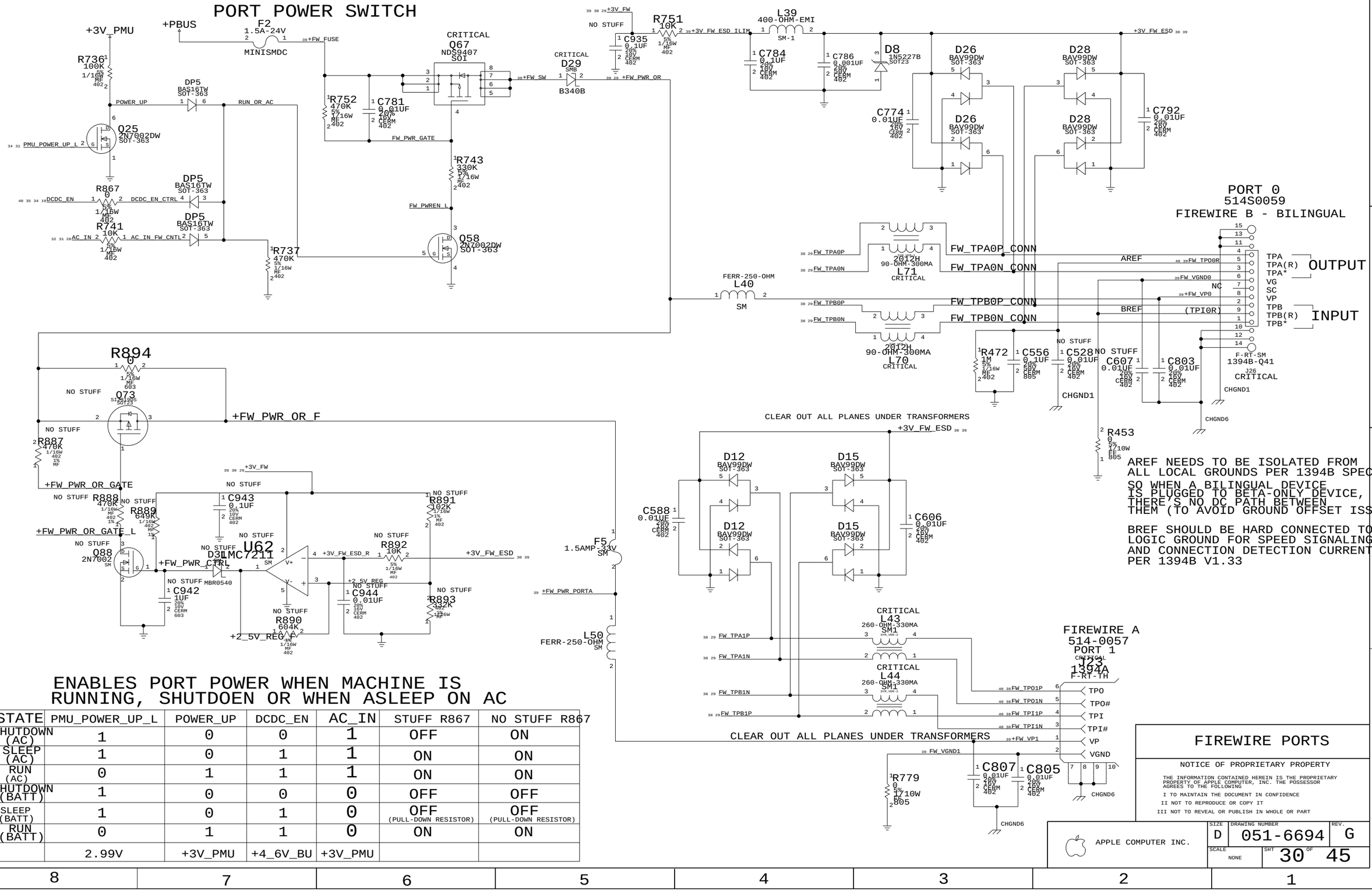
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 29 OF 45	

PORT POWER SWITCH



ENABLES PORT POWER WHEN MACHINE IS RUNNING, SHUTDOEN OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	STUFF R867	NO STUFF R867
SHUTDOWN (AC)	1	0	0	1	OFF	ON
SLEEP (AC)	1	0	1	1	ON	ON
RUN (AC)	0	1	1	1	ON	ON
SHUTDOWN (BATT)	1	0	0	0	OFF	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU		

FIREWIRE PORTS

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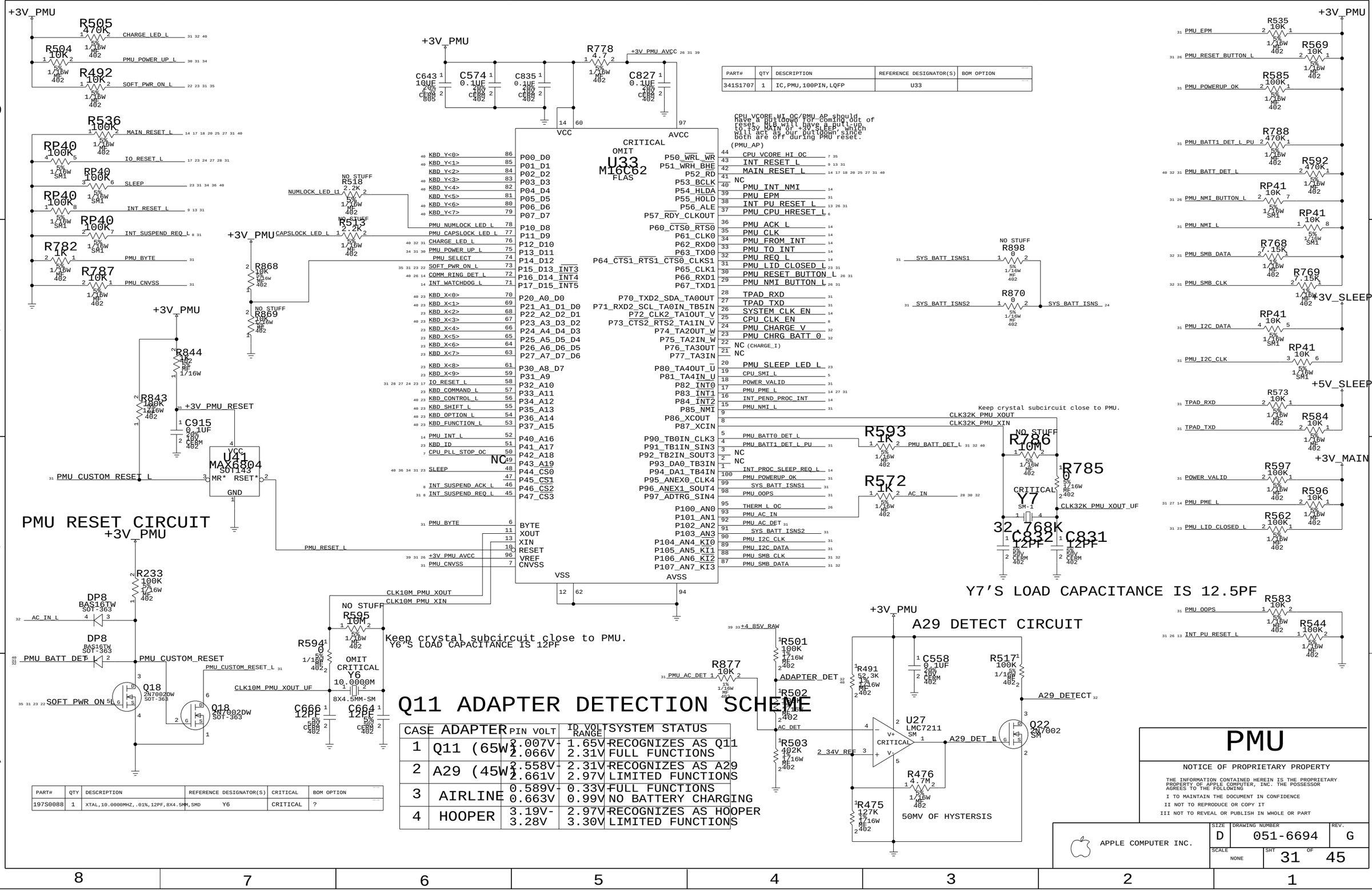
+3V_PMU
R505 470K CHARGE_LED_L
R504 10K PMU_POWER_UP_L
R492 10K SOFT_PWR_ON_L
R536 100K MAIN_RESET_L
RP40 100K IO_RESET_L
RP40 100K SLEEP
RP40 100K INT_RESET_L
RP40 100K INT_SUSPEND_REQ_L
R782 1K PMU_BYTE
R787 10K PMU_CNVSS
+3V_PMU
R844 10K
R843 100K
+3V_PMU_RESET
C915 0.1UF
U41 MAX6804 SOT143
MR* RSET*
GND
PMU_CUSTOM_RESET_L
PMU RESET CIRCUIT
+3V_PMU
R233 100K
DP8 BAS16TW SOT-363
AC_IN_L
DP8 BAS16TW SOT-363
PMU_BATT_DET
PMU_CUSTOM_RESET
Q18 2N7002DW SOT-363
SOFT_PWR_ON_L
Q18 2N7002DW SOT-363
+3V_PMU
C643 10UF 20% 6.3V CERM 805
C574 0.1UF 20% 16V CERM 402
C835 0.1UF 20% 16V CERM 402
R778 4.7
+3V_PMU_AVCC
C827 0.1UF 20% 16V CERM 402
VCC
AVCC
VSS
CRITICAL
OMIT
U33 M16C62 FLAS
P00_D0
P01_D1
P02_D2
P03_D3
P04_D4
P05_D5
P06_D6
P07_D7
P10_D8
P11_D9
P12_D10
P13_D11
P14_D12
P15_D13_INT3
P16_D14_INT4
P17_D15_INT5
P20_A0_D0
P21_A1_D1_D0
P22_A2_D2_D1
P23_A3_D3_D2
P24_A4_D4_D3
P25_A5_D5_D4
P26_A6_D6_D5
P27_A7_D7_D6
P30_A8_D7
P31_A9
P32_A10
P33_A11
P34_A12
P35_A13
P36_A14
P37_A15
P40_A16
P41_A17
P42_A18
P43_A19
P44_CS0
P45_CS1
P46_CS2
P47_CS3
BYTE
XOUT
XIN
RESET
VREF
CNVSS
P50_WRL_WR
P51_WRH_BHE
P52_RD
P53_BCLK
P54_HLDA
P55_HOLD
P56_ALE
P57_RDY_CLKOUT
P60_CTS0_RTS0
P61_CLK0
P62_RXD0
P63_TXD0
P64_CTS1_RTS1_CTS0_CLKS1
P65_CLK1
P66_RXD1
P67_TXD1
P70_TXD2_SDA_TA0OUT
P71_RXD2_SCL_TA0IN_TB5IN
P72_CLK2_TA1OUT_V
P73_CTS2_RTS2_TA1IN_V
P74_TA2OUT_W
P75_TA2IN_W
P76_TA3OUT
P77_TA3IN
P80_TA4OUT_U
P81_TA4IN_U
P82_INT0
P83_INT1
P84_INT2
P85_NMI
P86_XCOUT
P87_XCIN
P90_TB0IN_CLK3
P91_TB1IN_SIN3
P92_TB2IN_SOUT3
P93_DA0_TB3IN
P94_DA1_TB4IN
P95_ANEX0_CLK4
P96_ANEX1_SOUT4
P97_ADTRG_SIN4
P100_AN0
P101_AN1
P102_AN2
P103_AN3
P104_AN4_KI0
P105_AN5_KI1
P106_AN6_KI2
P107_AN7_KI3
AVSS
CPU_VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. MCU will have a pullup to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.
(PMU_AP)
CPU_VCORE_HI_OC
INT_RESET_L
MAIN_RESET_L
PMU_INT_NMI
PMU_EPM
INT_PU_RESET_L
PMU_CPU_HRESET_L
PMU_ACK_L
PMU_CLK
PMU_FROM_INT
PMU_TO_INT
PMU_REQ_L
PMU_LID_CLOSED_L
PMU_RESET_BUTTON_L
PMU_NMI_BUTTON_L
TPAD_RXD
TPAD_TXD
SYSTEM_CLK_EN
CPU_CLK_EN
PMU_CHARGE_V
PMU_CHRG_BATT_0
NC (CHARGE_I)
NC
PMU_SLEEP_LED_L
CPU_SMI_L
POWER_VALID
PMU_PME_L
INT_PEND_PROC_INT
PMU_NMI_L
PMU_BATT0_DET_L
PMU_BATT1_DET_L_PU
NC
NC
INT_PROC_SLEEP_REQ_L
PMU_POWERUP_OK
SYS_BATT_ISNS1
PMU_OOPS
THERM_L_OC
PMU_AC_IN
PMU_AC_DET
SYS_BATT_ISNS2
PMU_I2C_CLK
PMU_I2C_DATA
PMU_SMB_CLK
PMU_SMB_DATA
NUMLOCK_LED_L
CAPSLOCK_LED_L
CHARGE_LED_L
PMU_POWER_UP_L
PMU_SELECT
SOFT_PWR_ON_L
COMM_RING_DET_L
INT_WATCHDOG_L
KBD_X<0>
KBD_X<1>
KBD_X<2>
KBD_X<3>
KBD_X<4>
KBD_X<5>
KBD_X<6>
KBD_X<7>
KBD_X<8>
KBD_X<9>
IO_RESET_L
KBD_COMMAND_L
KBD_CONTROL_L
KBD_SHIFT_L
KBD_OPTION_L
KBD_FUNCTION_L
PMU_INT_L
KBD_ID
CPU_PLL_STOP_OC
SLEEP
INT_SUSPEND_ACK_L
INT_SUSPEND_REQ_L
PMU_BYTE
+3V_PMU_AVCC
PMU_CNVSS
NO STUFF R518 2.2K
NO STUFF R513 2.2K
R868 10K
NO STUFF R869 10K
CLK10M_PMU_XOUT
CLK10M_PMU_XIN
NO STUFF R595 10M
R594 0
OMIT CRITICAL Y6 10.0000M 8X4.5MM-SM
C666 12PF
C664 12PF
CLK10M_PMU_XOUT_UF
Keep crystal subcircuit close to PMU.
Y6'S LOAD CAPACITANCE IS 12PF
Keep crystal subcircuit close to PMU.
CLK32K_PMU_XOUT
CLK32K_PMU_XIN
R593 1K
R572 1K
PMU_BATT_DET_L
AC_IN
NO STUFF R786 10M
R785 0
CRITICAL Y7 SM-1 32.768K
CLK32K_PMU_XOUT_UF
C832 12PF
C831 12PF
Y7'S LOAD CAPACITANCE IS 12.5PF
+4.85V_RAW
R877 10K
PMU_AC_DET
R501 100K
ADAPTER_DET
R502 100K
R503 402K
2.34V_REF
A29 DETECT CIRCUIT
+3V_PMU
R491 52.3K
C558 0.1UF
R517 100K
U27 LMC7211 SM
CRITICAL
A29_DETECT
A29_DET_L
Q22 2N7002 SM
R476 4.7M
R475 127K
50MV OF HYSTERSIS
NO STUFF R898 0
NO STUFF R870 0
SYS_BATT_ISNS1
SYS_BATT_ISNS2
SYS_BATT_ISNS
+3V_PMU
R535 10K PMU_EPM
R569 10K PMU_RESET_BUTTON_L
R585 100K PMU_POWERUP_OK
R788 470K PMU_BATT1_DET_L_PU
R592 470K PMU_BATT_DET_L
RP41 10K PMU_NMI_BUTTON_L
RP41 10K PMU_NMI_L
R768 7.15K PMU_SMB_DATA
R769 7.15K PMU_SMB_CLK
+3V_SLEEP
RP41 10K PMU_I2C_DATA
RP41 10K PMU_I2C_CLK
+5V_SLEEP
R573 10K TPAD_RXD
R584 10K TPAD_TXD
+3V_MAIN
R597 100K POWER_VALID
R596 10K PMU_PME_L
R562 100K PMU_LID_CLOSED_L
R583 10K PMU_OOPS
R544 100K INT_PU_RESET_L
Q11 ADAPTER DETECTION SCHEME
CASE ADAPTER PIN VOLT ID VOLT RANGE SYSTEM STATUS
1 Q11 (65W) 2.007V-2.066V 1.65V-2.31V RECOGNIZES AS Q11 FULL FUNCTIONS
2 A29 (45W) 2.558V-2.661V 2.31V-2.97V RECOGNIZES AS A29 LIMITED FUNCTIONS
3 AIRLINE 0.589V-0.663V 0.33V-0.99V FULL FUNCTIONS NO BATTERY CHARGING
4 HOOPER 3.19V-3.28V 2.97V-3.30V RECOGNIZES AS HOOPER LIMITED FUNCTIONS
PART# QTY DESCRIPTION REFERENCE DESIGNATOR(S) BOM OPTION
341S1707 1 IC,PMU,100PIN,LQFP U33
PART# QTY DESCRIPTION REFERENCE DESIGNATOR(S) CRITICAL BOM OPTION
197S0088 1 XTAL,10.0000MHZ,.01%,12PF,8X4.5MM,SMD Y6 CRITICAL ?
PMU
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DRAWING NUMBER 051-6694
REV. G
SCALE NONE
SHT 31 OF 45

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)
CRITICAL

J18
87438-0833
M-RT-SM

CHARGE_LED_L
+ADAPTER
ADAPTER_DET

R396 20K 1% 1/16W MF 402

R395 102K 1% 1/16W MF 402

R364 102K 1% 1/16W MF 402

R375 10K 1% 1/16W MF 402

R365 57.6K 1% 1/16W MF 402

R394 1M 5% 1/16W MF 402

C757 0.1UF 20% 25V CERM 805
NO STUFF
PLACE CLOSE TO DC INPUT

C468 0.01UF 20% 25V CERM 402

R363 10K 5% 1/16W MF 402

+3V_PMU

U15 LMC7211 SM
CRITICAL
1V20_REF
AC_DIV
AC_IN
AC_IN_L

Q10 2N7002DW SOT-363

R383 470K 5% 1/16W MF 402

GREATER THAN 13.5V DETECT

DC INRUSH LIMITER

Q13 SI4435DY SOI
Q16 SI4435DY SOI
S1 S2 S3 D1 D2 D3 D4 GATE

+ADAPTER_SW
+ADAPTER_SENSE

C572 0.010UF 20% 50V CERM 603

R414 330K 5% 1/16W MF 402
C458 0.1UF 20% 25V CERM 805

R474 47K 5% 1/16W MF 402
AC_ENABLE_GATE
R374 470K 5% 1/16W MF 402
AC_ENABLE_L
BCKFD_PROT_GATE
C592 0.01UF 20% 25V CERM 603
R499 68K 5% 1/16W MF 402
BCKFD_PROT_EN_L

Q10 2N7002DW SOT-363
Q21 2N7002DW SOT-363
AC_IN

+24V_PBUS

PLACE U23 NEXT TO R460

U23 MAX4172 TSSOP
CRITICAL
V+ RS+ RS- NC1 NC2 GND OUT PG
MAX4172_OUT
R466 10K 1% 1/16W MF 402
CURRENT THRESHOLD
R454 2.21K 1% 1/16W MF 603
C883 0.1UF 10% 50V X7R 603-1

U23 SENSE VOLTAGE DROP ACROSS R460

R460 0.025 1% 1W MF 2512

R488 4.7 5% 1/16W MF 402
R498 4.7 5% 1/16W MF 402
1772_CSSP
1772_CSSN
IF A29 ADAPTER USED, ADJUST CURRENT SETTING

1MSEC INTEGRATION TIME

R742 1K 1% 1/16W MF 402
C771 0.1UF 20% 10V CERM 402
IAC_RC_COMP
+3V_PMU
C772 0.1UF 20% 10V CERM 402
R747 42.2K 0.1% 1/16W 603
IAC_FB

U50 SOT23-5
CRITICAL

PLACE R358 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY

LTC1625_ITH
DP4 BAS16TW SOT-363
R358 150 1% 1/16W MF 402
1625_COMP
ADAPTER_I_REG

R738 42.2K 0.1% 1/16W MF 603
R734 82.5K 0.1% 1/16W MF 603
A29_CURRENT_ADJ
+3V_PMU
R739 51.1K 0.1% 1/16W MF 603
IF ADAPTER IS OVER 18V, ADJUST CURRENT SETTING

Q20 2N7002DW SOT-363
A29_DETECT
R748 100K 5% 1/16W MF 402
OVER_18V_ADJ
AC_GTR_18V
C775 1UF 20% 10V CERM 603
1772_ACOK
Q65 2N7002DW SOT-363

BATTERY SWITCH-OVER CIRCUIT

+BATT
F4 5AMP-125V SM-2
F3 5AMP-125V SM-2
+24V_PBUS
+PBUS
+BATT_24V_FUSE
+BATT_14V_FUSE

Q24 SI4435DY SOI
CRITICAL
Q76 SUD45P03 TO-252
CRITICAL
GATE

R490 47K 5% 1/16W MF 402
R746 47K 5% 1/16W MF 402
BATT_14V_GATE
BATT_24V_GATE

R512 10K 5% 1/16W MF 402
R744 10K 5% 1/16W MF 402
DP4 BAS16TW SOT-363
BATT_24PBUS_EN
BATT_14PBUS_EN

AC_IN_L
DP4 BAS16TW SOT-363
R489 158K 1% 1/16W MF 402
Q21 2N7002DW SOT-363
AC_IN_L_RC
C593 10UF 20% 6.3V CERM 805

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

+3V_PMU
R567 27.4K 1% 1/16W MF 402
R558 10K 1% 1/16W MF 402
R548 10K 1% 1/16W MF 402
OD OUTPUT LOW - WHEN AC GREATER THAN 18V

R560 4.12K 1% 1/16W MF 402
R565 48.7K 1% 1/16W MF 402
R566 1K 1% 1/16W MF 402
BATTV_HIGH
BATTV_LOW
BATT_LOW_L

Q27 2N7002DW SOT-363
R580 5.23K 1% 1/16W MF 402
Q29 2N7002DW SOT-363
Q29 2N7002DW SOT-363
PMU_CHARGE_V
Q27 2N7002DW SOT-363

R561 100K 5% 1/16W MF 402

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

R754 100K 1% 1/16W MF 402
D9 1N914 SOT23
R755 12.7K 1% 1/16W MF 402
C600 1UF 20% 50V CERM 1210

U31 MAX1772 QSOP
CRITICAL

1772_DCIN
1772_ACIN
1772_ACOK_L
(+3V_PMU)
1772_VCTL
1772_ICTL
1772_ICHG
1772_IINP
1772_CCV
1772_CCI
1772_CCS
1772_CCV_RC
1772_REF
1772_GND
1772_CLS
1772_CSSP
1772_CSSN
1772_LDO
1772_CELLS
1772_DLOV
1772_BST
1772_DHI
1772_LX
1772_DLO
(GND)
1772_CSIP
1772_CSIN
REF = 4.096V
REF_CLS = 4.096V / 27

R526 1K 1% 1/16W MF 402
C622 0.01UF 20% 25V CERM 402
C616 0.01UF 20% 16V CERM 402
R497 1K 1% 1/16W MF 402
C621 0.1UF 20% 25V CERM 402
C630 1UF 20% 10V CERM 603
R487 10K 1% 1/16W MF 402
R473 4.12K 1% 1/16W MF 402

C578 0.47UF 10% 16V CERM 1206
C579 0.47UF 10% 16V CERM 1206
R549 100K 5% 1/16W MF 402
C624 0.1UF 20% 25V CERM 603
R571 33 5% 1/8W 1206
D10 1N914 SOT23
1772_BST_ESR
R774 4.7 5% 1/16W MF 603
C608 0.1UF 20% 25V CERM 805

C652 1UF 20% 10V CERM 603
C817 0.1UF 20% 25V CERM 603
C802 0.1UF 20% 25V CERM 603
R559 100K 1% 1/16W MF 402
C906 0.0022UF 10% 50V CERM 402
NO STUFF
XW19 SM

Q63 IRF7805 SM
Q64 IRF7811W SO-8
CRITICAL

C547 2.2UF 10% 6.3V CERM 1812
C562 2.2UF 10% 6.3V CERM 1812
C563 2.2UF 10% 6.3V CERM 1812
C557 2.2UF 10% 6.3V CERM 1812
C564 2.2UF 10% 6.3V CERM 1812

L42 10UH SM1
CRITICAL
+BATT_RSNS
R763 0.05 1% 1W MF 2512
+BATT_24V_FUSE
D30 MBRS140T3 SM
CRITICAL

C619 4.7UF 20% 25V CERM 1206
C632 4.7UF 20% 25V CERM 1206
C617 4.7UF 20% 25V CERM 1206
C824 33UF 20% 25V ELEC SMI
C631 4.7UF 20% 25V CERM 1206
C633 4.7UF 20% 25V CERM 1206
C618 4.7UF 20% 25V CERM 1206

R543 1 5% 1/16W MF 603
R511 1 5% 1/16W MF 603

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{REFIN} / V_{CTL}))$
For 4.15V cells, VCTL = 0.123 REFIN
For 4.20V cells, VCTL = 0.245 REFIN
$I_{CHG} = (0.2048/R_{62}) * ICTL * (V_{REFIN} / V_{CTL})$

R588 100K 1% 1/16W MF 402
R579 499K 1% 1/16W MF 402
BATT_DIV
1V65_REF
U38 LMC7211 SM
CRITICAL
BATT_LOW
R599 100K 1% 1/16W MF 402
R570 100K 1% 1/16W MF 402
C658 0.047UF 10% 16V CERM 402

R578 100K 5% 1/16W MF 402
CHARGE_DISABLE
Q30 2N7002DW SOT-363
Q30 2N7002DW SOT-363
PMU_CHRG_BATT_V
C615 0.1UF 10% 25V CERM 402

R749 6.34K 1% 1/16W MF 402
A29_CLS_ADJ
Q65 2N7002DW SOT-363
A29_DETECT

+BATT_VSNS
+BATT_ISNS

BATTERY CONNECTOR
CRITICAL
J25
87438-0833
M-RT-SM
+BATT_POS (BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
BATT_NEG

L9 FERR-EMI-100-OHM SM
L53 FERR-50-OHM SM
L10 FERR-EMI-100-OHM SM
PMU_SMB_CLK
L8 FERR-EMI-100-OHM SM
PMU_SMB_DATA
L12 FERR-50-OHM SM

BATTERY CHARGER

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SCALE: NONE	SHT 32 OF 45	

12.8V PBUS SUPPLY

PBUS HOLD-UP CAPS

BACKUP BATTERY / USB CONNECTOR

PMU SUPPLY

BOOTSTRAP SYSTEM FROM ADAPTER OR BATTERY

+PBUS IS BOTH AN INPUT AND OUTPUT TO BUBBA
24V IS AN OUTPUT FROM BUBBA

WHEN +24V_PBUS IS BELOW ~13.44V, 1625 IS SHUT-OFF

CONNECT LTC1625 TK PIN AT TOP-SIDE FET

KEEP VIN/TK LOOP SHORT

IF SUPERCAP BOM OPTION IS CHOSEN:
OUTPUT AT U30.1 IS 5.65V
INPUT AT U25.8 IS 5.4V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S3575	1	RES,MF,1/16W/357K OHM,1%,0	402,SMD R521	?	SUPERCAP

12.8V REGULATOR

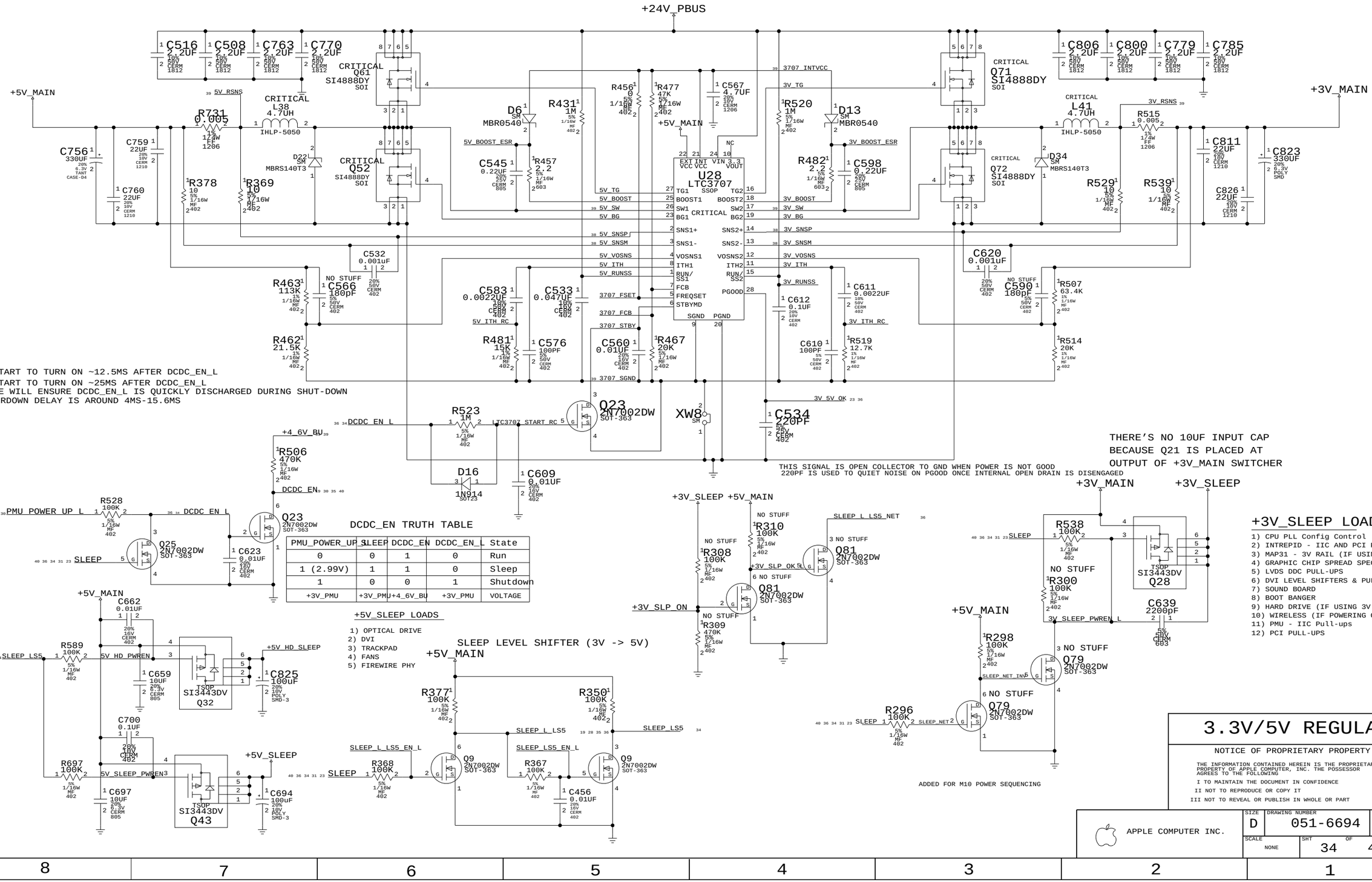
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G

SCALE: NONE

SHT 33 OF 45

3.3V/5V MAIN SUPPLY



DCDC_EN TRUTH TABLE

PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

3.3V/5V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 34 OF 45	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

+5V_MAIN

MAXBUS_SLEEP

CPU_VCORE_PWR_SEQ

CPU_VCORE_SEQ_L

CPU_VCORE_SEQ

SLEEP_L

DCDC_EN

CPU_VCORE_HI_OC

INT_GPIO1_PU

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

1.67GHZ (WITHOUT VCORE OFFSET) 1.300V -> 0.975V

+3V_MAIN

VCC NO STUFF U11 PT3B3257 QSOP

SEL = 0; Y1=A1
SEL = 1; Y1=B1

CRITICAL

Keep trace fat (40-100 mils) and short!!

+PBUS

+5V_MAIN

PLACE C423 CLOSE TO PINS 15 & 13!!!

U20 MAX1717 QSOP

VCORE_BOOST

VCORE_VPLUS

VCORE_BST2

VCORE_DH

VCORE_LX

VCORE_DL

VCORE_GND

VCORE_FB

VCORE_TIME

VCORE_VGATE

VCORE_MUX_SEL

VCORE_MUX_EN

VCORE_SLOW<1>
VCORE_SLOW<2>
VCORE_SLOW<3>
VCORE_SLOW<4>

VCORE_FAST<1>
VCORE_FAST<2>
VCORE_FAST<3>
VCORE_FAST<4>

VCORE_VID<1>
VCORE_VID<2>
VCORE_VID<3>
VCORE_VID<4>

NO_4XVCORE

CPU_VCORE_SLEEP

XW15 SM

CPU_VCORE_SLEEP_F

Keep trace fat and short!!

OMIT CRITICAL L36 1.2UH-18.3A SM1

CRITICAL D25 B540C SM

CRITICAL R331 0.001 1% 1W MF 2512

CPU_VCORE_SLEEP

Keep trace fat and short!!

Keep trace fat and short!!

Connect MAX1717 GND pin 13 to GND at bottom-side FET

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V WITH A 0.85 SCALE FACTOR, HENCE VOFFSET = 1.7V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

PLACE THIS SHORT AT PIN OF 1000uF CAP CLOSEST TO CPU

XW3 SM

VCORE_GNDSNS

VCORE_SNS

ROUTE AS DIFFERENTIAL PAIR

VCORE_GNDDIV

VCORE_GNDSNS

VCORE_GNDDIV_TEST

VCORE_GNDSNS_TEST

+3V_PMU_RESET

SOFT_PWR_ON_L

NC (RFU)

OUTPUT VOLTAGE

V DAC D4=0	V DAC D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, VB = V .

1.67GHZ (WITH VCORE OFFSET) 1.320V -> 0.990V
(CPU SPEC: 1.280V -> 0.980V)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S4023	1	RES,4.02KOHM,1%,1/16W,0402,LF	R321	VCORE13
114S2433	1	RES,2.43KOHM,1%,1/16W,0402,LF	R809	VCORE13

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S0242	1	IND,PWR,1.0UH,20,20.5A,SMD	L36	CRITICAL	

FMAX CONNECTOR

CRITICAL NO STUFF J5 M-ST-SM-52465-1217

VCORE SUPPLY

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APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6694 | REV. G
SCALE NONE | SHT 35 OF 45

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE
2) AGP I/O IF USING D3HOT

THERE'S 100K PULL-UP ON PG 31 ALREADY

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES
5) CLOCK SLEWING I/O
6) PCI1510 CORE

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD
2) INTREPID MEMORY I/O

DIODE PROVIDE PROVIDE QUICK SHUT-DOWN POWER DOWN DELAY 1.5MS TO 3.5MS

CHANGE R424 BACK TO 10K, 1%, AND STUFF 5.11K FOR 1.5V OPERATION
CONNECTING 1_5V_FB TO GND, FORCES 1.8V OUTPUT

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7450 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) OPTIONAL VIDEO MEMORY (M10 PRO ONLY)

1.5V/1.8V/2.5V SUPPLIES

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6694 | REV. G
SCALE NONE | SHT 36 OF 45

DIGITAL SIGNALS

GROUP	SIG_NAME		MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L				250.0000	10 MIL SPACING			5 8
	CPU_ADDR<0..31>		5		250			83 MHZ	5 8
	CPU_ARTRY_L				250.0000	10 MIL SPACING			5 8
	CPU_BG_L				250.0000	10 MIL SPACING			5 8
	CPU_BR_L				250.0000	10 MIL SPACING			5 8
	CPU_CI_L		5		250.0000				5 8
	CPU_DATA<0..31>		5		250			83 MHZ	6 8
	CPU_DATA<32..63>		5		250			83 MHZ	6 8
	CPU_DBG_L		5		250.0000	10 MIL SPACING			5 8
	CPU_DTI<0..2>		5		250				5 8
	CPU_DRDY_L_UF					10 MIL SPACING			
	CPU_DRDY_L				250.0000	10 MIL SPACING			5 8
	CPU_GBL_L		5		250.0000				5 8
	CPU_HIT_L				250.0000	10 MIL SPACING			5 8
	CPU_QACK_L		5		250.0000	10 MIL SPACING			5 8
	CPU_QREQ_L				250.0000	10 MIL SPACING			5 8
	CPU_TA_L				250.0000	10 MIL SPACING			5 8
	CPU_TBST_L		5		250.0000	10 MIL SPACING			5 8
	CPU_TEA_L				250.0000				5 8
	CPU_TS_L				250.0000	10 MIL SPACING			5 8
	CPU_TSIZ<0..2>		5		250				5 8
	CPU_TT<0..4>		5		250				5 8
	CPU_WT_L		5		250.0000				5 8
GROUP 0	MEM_DATA<7..0>		4		200			167 MHZ	9 10
	RAM_DATA_A<7..0>		4		200			167 MHZ	10 11
	RAM_DATA_B<7..0>		4		200			167 MHZ	10 11
	MEM_DQS<0>			TOTAL LENGTH CONTROLLED BY SPREADSHEET	200				9 10
	RAM_DQS_A<0>		4		200				10 11
	RAM_DQS_B<0>		4		200				10 11
	MEM_DQM<0>		4		200				9 10
	RAM_DQM_A<0>		4		200				10 11
	RAM_DQM_B<0>		4		200				10 11
GROUP 1	MEM_DATA<15..8>		4		200			167 MHZ	9 10
	RAM_DATA_A<15..8>		4		200			167 MHZ	10 11
	RAM_DATA_B<15..8>		4		200			167 MHZ	10 11
	MEM_DQS<1>		4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200				9 10
	RAM_DQS_A<1>		4		200				10 11
	RAM_DQS_B<1>		4		200				10 11
	MEM_DQM<1>				200				9 10
	RAM_DQM_A<1>		4		200				10 11
	RAM_DQM_B<1>		4		200				10 11
GROUP 2/3	MEM_DATA<31..16>		4		200			167 MHZ	9 10
	RAM_DATA_A<31..16>		4		200			167 MHZ	10 11
	RAM_DATA_B<31..16>		4		200			167 MHZ	10 11
	MEM_DQS<3..2>		4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167 MHZ	9 10
DDR RAM	RAM_DQS_A<3..2>		4		200			167 MHZ	10 11
	RAM_DQS_B<3..2>		4		200			167 MHZ	10 11
	MEM_DQM<3..2>		4		200			167 MHZ	9 10
	RAM_DQM_A<3..2>		4		200			167 MHZ	10 11
	RAM_DQM_B<3..2>		4		200			167 MHZ	10 11
GROUP 4/5	MEM_DATA<47..32>		4		200			167 MHZ	9 10
	RAM_DATA_A<47..32>		4		200			167 MHZ	10 11
	RAM_DATA_B<47..32>		4		200			167 MHZ	10 11
	MEM_DQS<5..4>		4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167 MHZ	9 10
	RAM_DQS_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQS_B<5..4>		4		200			167 MHZ	10 11
	MEM_DQM<5..4>		4		200			167 MHZ	9 10
	RAM_DQM_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQM_B<5..4>		4		200			167 MHZ	10 11
GROUP 6	MEM_DATA<55..48>		4		200			167 MHZ	9 10
	RAM_DATA_A<55..48>		4		200			167 MHZ	10 11
	RAM_DATA_B<55..48>		4		200			167 MHZ	10 11
	MEM_DQS<6>		4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200				9 10
	RAM_DQS_A<6>				200				10 11
	RAM_DQS_B<6>		4		200				10 11
	MEM_DQM<6>				200				9 10
	RAM_DQM_A<6>		4		200				10 11
	RAM_DQM_B<6>		4		200				10 11
GROUP 7	MEM_DATA<63..56>		4		200			167 MHZ	9 10
	RAM_DATA_A<63..56>		4		200			167 MHZ	10 11
	RAM_DATA_B<63..56>		4		200			167 MHZ	10 11
	MEM_DQS<7>		4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200				9 10
	RAM_DQS_A<7>				200				10 11
	RAM_DQS_B<7>				200				10 11
	MEM_DQM<7>		4		200				9 10
	RAM_DQM_A<7>		4		200				10 11
	RAM_DQM_B<7>		4		200				10 11
ADDR	MEM_ADDR<12..0>		4					83 MHZ	9
	RAM_ADDR<12..0>		6		200				9 11
	MEM_BA<1..0>		4						9
	RAM_BA<1..0>		6		200				9 11
CONTROL	MEM_CS_L<3..0>		4						9
	RAM_CS_L<3..0>		6		200				9 11
	MEM_CKE<3..0>		4						9
	RAM_CKE<3..0>		6		200				9 11
	MEM_RAS_L		4						9
	RAM_RAS_L				200.0000				9 11
	MEM_CAS_L		4						9
	RAM_CAS_L				200.0000				9 11
	MEM_WE_L		4						9
	RAM_WE_L				200.0000				9 11
	MEM_MUXSEL_H<1..0>		3						9 10
	MEM_MUXSEL_L<1..0>		3						9 10
	RAM_MUXSEL_H		5						10
	RAM_MUXSEL_L		5						10

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME			MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF						10 MIL SPACING		8
	SYSCLK_CPU			4		200.0000	10 MIL SPACING		5 8
	INT_CPUFB_OUT			3			10 MIL SPACING		8
	INT_CPUFB_OUT_SHORT			3			10 MIL SPACING		8
	INT_CPUFB_OUT_NORM			3			10 MIL SPACING		8
	INT_CPUFB_IN_NORM			3			10 MIL SPACING		8
	INT_CPUFB_LONG			3			10 MIL SPACING		8
	INT_CPUFB_IN					200.0000	10 MIL SPACING		8
	SYSCLK_DDRCLK_A0_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0	DDRCLK_A0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A0_L	DDRCLK_A0				200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1	DDRCLK_A1		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1_L	DDRCLK_A1				200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0	DDRCLK_B0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0_L	DDRCLK_B0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1	DDRCLK_B1		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1_L	DDRCLK_B1		3		200.0000	10 MIL SPACING		9 11
	INT_REF_CLK_OUT			3		200.0000	10 MIL SPACING		14
	INT_REF_CLK_IN					200.0000	10 MIL SPACING		14
	CLK66M_GPU_AGP_UF					200.0000	10 MIL SPACING		12
	CLK66M_GPU_AGP			4		200.0000	10 MIL SPACING		12 18
	INT_AGP_FB_OUT					200.0000	10 MIL SPACING		12
	INT_AGP_FB_IN			4		200.0000	10 MIL SPACING		12
	CLK33M_CBUS_UF					200.0000	10 MIL SPACING		12
	CLK33M_CBUS	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10 MIL SPACING		12 17
	CLK33M_AIRPORT_UF					200.0000	10 MIL SPACING		12
	CLK33M_AIRPORT	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10 MIL SPACING		12 25 40
	CLK33M_USB2_UF					200.0000	10 MIL SPACING		12
	CLK33M_USB2	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10 MIL SPACING		12 27
	INT_PCI_FB_OUT					200.0000	10 MIL SPACING		12
	INT_PCI_FB_IN			3		200.0000	10 MIL SPACING		12
MAP31	GPU_CLK27M_OUT						10 MIL SPACING		
	GPU_CLK27M_UF						10 MIL SPACING		
	GPU_SSCLK_UF						10 MIL SPACING		
	GPU_SSCLK_IN						10 MIL SPACING		
	GPU_FBCLK0						10 MIL SPACING		
	GPU_FBCLK0_L						10 MIL SPACING		
	GPU_FBCLK1						10 MIL SPACING		
	GPU_FBCLK1_L						10 MIL SPACING		
	GPU_DVO_CLKP						10 MIL SPACING		19
CRYSTALS	CLK27M_GPU_XOUT						10 MIL SPACING		
	CLK27M_XTAL_IN						10 MIL SPACING		
	CLK27M_GPU_XIN						10 MIL SPACING		
	CLK18M_INT_XIN						10 MIL SPACING		14
	CLK18M_INT_XOUT						10 MIL SPACING		14
	CLK18M_XTAL_IN						10 MIL SPACING		14
	CLK18M_INT_EXT						10 MIL SPACING		14
	CLK25M_ENET_XIN						10 MIL SPACING		28
	CLK25M_ENET_XOUT						10 MIL SPACING		28
	NEC_XT1						10 MIL SPACING		27
	NEC_XT2	THERE'S ANOTHER 280MIL LEG					10 MIL SPACING		27
SOUND	SND_SCLK			7		200.0000	10 MIL SPACING		14 26 40
	SND_CLKOUT					200.0000	10 MIL SPACING		14 26 40
ETHERNET MARVELL	CLKENET_PHY_RX					200.0000			28
	CLKENET_LINK_RX			3		200.0000	10 MIL SPACING		13 28
	CLKENET_PHY_GBE_REF					200.0000			28
	CLKENET_LINK_GBE_REF			3		200.0000	10 MIL SPACING		13 28
	CLKENET_PHY_TX					200.0000			28
	CLKENET_LINK_TX			5		200.0000	10 MIL SPACING		13 28
	CLKENET_LINK_GTX					200.0000			13
	CLKENET_PHY_GTX			3		200.0000	10 MIL SPACING		13 28
FIREWIRE	CLKFW_PHY_PCLK					200.0000			29
	CLKFW_LINK_PCLK			3		200.0000	10 MIL SPACING		13 29
	CLKFW_PHY_LCLK			3		200.0000	10 MIL SPACING		13 29
	CLKFW_LINK_LCLK					200.0000			13
	FW_XI					200.0000	10 MIL SPACING		29
	FW_OSC					200.0000	10 MIL SPACING		29

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G

SCALE	SHT	OF
NONE	37	45

Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
AGP	AGP_AD<15..0>		5	100				66 MHZ
AGP BYTES 0-1	AGP_CBE<1..0>		5	100				66 MHZ
	AGP_AD_STB<0>		5	100		8 MIL SPACING		
	AGP_AD_STB_L<0>		5	100		8 MIL SPACING		
AGP BYTES 2-3	AGP_AD<31..16>		5	100				66 MHZ
	AGP_CBE<3..2>		5	100				66 MHZ
	AGP_AD_STB<1>		5	100		8 MIL SPACING		
	AGP_AD_STB_L<1>			100		8 MIL SPACING		
AGP SIDEBAND	AGP_SBA<7..0>		5	100				66 MHZ
	AGP_SB_STB			100.0000		8 MIL SPACING		
	AGP_SB_STB_L		5	100.0000		8 MIL SPACING		
AGP CONTROL	AGP_FRAME_L			250.0000				
	AGP_IRDY_L			250.0000				
	AGP_TRDY_L		6	250.0000				
	AGP_DEVSEL_L			250.0000				
	AGP_STOP_L		6	250.0000				
	AGP_PAR		6	250.0000				
	AGP_REQ_L			285.0000				
	AGP_GNT_L			250.0000				
	AGP_RBF_L			250.0000				
DVO	GPU_DVOD<0..23>		5	250				
	GPU_DVO_HSYNC							
	GPU_DVO_VSYNC							
PCI	PCI_AD<31..0>					MIN_DAISY_CHAIN		33 MHZ
	PCI_CBE<3..0>					MIN_DAISY_CHAIN		33 MHZ
	PCI_FRAME_L					MIN_DAISY_CHAIN		
	PCI_IRDY_L					MIN_DAISY_CHAIN		
	PCI_TRDY_L					MIN_DAISY_CHAIN		
	PCI_DEVSEL_L					MIN_DAISY_CHAIN		
	PCI_STOP_L					MIN_DAISY_CHAIN		
	PCI_PAR					MIN_DAISY_CHAIN		
ULTRA ATA-100	UIDE_DATA<15..8>				200			100 MHZ
	UIDE_DATA<7>			NEED TO MATCH DELAY TO 250	200			
	UIDE_DATA<6..0>				200			100 MHZ
	UIDE_ADDR<2..0>				200			100 MHZ
	UIDE_RST_L				200.0000			
	UIDE_DIOW_L				200.0000			
	UIDE_DIOR_L			10 MIL SPACING	200.0000			
	UIDE_DMACK_L				200.0000			
	UIDE_CS0_L				200.0000			
	UIDE_CS1_L				200.0000			
	UIDE_DMARQ				200.0000			
	UIDE_IOCHRDY			10 MIL SPACING	200.0000			
	UIDE_INTRQ				200.0000			
	HD_DATA<15..0>		5	TOTAL UIDE+HD SKEW <500MIL	200			100 MHZ
	HD_ADDR<2..0>		5		200			100 MHZ
	HD_RESET_L		5		200.0000			
	HD_DIOW_L		5		200.0000			
	HD_DIOR_L		5	10 MIL SPACING	200.0000			
	HD_DMACK_L		5		200.0000			
	HD_CS0_L		5		200.0000			
	HD_CS1_L		5		200.0000			
	HD_DMARQ				200.0000			
	HD_IOCHRDY		5	10 MIL SPACING	200.0000			
	HD_INTRQ		5					
EIDE INTREPID	EIDE_DATA<15..0>							33 MHZ
	EIDE_ADDR<2..0>							33 MHZ
	EIDE_CS0_L							
	EIDE_CS1_L							
	EIDE_RD_L							
	EIDE_WR_L							
	EIDE_IOCHRDY							
	EIDE_INT							
	EIDE_RST_L							
	EIDE_DMACK_L							
	EIDE_DMARQ							
OPTICAL	EIDE_OPTICAL_DATA<15..0>							33 MHZ
	EIDE_OPTICAL_ADDR<2..0>							33 MHZ
	EIDE_OPTICAL_CS0_L							
	EIDE_OPTICAL_CS1_L							
	EIDE_OPTICAL_RD_L							
	EIDE_OPTICAL_WR_L							
	EIDE_OPTICAL_IOCHRDY							
	EIDE_OPTICAL_INT							
	EIDE_OPTICAL_RST_L							
	EIDE_OPTICAL_DMAACK_L							
	EIDE_OPTICAL_DMA_RQ							
ETHERNET MII	ENET_LINK_RXD<7..0>		5					
	ENET_RX_DV							
	ENET_RX_ER							
	ENET_PHY_TXD<7..0>		5					
	ENET_LINK_TXD<7..0>							
	ENET_PHY_TX_ER		5					
	ENET_LINK_TX_ER							
	ENET_PHY_TX_EN		5					
	ENET_LINK_TX_EN							
	ENET_MDIO							
	ENET_MDC							
	ENET_COL							
	ENET_CRS							
FIREWIRE MII	FW_LINK_DATA<7..0>		5					
	FW_PHY_DATA<7..0>		5					
	FW_LINK_CNTL<1..0>							
	FW_PHY_CNTL<1..0>							
	FW_LINK_LREQ							
	FW_PHY_LREQ							
	FW_PINT							

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS
ETHERNET	MDI_M<0>	ENET_MDI0			
	MDI_P<0>	ENET_MDI0			
	MDI_M<1>	ENET_MDI1	SPACING DELETED BECAUSE		
	MDI_P<1>	ENET_MDI1	OF PHYSICAL CONSTRAINTS		
	MDI_M<2>	ENET_MDI2	AROUND MARVELL PHY		
	MDI_P<2>	ENET_MDI2			
	MDI_M<3>	ENET_MDI3			
	MDI_P<3>	ENET_MDI3			
	RJ45_DN<0>	RJ45_DP0		10 MIL SPACING	
	RJ45_DP<0>	RJ45_DP0		10 MIL SPACING	
	RJ45_DN<1>	RJ45_DP1		10 MIL SPACING	
	RJ45_DP<1>	RJ45_DP1		10 MIL SPACING	
	RJ45_DN<2>	RJ45_DP2		10 MIL SPACING	
	RJ45_DP<2>	RJ45_DP2		10 MIL SPACING	
	RJ45_DN<3>	RJ45_DP3		10 MIL SPACING	
	RJ45_DP<3>	RJ45_DP3		10 MIL SPACING	
FIREWIRE	FW_TPA0N	FW_TPA0		MIN_LINE_WIDTH=3.4 10 MIL SPACING	
	FW_TPA0P	FW_TPA0		MIN_LINE_WIDTH=3.4 10 MIL SPACING	
	FW_TPB0N	FW_TPB0		MIN_LINE_WIDTH=3.4 10 MIL SPACING	
	FW_TPB0P	FW_TPB0		MIN_LINE_WIDTH=3.4 10 MIL SPACING	
	FW_TPI0N	FW_TPI0		MIN_LINE_WIDTH=3.4 10 MIL SPACING	
	FW_TPI0P	FW_TPI0		MIN_LINE_WIDTH=3.4 10 MIL SPACING	
	FW_TPO0N	FW_TPO0		MIN_LINE_WIDTH=3.4 10 MIL SPACING	
	FW_TPO0P	FW_TPO0		MIN_LINE_WIDTH=3.4 10 MIL SPACING	
	FW_TPA1N	FW_TPA1	500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING	
	FW_TPA1P	FW_TPA1	500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING	
	FW_TPB1N	FW_TPB1	500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING	
	FW_TPB1P	FW_TPB1	500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING	
	FW_TPI1N	FW_TPI1		MIN_LINE_WIDTH=3.4 10 MIL SPACING	
	FW_TPI1P	FW_TPI1		MIN_LINE_WIDTH=3.4 10 MIL SPACING	
	FW_TPO1N	FW_TPO1		MIN_LINE_WIDTH=3.4 10 MIL SPACING	
	FW_TPO1P	FW_TPO1		MIN_LINE_WIDTH=3.4 10 MIL SPACING	
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L		10 MIL SPACING	4
	CLKLVDS_LP	CLKLVDS_L		10 MIL SPACING	4
	LVDS_L0N	LVDS_L0		10 MIL SPACING	
	LVDS_L0P	LVDS_L0		10 MIL SPACING	
	LVDS_L1N	LVDS_L1		10 MIL SPACING	
	LVDS_L1P	LVDS_L1		10 MIL SPACING	
	LVDS_L2N	LVDS_L2		10 MIL SPACING	
	LVDS_L2P	LVDS_L2		10 MIL SPACING	
UPPER	CLKLVDS_UN	CLKLVDS_U		10 MIL SPACING	4
	CLKLVDS_UP	CLKLVDS_U		10 MIL SPACING	4
	LVDS_U0N	LVDS_U0		10 MIL SPACING	
	LVDS_U0P	LVDS_U0		10 MIL SPACING	
	LVDS_U1N	LVDS_U1		10 MIL SPACING	
	LVDS_U1P	LVDS_U1		10 MIL SPACING	
	LVDS_U2N	LVDS_U2		10 MIL SPACING	
	LVDS_U2P	LVDS_U2		10 MIL SPACING	
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS		10 MIL SPACING	4
	TMDS_CONN_CLKP	CLKCONN_TMDS		10 MIL SPACING	4
	TMDS_CLKN	CLKTMDS		10 MIL SPACING	4
	TMDS_CLKP	CLKTMDS		10 MIL SPACING	4
	TMDS_DN<0>	TMDS_D0		10 MIL SPACING	
	TMDS_DP<0>	TMDS_D0		10 MIL SPACING	
	TMDS_DN<1>	TMDS_D1		10 MIL SPACING	
	TMDS_DP<1>	TMDS_D1		10 MIL SPACING	
	TMDS_DN<2>	TMDS_D2		10 MIL SPACING	
	TMDS_DP<2>	TMDS_D2		10 MIL SPACING	
USB	NEC_USB_DAM	NEC_USB_DA	MIN_LINE_WIDTH=5	10 MIL SPACING	
	NEC_USB_DAP	NEC_USB_DA	MIN_LINE_WIDTH=5	10 MIL SPACING	
	USB_DEM	USB_DE		5 MIL SPACING	
	USB_DEP	USB_DE		5 MIL SPACING	
	NEC_USB_DBM	NEC_USB_DB	MIN_LINE_WIDTH=5	10 MIL SPACING	
	NEC_USB_DBP	NEC_USB_DB	MIN_LINE_WIDTH=5	10 MIL SPACING	
	USB_DFM	USB_DF		5 MIL SPACING	
	USB_DFP	USB_DF		5 MIL SPACING	
	BT_USB_DM	BT_USB_D		5 MIL SPACING	
	BT_USB_DP	BT_USB_D		5 MIL SPACING	
	NEC_USB_RSDM1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10 MIL SPACING	
	NEC_USB_RSDP1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10 MIL SPACING	
	NEC_USB_RSDM2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10 MIL SPACING	
	NEC_USB_RSDP2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10 MIL SPACING	
	MODEM_USB_DM	MODEM_USB_D		5 MIL SPACING	
	MODEM_USB_DP	MODEM_USB_D		5 MIL SPACING	
	LEFT_USB_DM	LEFT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING	
	LEFT_USB_DP	LEFT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING	
	RIGHT_USB_DM	RIGHT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING	
	RIGHT_USB_DP	RIGHT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING	
POWER SUPPLIES	1772_CSSN	1772_CSS		DIFF	
	1772_CSSP	1772_CSS		DIFF	
	1772_CSIN	1772_CSI		DIFF	
	1772_CSIP	1772_CSI		DIFF	
	3V_SNSM	3V_SNS		DIFF	
	3V_SNSP	3V_SNS		DIFF	
	5V_SNSM	5V_SNS		DIFF	
	5V_SNSP	5V_SNS		DIFF	
THERMOSTAT	THERM1_DM	THERM1		DIFF	
	THERM1_DP	THERM1		DIFF	
	THERM2_DM	THERM2		DIFF	
	THERM2_DP	THERM2		DIFF	
	THERM1_M_DM	THERM1_MAIN		DIFF	
	THERM1_M_DP	THERM1_MAIN		DIFF	
	THERM2_M_DM	THERM2_MAIN		DIFF	
	THERM2_M_DP	THERM2_MAIN		DIFF	
	THERM1_A_DM	THERM1_ALT		DIFF	
	THERM1_A_DP	THERM1_ALT		DIFF	
	THERM2_A_DM	THERM2_ALT		DIFF	
	THERM2_A_DP	THERM2_ALT		DIFF	

INTERNAL LAYER

ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.80HM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)

ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 38 OF 45	

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 40
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 40
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 23
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 23
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6 20 23
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 40
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6 40
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 36
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 36
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 32 33
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 32
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 32
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32 40
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32 40
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	32
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 32
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 32
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 32
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 32
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 31 33
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33 34
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 26 31
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 25 34
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 25
TRACKPAD	+5V_MAIN_CONN	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 23 40
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22 40
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22 40
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22 40
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10 22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22 40
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22 40
KB LED	KBDLED_ANODE	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 23
	KBDLED_RETURN	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 23
FAN GND	FANL_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 40
	FANR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 40
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15 26

I/O AREA	GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6
	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND1
INVERTER	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND2
TRACKPAD	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND3
LVDS	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND4 40
I/O AREA	CHGND5	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND5
I/O AREA	CHGND6	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND6
	ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 28

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5 6 35 40
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5 6 7 8 15 16 35
DDR RAM INTREPID PLLS	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 11
	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 14
	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5 14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5 12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 12 18
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 13
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 17
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 17
ATI M11	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 18 19 40
	+GPU_MEM	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 18 21
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 12 18 19 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8 21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 12 15 16 18 19 21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 21
	+GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 18 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 19 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 19
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
1321	1_8V_GPU_VDDCI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
1322	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 18
1326	2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
1324	1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
1323	1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
1325	1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
1327	GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
1328	1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
1311	1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
1310	3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 18
1309	3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 18
1312	GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 19
1313	2_5V_SLEEP_NECK2	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
1317	3V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
1315	1_5V_AGP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
1316	1_8V_PVDD_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
1314	GPU_VCORE_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
1318	GPU_VDD15_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
1319	2_5V_SLEEP_NECK2	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
1320	1_8V_SLEEP_NECK	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
1321	1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
1322	2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
SILICON IMIAGE	PP3V3_SI_PVCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
1335	PP3V3_SI_AVCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
1337	PP3V3_SI_VCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
1336	PP3V3_SI_PVCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
1337	PP3V3_SI_AVCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
1338	PP3V3_SI_VCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 28
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8 28
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8 28
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8 28
	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
FW	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 30
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 30
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 29 30
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29 30
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6 29
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 30 40
USB 2.0 INTREPID SSCG	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 27
	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 27
	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8 14
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8 14

MIN_NECK_WIDTH REDUCED FOR TESTPOINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 33
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 2 33
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 4
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 4
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 4
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 4
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 4
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 34
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 6
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 6
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 6
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 6
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 6
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 6
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 6
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 6
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 6
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 6
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	2_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	MAX1715_TON		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	MAX1715_SKIP		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 6
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 6
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 5
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 5
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 5
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 5
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 5
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 5
	VCORE_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_REF		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_CC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35 40
	VCORE_TIME		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_VGATE		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 14 35
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=15 5
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 9
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 9
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 9
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 9
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 9
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 9
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 9
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 9
	1778_ION		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19
	1778_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19
	1778_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	1778_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19 40
	1778_FCB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19
	1778_VRNG		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 6
	1_8V_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
	LTC3411_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
	LTC3411_SYNC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
	LTC3411_SHDN		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 4
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10

SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 39 OF 45	

FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 13 28
FUNC_TEST=YES JTAG_ASIC_TDI 28
FUNC_TEST=YES JTAG_ASIC_TDO 13 14
FUNC_TEST=YES JTAG_ASIC_TCK 13 28
FUNC_TEST=YES JTAG_ASIC_TRST_L 13 28
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5
FUNC_TEST=YES CPU_SRESET_L 5
FUNC_TEST=YES CPU_HRESET_L 5 6 7
FUNC_TEST=YES JTAG_CPU_TMS 5 6
FUNC_TEST=YES JTAG_CPU_TDI 5 6
FUNC_TEST=YES JTAG_CPU_TDO_TP 5
FUNC_TEST=YES JTAG_CPU_TCK 5 6
FUNC_TEST=YES JTAG_CPU_TRST_L 5 6 40

FUNC_TEST=YES TMDS_CONN_CLKP 22 38
FUNC_TEST=YES VGA_R 22
FUNC_TEST=YES VGA_G 22
FUNC_TEST=YES VGA_B 22
FUNC_TEST=YES VGA_VSYNC 22
FUNC_TEST=YES VGA_HSYNC 22
FUNC_TEST=YES DVI_DDC_CLK_UF 22
FUNC_TEST=YES DVI_DDC_DATA_UF 22
FUNC_TEST=YES DVI_HPD_UF 22
FUNC_TEST=YES LVDS_L0N 19 22 38
FUNC_TEST=YES LVDS_L0P 19 22 38
FUNC_TEST=YES LVDS_L1N 19 22 38
FUNC_TEST=YES LVDS_L1P 19 22 38
FUNC_TEST=YES LVDS_L2N 19 22 38
FUNC_TEST=YES LVDS_L2P 19 22 38
FUNC_TEST=YES CLKLVDS_LN 19 22 38
FUNC_TEST=YES CLKLVDS_LP 19 22 38
FUNC_TEST=YES LVDS_U0N 19 22 38
FUNC_TEST=YES LVDS_U0P 19 22 38
FUNC_TEST=YES LVDS_U1N 19 22 38
FUNC_TEST=YES LVDS_U1P 19 22 38
FUNC_TEST=YES LVDS_U2N 19 22 38
FUNC_TEST=YES LVDS_U2P 19 22 38
FUNC_TEST=YES CLKLVDS_UN 19 22 38
FUNC_TEST=YES CLKLVDS_UP 19 22 38
FUNC_TEST=YES LVDS_DDC_CLK 19 22
FUNC_TEST=YES LVDS_DDC_DATA 19 22
FUNC_TEST=YES BRIGHT_PWM 22
FUNC_TEST=YES TV_GND1 22 39
FUNC_TEST=YES TV_GND2 22 39

FUNC_TEST=YES TV_C 22
FUNC_TEST=YES TV_Y 22
FUNC_TEST=YES TV_COMP 22
FUNC_TEST=YES SND_TO_AUDIO 14 26
FUNC_TEST=YES SND_SYNC 14 26
FUNC_TEST=YES SND_CLKOUT 14 26 37

FUNC_TEST=YES INT_AUDIO_TO_SND 14 26
FUNC_TEST=YES SND_SCLK 14 26 37
FUNC_TEST=YES SND_HW_RESET_L 14 26
FUNC_TEST=YES SND_HP_SENSE_L
FUNC_TEST=YES SND_LIN_SENSE_L
FUNC_TEST=YES INT_I2C_DATA2 14 26
FUNC_TEST=YES INT_I2C_CLK2 14 26
FUNC_TEST=YES ~~I393~~ CHGND4 39
FUNC_TEST=YES ~~I394~~ SLEEP_LED

FUNC_TEST=YES INT_I2C_CLK0 6 11 13 23
FUNC_TEST=YES INT_I2C_DATA0 6 11 13 23
FUNC_TEST=YES INT_I2C_CLK1 13 14 23 24 26
FUNC_TEST=YES INT_I2C_DATA1 13 14 23 24 26
FUNC_TEST=YES CBUS_DET_1_L 17
FUNC_TEST=YES CBUS_DET_2_L 17
FUNC_TEST=YES TMDS_DN<0> 20 22 38
FUNC_TEST=YES TMDS_DP<0> 20 22 38
FUNC_TEST=YES TMDS_DN<1> 20 22 38
FUNC_TEST=YES TMDS_DP<1> 20 22 38
FUNC_TEST=YES TMDS_DN<2> 20 22 38
FUNC_TEST=YES TMDS_DP<2> 20 22 38
FUNC_TEST=YES TMDS_CONN_CLKN 22 38

FUNC_TEST=YES BT_USB_DM 14 25 38
FUNC_TEST=YES BT_USB_DP 14 25 38
FUNC_TEST=YES MODEM_USB_DM 14 26 38
FUNC_TEST=YES MODEM_USB_DP 14 26 38
FUNC_TEST=YES PCI_AD<0> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<1> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<2> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<3> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<4> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<5> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<6> 9 12 17 25 27 38

FUNC_TEST=YES PCI_AD<7> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<8> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<9> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<10> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<11> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<12> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<13> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<14> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<15> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<16> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<17> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<18> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<19> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<20> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<21> 12 17 25 27 38
FUNC_TEST=YES PCI_AD<22> 12 17 25 27 38
FUNC_TEST=YES PCI_AD<23> 12 17 25 27 38
FUNC_TEST=YES PCI_AD<24> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<25> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<26> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<27> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<28> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<29> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<30> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<31> 9 12 17 25 27 38
FUNC_TEST=YES PCI_FRAME_L 12 17 25 27 38
FUNC_TEST=YES PCI_TRDY_L 12 17 25 27 38
FUNC_TEST=YES PCI_IRDY_L 12 17 25 27 38
FUNC_TEST=YES PCI_DEVSEL_L 12 17 25 27 38
FUNC_TEST=YES PCI_STOP_L 12 17 25 27 38

FUNC_TEST=YES PCI_PAR 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<0> 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<1> 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<2> 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<3> 12 17 25 27 38
FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 25
FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 25
FUNC_TEST=YES AIRPORT_PCI_INT_L 14 25
FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 25 38
FUNC_TEST=YES EIDE_OPTICAL_RD_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 25 38
FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 25 38
FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 25 38
FUNC_TEST=YES SND_AMP_MUTE 26
FUNC_TEST=YES SND_HP_MUTE_INV

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_CS1_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_RST_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_WR_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 25 38
FUNC_TEST=YES EIDE_OPTICAL_INT 25 38
FUNC_TEST=YES TPAD_F_TXD
FUNC_TEST=YES TPAD_F_RXD
FUNC_TEST=YES LID_CLOSED_L 23
FUNC_TEST=YES COMM_RESET_L 14 26
FUNC_TEST=YES COMM_SHUTDOWN 14 26
FUNC_TEST=YES COMM_RING_DET_L 14 26 31

FUNC_TEST=YES +5V_TPAD_SLEEP
FUNC_TEST=YES +3V_HALL_EFFECT 23 39
FUNC_TEST=YES KBD_CAPSLOCK_LED
FUNC_TEST=YES KBD_FUNCTION_L 23 31
FUNC_TEST=YES KBD_CONTROL_L 23 31
FUNC_TEST=YES +PPBATT_ISNS_N 24
FUNC_TEST=YES KBD_OPTION_L 23 31
FUNC_TEST=YES KBD_SHIFT_L 23 31
FUNC_TEST=YES KBD_X<0> 23 31
FUNC_TEST=YES KBD_X<1> 23 31
FUNC_TEST=YES KBD_X<3> 23 31
FUNC_TEST=YES MMM_ACC_SELFTEST 24
FUNC_TEST=YES MMM_ACC_X_AXIS 24
FUNC_TEST=YES MMM_ACC_Y_AXIS 24
FUNC_TEST=YES MMM_ACC_Z_AXIS 24

FUNC_TEST=YES SRCLK_TP 27
FUNC_TEST=YES SRMOD_TP 27
FUNC_TEST=YES TEB_TP 27
FUNC_TEST=YES TEST_TP 27

FUNC_TEST=YES KBD_Y<0> 31
FUNC_TEST=YES KBD_Y<1> 31
FUNC_TEST=YES KBD_Y<3> 31
FUNC_TEST=YES KBD_Y<4> 31
FUNC_TEST=YES KBD_Y<6> 31
FUNC_TEST=YES KBD_Y<7> 31
FUNC_TEST=YES KBD_NUMLOCK_LED
FUNC_TEST=YES +BATT_POS 32 39
FUNC_TEST=YES BATT_CLK 32
FUNC_TEST=YES BATT_DATA 32
FUNC_TEST=YES BATT_NEG 32 39
FUNC_TEST=YES PMU_BATT_DET_L 31 32
FUNC_TEST=YES FANR_GND 39

FUNC_TEST=YES FANL_GND 39
FUNC_TEST=YES FANL_TACH
FUNC_TEST=YES FANR_PWM
FUNC_TEST=YES FANL_PWM
FUNC_TEST=YES RJ45_DP<0> 28 38
FUNC_TEST=YES RJ45_DN<0> 28 38
FUNC_TEST=YES RJ45_DP<1> 28 38
FUNC_TEST=YES RJ45_DN<1> 28 38
FUNC_TEST=YES RJ45_DP<2> 28 38
FUNC_TEST=YES RJ45_DN<2> 28 38
FUNC_TEST=YES RJ45_DP<3> 28 38
FUNC_TEST=YES RJ45_DN<3> 28 38
FUNC_TEST=YES FW_TPO0R 30 39
FUNC_TEST=YES VCORE_VID0
FUNC_TEST=YES VCORE_VID1
FUNC_TEST=YES VCORE_VID2
FUNC_TEST=YES VCORE_VID3
FUNC_TEST=YES VCORE_VID4

FUNC_TEST=YES FW_TPO1P 30 38
FUNC_TEST=YES FW_TPO1N 30 38
FUNC_TEST=YES FW_TPI1P 30 38
FUNC_TEST=YES FW_TPI1N 30 38
FUNC_TEST=YES CHARGE_LED_L 31 32
FUNC_TEST=YES ADAPTER_DET 31 32
FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 25
FUNC_TEST=YES SUTRO_ALS_OUT 23 25
FUNC_TEST=YES KBD_LED1_OUT
FUNC_TEST=YES KBD_LED2_OUT
FUNC_TEST=YES COMM_TXD_L 14 26
FUNC_TEST=YES COMM_TRXC 14 26
FUNC_TEST=YES COMM_GPIO_L 14 26
FUNC_TEST=YES COMM_DTR_L 14 26
FUNC_TEST=YES COMM_RTS_L 14 26
FUNC_TEST=YES COMM_RXD 14 26
FUNC_TEST=YES PMU_KB_RESET_L
FUNC_TEST=YES PWR_BUTTON_L 23 26
FUNC_TEST=YES +PBUS 39
FUNC_TEST=YES +24V_PBUS 39
FUNC_TEST=YES GPU_VCORE 18 19 39
FUNC_TEST=YES CPU_VCORE_SLEEP 5 6 35 39
FUNC_TEST=YES VCORE_FB 35 39
FUNC_TEST=YES +1_8V_MAIN 39
FUNC_TEST=YES +3V_PMU 39
FUNC_TEST=YES +5V_DDC_SLEEP 22 39
FUNC_TEST=YES +12_8V_INV 22 39
FUNC_TEST=YES VCORE_MUX_EN 35

FUNC_TEST=YES +5V_INV_SW 22 39
FUNC_TEST=YES LEFT_USB_DM 25 27 38
FUNC_TEST=YES LEFT_USB_DP 25 27 38
FUNC_TEST=YES RIGHT_USB_DM 27 33 38
FUNC_TEST=YES RIGHT_USB_DP 27 33 38
FUNC_TEST=YES NEC_LEFT_USB_PWREN 25 27
FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 25 27
FUNC_TEST=YES NEC_RIGHT_USB_PWREN 27 33
FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 27 33
FUNC_TEST=YES DCDC_EN 19 30 34 35
FUNC_TEST=YES BBANG_HRESET_L 6

FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 25 27 31
FUNC_TEST=YES RF_DISABLE_L_SPN 25
FUNC_TEST=YES AIRPORT_CLKRUN_L 25
FUNC_TEST=YES ROM_RW_L 9 12 25
FUNC_TEST=YES ROM_ONBOARD_CS_L 9 25
FUNC_TEST=YES ROM_CS_L 9 12 25
FUNC_TEST=YES CLK33M_AIRPORT 12 25 37
FUNC_TEST=YES AIRPORT_IDSEL 25
FUNC_TEST=YES ROM_OE_L 9 12 25
FUNC_TEST=YES INT_MOD_DTI 14 26
FUNC_TEST=YES JTAG_CPU_TRST_L 5 6 40
FUNC_TEST=YES MOD_BITCLK 14 26
FUNC_TEST=YES MOD_CLKOUT 14 26
FUNC_TEST=YES MOD_DTO 14 26
FUNC_TEST=YES MOD_SYNC 14 26
FUNC_TEST=YES SLEEP 23 31 34 36
FUNC_TEST=YES 1778_VFB 19 39

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6694 | REV. G

SCALE NONE | SHT 40 OF 45

REVISION HISTORY

12/11/03

1) IMPORTED Q41 PRODUCTION RELEASE SCHEMATIC
2) CHANGED CPU (U43) TO A7PM
3) CHANGED PLL CONFIG SIUEEING FOR NEW CPU
4) CHANGED U41 TO M1T-CSP64 SYMBOL
5) ADDED CPU AVDD LDO (D5)
6) ADDED R284 AND R604 TO ADD OPTION FOR PD_L OE_U42 (CLOCK CHIP) TO BE DRIVEN BY JTAG_ASIC_TDO FROM INTREPID
7) ADDED R888 TO DISCONNECT INT_GPIO9 FROM CC FSE
8) CHANGED JTAG_ASIC_TDO_TP TO JTAG_ASIC_TDO AND MOVED IT TO INTREPID'S TDO
9) CHANGED JTAG_ASIC_TDI TO CONNECT TO ETHERNET PHY'S TDI

12/15/03

10) CHANGED PIN 4 (DCDC_EN) ON J11 TO NEC_RIGHT_USBOVERCURRENT
11) CHANGED PIN 11 OF J11 TO NC

12/16/03

12) ADDED R633 AS PULLUP ON JTAG_ASIC_TDI
13) CHANGED CPU_TEMP_DN TO CPU_THERM_DM
14) CHANGED CPU_TEMP_DP TO CPU_THERM_DP
15) CHANGED GPU_THERM_DP TO GPU_THERM_DP_TP
16) CHANGED GPU_THERM_DN TO GPU_THERM_DM_TP
17) FIXED MISSED CONNECTION WITH MAXBUS_SLEEP TO CPU

12/17/03

18) CHANGED R657 (EXTPLL_SDWN_POL_BOOT_STRAP) TO NO_STUFF AND REMOVED NO_STUFF FROM R153
19) UPDATE DIFF_NET_SPACING_TYPE PROPERTY ON POWER_SUPPLY_SENSE AND THERMAL DIODE DIFF PAIRS
20) CHANGED FIREWIRE OSCILLATOR (G1) TO NEW PREFERRED SUNNY PART

12/18/03

21) CHANGED MAX VIA COUNT ON ALL AGP STB NETS TO 5 TO CLEAR DRCS

** RELEASED FOR EVT **

2/10/04

22) REMOVED XW11 - JUMPER ON 1.8V SWITCHER OUTPUT
23) CHANGED R857 TO STUFFE AND R153 TO NO STUFF
24) CHANGED CPU PLL CONFIG TO 9X HIGH AND 5X LOW

** RELEASED FOR DVT **

3/24/04

25) REMOVED ALTERNATE BOM OPTION FROM ALTERNATE ETHERNET CRYSTALS

3/29/04

26) ADDED ALTERNATE FOR Q41A REV 1.1.1 CPU (U43)
27) ADDED ALTERNATES FOR 128MB AND 64MB A16 M1T'S
28) CHANGED TMDS SERIES RPAKS TO 0 OHMS (RP57,RP27,RP32,RP28)
29) ADDED ALTERNATE FOR ALS OP-AMP (U40)

** RELEASED TO REV A **

30) CHANGED TMDS TERMINATION R,C AND LS TO PRODUCTION VALUES

** RELEASED TO REV A UNDER NEW PART NUMBER **

09/17/2004

1) GPU_DVOD<0..12> NETNAME CHANGE TO GPU_DVOD<0..23>
2) D8 FROM 1N5227B CHANGE TO BZX84C2V7LT1
3) R751 VALUE FROM 10K OHM CHANGE TO 604 OHM
4) ADD C935 (0.1UF)
5) ADD R867 (0 OHM) FOR IPOD ACTION
6) PMU PIN74 NETNAME FROM NC TO PMU_SELECT
7) ADD R868 (10K OHM; NO_STUFF) PULL UP TO +3V_PMU
8) ADD R869 (10K OHM) PULL DOWN TO GND
9) PMU PIN 91 NETNAME FROM NC TO SYS_BATT_ISNS2
10) ADD R870 (0 OHM) SYS_BATT_ISNS2 LINK TO SYS_BATT_ISNS
11) ADD U51 (INA138)
12) ADD R852 (0.010 OHM),R853 (150K OHM) AND R857(49.9 OHM)
13) ADD C917 (0.1UF) AND C925 (10UF)
14) ADD DESCRIPTION FOR MMM I2C BUS
15) MMM I2C BUS LINK TO INTREPID :INT_I2C_CLK1 AND INT_I2C_DATA1
16) CHANGE NETNAME FROM INT_EXTINT11_PU TO MMM_FFIRQ_L
17) CHANGE NETNAME FROM INT_EXTINT12_PU TO MMM_SIRQ_L
18) ADD R863 (10K OHM) AND R864 (10K OHM) FOR MMM_FFIRQ_L&MMM_SIRQ_L PULL UP TO +3V_MAIN
19) ADD U53 (16F818) AND U5 (KXM52)
20) ADD R845 (0 OHM),R846 (0 OHM;NO_STUFF),R847 (10K OHM;NO_STUFF),R848 (10K OHM;NO_STUFF)
21) ADD R849 (10K OHM),R850 (10K OHM;NO_STUFF),R851(0 OHM),R854 (10K OHM),R856 (10K OHM),
22) ADD R860 (0 OHM),R858 (0 OHM),R859 (0 OHM),R855 (10K OHM),R861 (10K OHM),R862(10K OHM;NO_STUFF)
23) ADD C936(0.1UF),C918(0.1UF),C919(0.1UF),C921(0.0047UF),C923(0.0047UF),C926(0.0047UF),C927(0.1UF)
24) DEL RP44 (100K OHM) AND ADD R874 (100K OHM), R875 (100K OHM) AND R873 (100K OHM)
25) ADD R872 (10K OHM) FOR AUDIO_LO_MUTE_L
26) ADD R871 (100 OHM) AND SUPERCAP C937 (N20P80;5.5V;ELEC;0.33F)
27) J21 PIN12 NETNAME FROM NC CHANGE TO THERM_L_OC
28) J21 PIN10 NETNAME FROM NC CHANGE TO INT_I2C_DATA1
29) J21 PIN11 NETNAME FROM NC CHANGE TO INT_I2C_CLK1
30) C592 VALUE FROM 0.001UF CHANGE TO 0.01UF (20%,50V,0603)
31) U59 FROM MP1518DJ CHANGE TO MM3120
32) L11 CHANGE TO 152S0235 (22UH;3.8*3.8*1.5MM)
33) DEL D31
34) R202 VALUE FROM 5.23 OHM CHANGE TO 25.5 OHM
35) C79 VALUE FROM 2.2UF CHANGE TO 1UF
36) ADD Q70 (SI3443), Q34 (2N7002)
37) ADD R866 (100K OHM),R865 (4.7 OHM),C929 (0.022UF)

09/20/2004

1) ADD R877 (10K OHM)
2) ADD R876 (470K OHM;NO_STUFF)

09/21/2004

1) ADD R878 AND R879 (0 OHM;NO_STUFF)[ADD A 0-OHM RESISTOR TO BY-PASS THE N-FET ON EACH FAN]

09/22/2004

1) R822 (680 OHM CHANGE TO 510 OHM) AND R826 (680 OHM CHANGE TO 510 OHM)

09/23/2004

1) ADD NC NETNAME AT U59 PIN6 AND PIN9
2) CHANGE R465 CAP SIZE FROM 0603 TO 0805
3) BOM OPTION FROM NO STUFF CHANGE TO SUPERCAP

09/24/2004

1) CHANGE R465 FROM MF 1/16W TO FF 1/10W
2) ADD R880 AND R871 (0 OHM;BOM_OPTIOM;FOR SUPERCAP AND BACKUP BATTERY SWITCH)
3) ADD U60 (LIS3L02AQ;ST SENSOR)
4) ADD R881 (10K OHM) ,R882 (10K OHM), R883 (10K OHM)
5) ADD C937 (0.1UF,10V,20%,0402)
6) ADD BOM_OPTION (KIONIX_ACCEL AND ST_ACCEL)

10/04/2004

1) CHANGE TEST POINT FUNC_TEST=NO FOR FUNC_TP_WRONG_SIDE.LOG
2) ADD NO_TEST=YES FOR NOTP.LOG(MMM_PIC_AN2_PD,MMM_PIC_AN3_PU)

10/05/2004

1) ADD R850 (0 OHM)

10/15/2004

1) REPLACE BOOT BANGER EEPROM U32 WITH 32KX M24256B FUNC_TP_WRONG_SIDE.LOG

12/16/2004

1) SCHEMATIC RELEASE FOR PRODUCTION

04/27/2005 REV.E

1) ADD LEAD FREE PHOTO SENSOR (385-0053)
2) ADD 337S3094 AND 337S3131

06/20/2005 REV.F

1) ADD LEAD FREE PHOTO SENSOR (385-0053)

08/25/2005 REV.G

1) ADDED 337S3216 (IC,A7PM,R1.5,1.67GHZ,1.3V,25W) AS OPTION
2) REPLACED 341S1561 (BOOTROM 4.91.F1) WITH 341S1793 (BOOTROM 4.9.1.F3)
3) ADDED LABEL WITH EEE:U3Y

REVISION HISTORY(1 OF 1)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
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*** Signal Cross-Reference for the entire design ***

Signal	References
+1_0V_MARVELL	28D2< 39B3>
+1_5V_AGP	12C5< 12D1< 12D4< 15D6< 16C8< 18C6< 18D6< 19A8< 19B4<> 19D5<> 21B8< 21D6< 39C3>
+1_5V_AGP_GPU	21C5< 39C3>
+1_5V_AGP_NECK	19B4<> 39B3>
+1_5V_GPU_VDD15	19D3< 39C3>
+1_5V_INTREPID_PLL	8D6< 12D4< 12D8< 14D6<> 39D3>
+1_5V_INTREPID_PLL1	14C3< 39D3>
+1_5V_INTREPID_PLL2	14D3< 39D3>
+1_5V_INTREPID_PLL3	14D3< 39D3>
+1_5V_INTREPID_PLL4	14D3< 39D3>
+1_5V_INTREPID_PLL5	12D3< 39D3>
+1_5V_INTREPID_PLL6	12D6< 39D3>
+1_5V_INTREPID_PLL7	8D5< 39D3>
+1_5V_INTREPID_PLL8	14D3< 39D3>
+1_5V_LDO	36D8< 39D6>
+1_5V_MAIN	39D6>
+1_5V_SLEEP	39D6>
+1_5V_SLEEP_NECK	21A3<> 39B3>
+1_5V_SLEEP_VIN	36D8<> 39D6>
+1_8V_ATI_PVDD	19C5<> 21B6< 21B6< 21D6<> 39C3>
+1_8V_ATI_TPVDD	21D2<>
+1_8V_DVO_F	21B2<
+1_8V_GPU	18A7< 19C8< 20A8< 21A2< 21A6< 21B1< 21B6< 21C8< 21D6< 21D8< 39C3>
+1_8V_GPU_AVDD	21D5< 39C3>
+1_8V_GPU_AVDDQ	21D4< 21D7< 39C3>
+1_8V_GPU_MEMPLL	21B5< 39C3>
+1_8V_GPU_PLL	21D5< 39C3>
+1_8V_GPU_PNLIO	21A5< 39C3>
+1_8V_GPU_PNLPLL	21B5< 39C3>
+1_8V_GPU_TP_PLL	21B4< 21D1<
+1_8V_GPU_VDDDI	21C7< 21D4< 39C3>
+1_8V_MAIN	39D6> 40A2>
+1_8V_PVDD_NECK	19B5<> 39B3>
+1_8V_SLEEP	39D6>
+1_8V_SLEEP_NECK	21A3<> 39B3>
+1_95V_FW_DVDD	29C4< 29C7<> 29D5< 39A3>
+1_95V_FW_DVDD_PORT1	29D6< 39A3>
+1_95V_FW_DVDD_RX0	29C5< 39A3>
+1_95V_FW_DVDD_TX0	29C5< 39A3>
+1_95V_FW_PLL400VDD	29D5< 39A3>
+1_95V_FW_PLL500VDD	29D5< 39A3>
+1_95V_FW_PLLVDD	29D5< 29D7<> 39A3>
+2_5V_CG_MAIN	14C6< 39A3>
+2_5V_GPU	21A8< 21B6< 21D3< 21D7< 21D8< 39B3>
+2_5V_GPU_A2VDD	21D4< 21D7< 39C3>
+2_5V_GPU_PNLIO	21A5< 39C3>
+2_5V_INTREPID	9A8< 10D3< 10D5< 10D7< 10D8< 15D7< 16B8< 39D3>
+2_5V_MAIN	39D6>
+2_5V_MARVELL	28B8< 28C4<> 39B3>
+2_5V_MARVELL_AVDD	28C4< 39B3>
+2_5V_REG	30B6<
+2_5V_REG_F	30A7<>
+2_5V_SLEEP	39D6>
+2_5V_SLEEP_NECK1	19C4<> 39B3>
+2_5V_SLEEP_NECK2	21A3<> 39B3>
+2_8V_GPU_LVDS_LDO	21A6<>
+3V_ATI_OSC_SLEEP	18D2< 39C3>
+3V_ATI_SS	18B2< 39C3>
+3V_CG_PLL_MAIN	14C6< 39A3>
+3V_FW	29A3< 29D7<> 30B7<> 30D5< 39A3>
+3V_FW_AVDD	29C6< 39A3>
+3V_FW_AVDD_PORT0	29C6< 39A3>
+3V_FW_AVDD_PORT1	29C6< 39A3>
+3V_FW_AVDD_PORT2	29D6< 39A3>
+3V_FW_ESD	30B3<> 30B5< 30D2<> 39B3>
+3V_FW_ESD_ILIM	30D4< 39B3>
+3V_FW_ESD_R	30B6<
+3V_FW_UF	29D7<> 39A3>
+3V_GPU	12D1< 18B8< 18C5< 18C7< 18D6< 19C4< 19C5< 19C7< 19D8< 21A7< 21B1< 21B8< 39C3>
+3V_GPU_FLT	21B2< 39C3>
+3V_HALL_EFFECT	23B6<> 39B6> 40C4>
+3V_INTREPID_USB	14C3< 39D3>
+3V_LCD	22B4<> 39B6>
+3V_LCD_SW	22A4<> 39B6>
+3V_MAIN	23A7< 39D6>
+3V_MAIN_CONN	23A6<>
+3V_NEC_VDD	27D7< 27D7< 39A3>
+3V_PMU	39D6> 40A2>
+3V_PMU_AVCC	26B1< 31B6< 31D5<> 39C6>
+3V_PMU_ESR	33A2< 39C6>
+3V_PMU_RESET	31C7< 35A3<>
+3V_SLEEP	20D5< 20D8< 23A5< 39D6>
+3V_SLEEP_AUDIO	26D6<> 26D7<>
+3V_SLEEP_NECK	21A3<> 39B3>
+3V_SLP_OK_L	34B4<>
+3V_SLP_ON	34A5<>
+4_6V_BU	33A3<> 34B6< 39C6>
+4_85V_ESR	33A4< 39C6>
+4_85V_RAW	31B4< 33A4<> 39C6>
+5V_DDC_SLEEP	22D3<> 22D5<> 39B6> 40A2>
+5V_DDC_SLEEP_UF	22D6< 39B6>
+5V_HD_SLEEP	25D1<> 34A7<> 39C6>
+5V_INV_SW	22B2<> 39B6> 40D1>
+5V_INV_UF_SW	22B2<> 39B6>
+5V_MAIN	39D6>
+5V_MAIN_AUDIO	26D7<>
+5V_MAIN_AUDIO_0	26D7<>
+5V_MAIN_CONN	39B6>
+5V_SLEEP	23A4< 39D6>
+5V_SLEEP_MM3120	23A4<>
+5V_SOUND_SLEEP	39B6>
+5V_TPAD	23B7<>
+5V_TPAD_FB	23B6<>
+5V_TPAD_SLEEP	40C4>
+12_8V_INV	22B1<> 39B6> 40A2>
+24V_PBUS	39D6> 40B2>
+24V_PBUS_CONN	33A8<>
+ADAPTER	32D8<> 33B7< 39D6>
+ADAPTER_ILIM	33B6<> 39C6>
+ADAPTER_OR_BATT	33A5<> 39C6>
+ADAPTER_SENSE	32D5<> 39C6>
+ADAPTER_SW	32D6<> 39C6>
+BATT	39D6>
+BATT_14V_FUSE	32D1<> 39C6>
+BATT_24V_FUSE	32B1< 32D2<> 39C6>
+BATT_ISNS_P	24A5<>
+BATT_POS	32A4<> 39C6> 40C3>
+BATT_RSNS	32B2< 39C6>
+BATT_VSNS	32A4< 39C6>
+FAN1_PWR	26A4<>
+FAN2_PWR	26A3<>
+FW_FUSE	30D7<> 39A3>
+FW_PWR_CTRL	30B7<>
+FW_PWR_OR	29B8< 29D8<> 30D5<> 39A3>
+FW_PWR_OR_F	30B7<>
+FW_PWR_OR_GATE	30B8<>
+FW_PWR_OR_GATE_L	30B8<
+FW_PWR_PORTA	30B5< 39A3>
+FW_SW	30D5<> 39A3>
+FW_VP0	30C2<> 39A3>
+FW_VP1	30A3<> 39A3>
+GPU_MCLK	21C7< 21D4< 39C3>
+GPU_MEM	18A6< 18B8< 21B4< 21B7< 21C6< 21C8< 21D2< 39C3>
+GPU_MEMCORE	21C5< 39C3>
+GPU_VDD15_NECK	19B5<> 39B3>
+GPU_VDD15_UF	19B5<> 19D4<> 39C3>
+HD_LOGIC_SLEEP	25C2<> 39C6>
+PBUS	39D6> 40B2>
+PPBATT_ISNS_N	24A4<> 40B4>
+VCC_CBUS_SW	17B1< 17B2< 17D2<> 39D3>
+VPP_CBUS_SW	17B1< 17B2< 17D2<> 39C3>
1V20_REF	32C7< 33C8< 39D1>
1V65_REF	32A5<
1_5V_2_5V_OK	36C5> 39B1>
1_5V_BOOST	36C6<> 39C1>
1_5V_BST	36C5<> 39C1>
1_5V_DH	36C5<> 39C1>
1_5V_DL	36B5<> 39C1>
1_5V_FB	36B5< 36B7< 39C1>
1_5V_ILIM	36C5<> 39C1>
1_5V_LX	36B5<> 39C1>
1_5V_SLEEP_EN_L	36C7<> 36D7<>
1_8V_SLEEP_PWREN_L	36A3<>
1_8V_SW	36A5<> 39A1>
1_8V_VFB	39A1>
2_5V_BOOST	36C4<> 39D1>
2_5V_BST	36C4<> 39D1>
2_5V_DH	36C4<> 39D1>
2_5V_DL	36B4<> 39D1>
2_5V_ILIM	36C5<> 39C1>
2_5V_LX	36B4<> 39D1>
2_5V_SLEEP_PWREN_L	36C2<>
2_34V_REF	31A4<
3V_5V_OK	23A7< 34B4<> 36A8<> 36D6<
3V_5V_OK_G	23B8<
3V_5V_OK_INV	36A8<>
3V_5V_OK_L	23B8<
3V_BG	34C4<>
3V_BOOST	34C4<>
3V_BOOST_ESR	34D3<>
3V_ITH	34C4<>
3V_ITH_RC	34C3<
3V_PMU_VTAP	33B3<
3V_RSNS	34D2< 39D1>
3V_RUNSS	34C4<
3V_SLEEP_PWREN_L	34A3<>
3V_SNSM	34C4< 38A2>
3V_SNSP	34C4< 38A2>
3V_SW	34C4<> 39D1>
3V_TG	34D4<>
3V_VOSNS	34C4<>
5V_BG	34C5<>
5V_BOOST	34C5<>
5V_BOOST_ESR	34D6<>
5V_HD_PWREN	34A8<>
5V_ITH	34C5<>
5V_ITH_RC	34C6<
5V_RSNS	34D7< 39D1>
5V_RUNSS	34C5<
5V_SLEEP_PWREN	34A8<>
5V_SNSM	34C5< 38A2>
5V_SNSP	34C5< 38A2>
5V_SW	34C5<> 39D1>
5V_TG	34C5<>
5V_VOSNS	34C5<>
1625_BG	33C5<>
1625_BST	33C5<
1625_BST_ESR	33C5<>
1625_COMP	32D2< 33C6<
1625_DIV	33C8<
1625_ENABLE	33D7<>
1625_ENABLE_L	33D7<>
1625_EXTVCC	33D5<> 39D1>
1625_FCB	33C6<
1625_INTVCC	33C5<> 39D1>
1625_RUNSS	33C6<
1625_SGND	33B7<> 39D1>
1625_TG	33C5<>
1625_VFB	33B5<>
1625_VIN	33C6< 39D1>
1625_VSW	33C4<> 39D1>
1772_ACIN	32B5<
1772_ACOK_L	32B5<> 32C4<>
1772_BST	32B4<>
1772_BST_ESR	32C3<
1772_CCI	32B5<>
1772_CCS	32B5<
1772_CCV	32B5<>
1772_CCV_RC	32B5<
1772_CELLS	32B4<
1772_CLS	32A4<
1772_CSIN	32B4<> 38A2>
1772_CSIP	32B4<> 38A2>
1772_CSSN	32C5< 38A2>
1772_CSSP	32C5< 38A2>
1772_DCIN	32B5< 39C6>
1772_DHI	32B4<>
1772_DLO	32B4<>
1772_DLOV	32B4<> 39C6>
1772_GND	32A5<> 39C6>
1772_ICHG	32B5<>
1772_ICTL	32B5<>
1772_IINP	32B5<
1772_LDO	32C4<> 39C6>
1772_LX	32B4<> 39C6>
1772_REF	32B5<>
1772_VCTL	32B5<
1778_BG	19A5<> 39B1>
1778_BST	19A5<> 39B1>
1778_BST_RC	19A4<> 39B1>
1778_FCB	19A5< 39B1>
1778_GND	19A5< 19A7<> 39B1>
1778_ION	19A5< 39B1>
1778_ITH	19A5<> 39B1>
1778_ITH_RC	19A7< 39B1>
1778_SHDN_L	19A6<
1778_SHDN_L_D3COLD	19A7<>
1778_TG	19A5<> 39B1>
1778_VCC	19A5<> 39B1>
1778_VFB	19A2< 19A5< 39B1> 40A1>
1778_VIN	19A5< 39B1>
1778_VRNG	19A5< 39B1>
3405_MODE	28D5<
3405_VFB	28D4<>
3707_FCB	34C5<
3707_FSET	34C5<
3707_INTVCC	34D4<> 39D1>
3707_SGND	34B5<> 39D1>
3707_STBY	34C5<>
A29_CLS_ADJ	32A5<>
A29_CURRENT_ADJ	32C4<>
A29_DETECT	31A2< 32A5<> 32C4<>
A29_DET_L	31A3<
AB_SEL_LOW	35A6<>
AC_DET	31A4<
AC_DIV	32C8<
AC_ENABLE_GATE	32D6<>
AC_ENABLE_L	32C6<>
AC_GTR_18V	32C4<>
AC_IN	28B8<> 30C8< 31B3< 32C5<> 32C7<>
AC_IN_FW_CNTL	30C8<>
AC_IN_L	31B8<> 32C2<> 32C6<>
AC_IN_L_RC	32C2<>
ADAPTER_DET	31A4< 32D8<> 40C2>
ADAPTER_I_REG	32D3<>
ADT7460_TACH3_TP	26B3<
ADT7467_ADR_EN_L	26B3<>
ADT7467_THERM	23A8< 26B2<> 26B3<
ADT7467_VCC	26C3<
ADT7467_VCORE_MON	5C8<> 26B4<
AGP8X_DET_PU	18C6<>
AGP_AD<0>	12D2<> 18C7<>
AGP_AD<15..0>	38D5>
AGP_AD<1>	12C2<> 18C7<>
AGP_AD<2>	12C2<> 18C7<>
AGP_AD<3>	12C2<> 18C7<>
AGP_AD<4>	12C2<> 18C7<>
AGP_AD<5>	12C2<> 18C7<>
AGP_AD<6>	12C2<> 18C7<>
AGP_AD<7>	12C2<> 18C7<>
AGP_AD<8>	12C2<> 18C7<>
AGP_AD<9>	12C2<> 18C7<>
AGP_AD<10>	12C2<> 18C7<>
AGP_AD<11>	12C2<> 18C7<>
AGP_AD<12>	12C2<> 18C7<>
AGP_AD<13>	12C2<> 18C7<>
AGP_AD<14>	12C2<> 18C7<>
AGP_AD<15>	12C2<> 18C7<>
AGP_AD<16>	12C2<> 18C7<>
AGP_AD<31..16>	38D5>
AGP_AD<17>	12C2<> 18C7<>
AGP_AD<18>	12C2<> 18C7<>
AGP_AD<19>	12C2<> 18C7<>
AGP_AD<20>	12C2<> 18C7<>
AGP_AD<21>	12C2<> 18C7<>
AGP_AD<22>	12C2<> 18C7<>
AGP_AD<23>	12C2<> 18C7<>
AGP_AD<24>	12C2<> 18C7<>
AGP_AD<25>	12C2<> 18D7<>
AGP_AD<26>	12C2<> 18D7<>
AGP_AD<27>	12B2<> 18D7<>
AGP_AD<28>	12B2<> 18D7<>
AGP_AD<29>	12B2<> 18D7<>
AGP_AD<30>	12B2<> 18D7<>
AGP_AD<31>	12B2<> 18D7<>
AGP_AD_STB<0>	12A2<> 12B2< 18D6<> 38D5>
AGP_AD_STB<1>	12A2<> 12B2< 18D6<> 38D5>
AGP_AD_STB_L<0>	12A2<> 12B2< 18D6<> 38D5>
AGP_AD_STB_L<1>	12A2< 12A2<> 18D6<> 38D5>
AGP_ATI_RESET_L	18B7<
AGP_ATI_VREF	18B7<
AGP_ATI_VREFG	18B7<
AGP_BUSY_L	12C4<> 12D2< 18D6>
AGP_CBE<0>	12B2<> 18B7<>
AGP_CBE<1..0>	38D5>
AGP_CBE<1>	12B2<> 18B7<>
AGP_CBE<2>	12B2<> 18B7<>
AGP_CBE<3..2>	38D5>
AGP_CBE<3>	12B2<> 18C7<>
AGP_DEVSEL_L	12B2<> 12C2< 18B7<> 38D5>
AGP_FRAME_L	12B2<> 12C2< 18B7<> 38D5>
AGP_GNT_L	12C2< 12D2<> 18B7< 38D5>
AGP_INT_L	14B5<> 18B7<>
AGP_IRDY_L	12B2<> 12C2< 18B7<> 38D5>
AGP_PAR	12B2<> 18B7> 38D5>
AGP_PIPE_L	12A2<> 12B2<
AGP_RBF_L	12A2<> 12C2< 18C6> 38D5>
AGP_REQ_L	12C2< 12D2<> 18B7<> 38D5>
AGP_SBA<0>	12B2< 18C6>
AGP_SBA<7..0>	38D5>
AGP_SBA<1>	12B2<> 18C6>
AGP_SBA<2>	12B2<> 18C6>
AGP_SBA<3>	12B2<> 18C6>
AGP_SBA<4>	12B2<> 18C6>
AGP_SBA<5>	12B2<> 18C6>
AGP_SBA<6>	12B2<> 18C6>
AGP_SBA<7>	12B2<> 18C6<>
AGP_SB_STB	12B2< 12B2<> 18C6<> 38D5>
AGP_SB_STB_L	12A2< 12A2<> 18C6<> 38D5>
AGP_ST<0>	12A2<> 18C6<
AGP_ST<1>	12A2<> 18C6<
AGP_ST<2>	12A2<> 18C6<
AGP_STOP_L	12B2<> 12C2< 18B7<> 38D5>
AGP_STP_L	18C6<
AGP_SUS_STAT_L_PU	18C6<
AGP_TRDY_L	12B2<> 12C2< 18B7<> 38D5>
AGP_WBF_L	12A4<> 12B2< 18B7>
AIRPORT_CLKRUN_L	25C6<> 40C1>
AIRPORT_IDSEL	25C5<> 40B1>
AIRPORT_PCI_GNT_L	12D7<> 25D5<> 40C4>
AIRPORT_PCI_INT_L	14B5<> 14D7< 25D5<> 40C4>
AIRPORT_PCI_REQ_L	12A7< 12D7<> 25D6<> 40D4>
AIRPORT_PME_L_TP	25D5<>
AMP_CONTROL	26C5<> 26D4<>
ATI_AGP_FBSKEW<0>	19C2< 19C7<>
ATI_AGP_FBSKEW<1>	19C2< 19C7<>
ATI_BUS_CFG<0>	19B2< 19C7<>
ATI_BUS_CFG<1>	19B2< 19C7<>
ATI_BUS_CFG<2>	19B2< 19C7<>
ATI_CLK27M_IN	18C1< 19B7<
ATI_CLK27M_OSC	18D2<
ATI_CLK27M_OSC_SS	18B2< 18D1<
ATI_DBI_HI_PU	18C6<>
ATI_DBI_LO_PU	18C6<>
ATI_DVOVMODE	21A2<
ATI_GPIO7	19C7<> 20D7<
ATI_GPIO8_PD	19C7<>
ATI_GPIO9_SPN	19C7<>
ATI_GPIO10_SPN	19C7<>
ATI_GPIO11_SPN	19C7<>
ATI_GPIO12_SPN	19C7<>
ATI_GPIO13_SPN	19C7<>
ATI_HSYNC	19D5<> 22C8<
ATI_MEMTEST	18A6<>
ATI_MEMVMODE0	18A7<
ATI_MEMVMODE1	18A7<
ATI_OSC_OE	18D3<
ATI_PVDD_BYP	21D6<>
ATI_R2SET	19D6<>
ATI_RSET	19D6<>
ATI_RSTB_MSK	18C6<>
ATI_SSCLK_IN	18B1< 19B7<>
ATI_SSCLK_UF	18B1<>
ATI_TESTEN	19B7<
ATI_TMDS_CLKN	19B7> 20D5<
ATI_TMDS_CLKP	19B7> 20D5<
ATI_TMDS_DN<0>	19B7> 20D5<
ATI_TMDS_DN<1>	19B7> 20D3<
ATI_TMDS_DN<2>	19B7> 20D3<
ATI_TMDS_DP<0>	19B7> 20D5<
ATI_TMDS_DP<1>	19B7> 20D3<
ATI_TMDS_DP<2>	19B7> 20D3<
ATI_TPVDD_BYP	21D1<>
ATI_VSYNC	19D5<> 22C8<
ATI_X1CLK_SKEW<0>	19C2< 19C7<>
ATI_X1CLK_SKEW<1>	19B2< 19C7<>
AUDIO_EXT_MCLK_SEL	26C7<> 26D7<
AUDIO_LI_DET_L	14B5<> 26C5<>
AUDIO_LI_OPTICAL_PLUG_L	26C5<> 26D7<
AUDIO_LI_SPDIF_PLUG_L	14B5<> 14B7< 26D8<
AUDIO_LO_DET_L	14B5<> 26D5<>
AUDIO_LO_MUTE_L	26C5<> 26C7<>
AUDIO_LO_OPTICAL_PLUG_L	26D5<> 26D7<
AUDIO_LO_SPDIF_PLUG_L	14B5<> 14C7< 26D8<
AUDIO_MCLK_SEL	14B5<> 14C7< 26D8<
AUDIO_SPDIF_GPO0	14B5<> 14B7<
AUDIO_SPDIF_RESET	14C5<>
AUDIO_SPDIF_RESET_C	14C6<> 14D7< 26B6<
AUDIO_SPDIF_RESET_L	14B5<> 14B7< 14C5<> 14D6<
AUDIO_SPKR_MUTE_F	26C5<> 26C7<
BATTV_HIGH	32B7<>
BATTV_LOW	32B8<>
BATT_14PBUS_EN	32C1<>
BATT_14V_GATE	32C1<>
BATT_24PBUS_EN	32C2<>
BATT_24V_GATE	32C1<>
BATT_CLK	32A4<> 40C3>
BATT_DATA	32A4<> 40C3>
BATT_DIV	32A5<
BATT_ISNS_OUT	24A4<>
BATT_ISNS_R	24A3<>
BATT_LOW	32A6<>
BATT_LOW_L	32B6<>
BATT_NEG	32A4<> 39C6> 40C3>
BBANG_HRESET_L	6A2< 6B3<> 40C1>
BBANG_JTAG_TCK	6A4< 6B1<> 6D2<
BBANG_TCK_EN	6A4<
BB_EEPR_ADDR0	6D3<
BB_EEPR_ADDR1	6D3<
BB_EEPR_ADDR2	6D3<
BB_MISO	6B3<> 6D2<
BB_MOSI	6B3<> 6D2<
BB_RESET_L	6C3<
BB_SCK	6B3<> 6D2<
BCKFD_PROT_EN_L	32C6<>
BCKFD_PROT_GATE	32D6<>
BFR_TDO	6C1<> 6D2<
BRIGHT_PWM	22A1<> 40A7>
BRIGHT_PWM_UF	22A2<>
BT_USB_DM	14C1< 25B2<> 38B2> 40B6>
BT_USB_DP	14C1< 25B2<> 38B2> 40B6>
CAPSLOCK_LED_L	31C7<
CBUS_ADDR<0>	17B1< 17B4>
CBUS_ADDR<1>	17B1< 17B4>
CBUS_ADDR<2>	17B1< 17B4>
CBUS_ADDR<3>	17B1< 17B4>
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CBUS_ADDR<6>	17B1< 17B4>
CBUS_ADDR<7>	17B1< 17B4>
CBUS_ADDR<8>	17B1< 17B4>
CBUS_ADDR<9>	17B1< 17B4>
CBUS_ADDR<10>	17B4> 17C1<
CBUS_ADDR<11>	17B1< 17B4>
CBUS_ADDR<12>	17B1< 17B4>
CBUS_ADDR<13>	17B1< 17B4>
CBUS_ADDR<14>	17B1< 17B4>
CBUS_ADDR<15>	17B1< 17B4>
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CBUS_ADDR<17>	17B2< 17B4>
CBUS_ADDR<18>	17B2< 17B4>
CBUS_ADDR<19>	17B2< 17B4>
CBUS_ADDR<20>	17B2< 17B4>
CBUS_ADDR<21>	17B2< 17B4>
CBUS_ADDR<22>	17A4> 17B2<
CBUS_ADDR<23>	17A4> 17B2<
CBUS_ADDR<24>	17A4> 17B2<
CBUS_ADDR<25>	17A4> 17B2<
CBUS_ADDR_16_UF	17B5<>
CBUS_BVD1_L	17B2< 17C4<
CBUS_BVD2_L	17B2< 17C4<
CBUS_CE1_L	17C1< 17C4<
CBUS_CE2_L	17B4> 17C2<
CBUS_DATA<0>	17A1< 17A4<>
CBUS_DATA<1>	17A1< 17A4<>
CBUS_DATA<2>	17A1< 17A4<>
CBUS_DATA<3>	17A4<> 17C1<
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CBUS_DATA<5>	17A4<> 17C1<
CBUS_DATA<6>	17A4<> 17C1<
CBUS_DATA<7>	17A4<> 17C1<
CBUS_DATA<8>	17A2< 17A4<>
CBUS_DATA<9>	17A2< 17A4<>
CBUS_DATA<10>	17A2< 17A4<>
CBUS_DATA<11>	17A4<> 17C2<
CBUS_DATA<12>	17A4<> 17C2<
CBUS_DATA<13>	17A4<> 17C2<
CBUS_DATA<14>	17A4<> 17C2<
CBUS_DATA<15>	17A4<> 17C2<
CBUS_DET_1_L	17C2< 17C4< 40B8>
CBUS_DET_2_L	17A2< 17C4< 40B8>
CBUS_INPACK_L	17B2< 17B4<
CBUS_INT_L	14B5<> 14B7< 17A7<>
CBUS_IORD_L	17B2< 17C4>
CBUS_IOWR_L	17B2< 17C4>
CBUS_MFUNC1_PD	17A7<> 17A7<
CBUS_MFUNC2_PD	17A7<> 17A7<
CBUS_MFUNC3_PD	17A7<> 17A7<
CBUS_MFUNC4_PD	17A7<> 17A7<
CBUS_MFUNC5_PD	17A7<> 17A7<
CBUS_MFUNC6_PD	17A7< 17A7<>
CBUS_OE_L	17C1< 17C4>
CBUS_PCI_GNT_L	12D7<> 17A7<
CBUS_PCI_IDSEL	17B7<
CBUS_PCI_PERR_L	17B7<> 17D7<
CBUS_PCI_REQ_L	12A7< 12D7<> 17A7>
CBUS_PCI_RESET_L	17A7<
CBUS_PCI_SERR_L	17B7> 17D7<
CBUS_READY	17B1< 17C4<
CBUS_REG_L	17B2< 17C4>
CBUS_RESET_L	17B2< 17C4>
CBUS_SUSPEND_PU	17A7< 17D7<
CBUS_VCCD0_L	17C4<>
CBUS_VCCD1_L	17C4<>
CBUS_VPPD0	17C4<>
CBUS_VPPD1	17C5<>
CBUS_VS1	17B2< 17C4<>
CBUS_VS2	17B2< 17C4<>
CBUS_WAIT_L	17B2< 17B4<
CBUS_WE_L	17B1< 17C4>
CBUS_WP_L	17A1< 17B4<
CG_ADDRSEL	14B7<
CG_CLKOUT	14B6<>
CG_FSEL	14B7< 14C5<
CG_LOCK	14B7<>
CG_RESET_L	14B7<
CG_SYSCLK_EN	14A6< 14B7<
CHARGE_DISABLE	32A7<>
CHARGE_LED_L	31C6< 31D7< 32D8<> 40D2>
CHGND1	39A6>
CHGND2	39A6>
CHGND3	39A6>
CHGND4	39A6> 40B6>
CHGND5	39A6>
CHGND6	39A6>
CLK10M_PMU_XIN	31B6<
CLK10M_PMU_XOUT	31B6<
CLK10M_PMU_XOUT_UF	31A7<
CLK18M_INT_EXT	14A6<> 37B1>
CLK18M_INT_XIN	14A5< 37B1>
CLK18M_INT_XOUT	14A5<> 37B1>
CLK18M_XTAL_IN	14A5< 37B1>
CLK25M_ENET_XIN	28A7< 37B1>
CLK25M_ENET_XOUT	28A7<> 37B1>
CLK25M_XTAL_IN	28A7<
CLK27M_GPU_XIN	37B1>
CLK27M_GPU_XOUT	37B1>
CLK27M_XTAL_IN	37B1>
CLK32K_PMU_XIN	31B3<>
CLK32K_PMU_XOUT	31B3<>
CLK32K_PMU_XOUT_UF	31B2<>
CLK33M_AIRPORT	12D8< 25D5<> 37C1> 40B1>
CLK33M_AIRPORT_UF	12C7<> 37C1>
CLK33M_CBUS	12D8< 17A7< 37C1>
CLK33M_CBUS_UF	12C7<> 37C1>
CLK33M_USB2	12C8< 27B7< 37C1>
CLK33M_USB2_UF	12C7<> 37C1>
CLK66M_AGP_15V_TP	12C4>
CLK66M_GPU_AGP	12C8< 18B7< 37C1>
CLK66M_GPU_AGP_UF	12C7<> 37C1>
CLKENET_LINK_GBE_REF	13C5< 28C8< 37B1>
CLKENET_LINK_GTX	13C5<> 37A1>
CLKENET_LINK_RX	13D5< 28C8< 37B1>
CLKENET_LINK_TX	13D5< 28D8< 37A1>
CLKENET_PHY_GBE_REF	28C7<> 37B1>
CLKENET_PHY_GTX	13C6< 28C7< 37A1>
CLKENET_PHY_RX	28C7<> 37B1>
CLKENET_PHY_TX	28D7<> 37B1>
CLKFW_LINK_LCLK	13C3<> 37A1>
CLKFW_LINK_PCLK	13C3<> 29C3< 37A1>
CLKFW_PHY_LCLK	13C2< 29B8< 37A1>
CLKFW_PHY_PCLK	29B4> 29C3< 37A1>
CLKLVDS_LN	19B5> 22A4<> 38C2> 40B7>
CLKLVDS_LP	19B5> 22A4<> 38C2> 40B7>
CLKLVDS_UN	19B5> 22A4<> 38C2> 40B7>
CLKLVDS_UP	19B5> 22A4<> 38C2> 40A7>
COMM_DTR_L	14C2> 26D1<> 40B2>
COMM_GPIO_L	14C2<> 26D2<> 40C2>
COMM_RESET_L	14C5<> 26D3<> 40C4>
COMM_RING_DET_L	14B5<> 14C7< 26C2<> 31C6<> 40C4>
COMM_RTS_L	14C2> 26D1<> 40B2>
COMM_RXD	14C2<> 26D1<> 40B2>
COMM_SHUTDOWN	14C5<> 26D3<> 40C4>
COMM_TRXC	14C2<> 26D2<> 40C2>
COMM_TXD_L	14C2<> 26D2<> 40C2>
COMP_DISABLE	22C2<>
COMP_ENABLE	22C1<>
COMP_RC	33C6<
CPU_AACK_L	5A7< 8B6<> 8C2< 37D5>
CPU_ADDR<0>	5C7<> 8D6<>
CPU_ADDR<0..31>	37D5>
CPU_ADDR<1>	5C7<> 8D6<>
CPU_ADDR<2>	5C7<> 8D6<>
CPU_ADDR<3>	5C7<> 8D6<>
CPU_ADDR<4>	5C7<> 8D6<>
CPU_ADDR<5>	5C7<> 8C6<>
CPU_ADDR<6>	5C7<> 8C6<>
CPU_ADDR<7>	5C7<> 8C6<>
CPU_ADDR<8>	5C7<> 8C6<>
CPU_ADDR<9>	5C7<> 8C6<>
CPU_ADDR<10>	5B7<> 8C6<>
CPU_ADDR<11>	5B7<> 8C6<>
CPU_ADDR<12>	5B7<> 8C6<>
CPU_ADDR<13>	5B7<> 8C6<>
CPU_ADDR<14>	5B7<> 8C6<>
CPU_ADDR<15>	5B7<> 8C6<>
CPU_ADDR<16>	5B7<> 8C6<>
CPU_ADDR<17>	5B7<> 8C6<>
CPU_ADDR<18>	5B7<> 8C6<>
CPU_ADDR<19>	5B7<> 8C6<>
CPU_ADDR<20>	5B7<> 8C6<>
CPU_ADDR<21>	5B7<> 8C6<>
CPU_ADDR<22>	5B7<> 8C6<>
CPU_ADDR<23>	5B7<> 8C6<>
CPU_ADDR<24>	5B7<> 8C6<>
CPU_ADDR<25>	5B7<> 8C6<>
CPU_ADDR<26>	5B7<> 8C6<>
CPU_ADDR<27>	5B7<> 8C6<>
CPU_ADDR<28>	5B7<> 8C6<>
CPU_ADDR<29>	5B7<> 8C6<>
CPU_ADDR<30>	5B7<> 8C6<>
CPU_ADDR<31>	5B7<> 8B6<>
CPU_ARTRY_L	5A7<> 8B6<> 8D2< 37D5>
CPU_AVDD	5C3< 39D3>
CPU_AVDD_ADJ	5C2<>
CPU_AVDD_SHDN_L	5C3<>
CPU_AVDD_VIN	5C4<
CPU_AVDD_VOUT	5C3<>
CPU_BG_L	5C7< 8C2< 8D6<> 37D5>
CPU_BR_L	5C7> 8D2< 8D6< 37D5>
CPU_BUS_VSEL	5C4< 7A6<
CPU_CHKSTP_OUT_L	5B4<> 5C2< 40D8>
CPU_CHKS_L	5A4< 5D2<
CPU_CI_L	5A7> 8B6<> 37D5>
CPU_CLKOUT_SPN	5C4>
CPU_CLK_EN	8A6< 31C4<>
CPU_DATA<0>	6D8<> 8D4<>
CPU_DATA<0..31>	37D5>
CPU_DATA<1>	6D8<> 8D4<>
CPU_DATA<2>	6D8<> 8D4<>
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CPU_DATA<5>	6D8<> 8D4<>
CPU_DATA<6>	6D8<> 8D4<>
CPU_DATA<7>	6D8<> 8D4<>
CPU_DATA<8>	6D8<> 8D4<>
CPU_DATA<9>	6D8<> 8D4<>
CPU_DATA<10>	6C8<> 8D4<>
CPU_DATA<11>	6C8<> 8D4<>
CPU_DATA<12>	6C8<> 8C4<>
CPU_DATA<13>	6C8<> 8C4<>
CPU_DATA<14>	6C8<> 8C4<>
CPU_DATA<15>	6C8<> 8C4<>
CPU_DATA<16>	6C8<> 8C4<>
CPU_DATA<17>	6C8<> 8C4<>
CPU_DATA<18>	6C8<> 8C4<>
CPU_DATA<19>	6C8<> 8C4<>
CPU_DATA<20>	6C8<> 8C4<>
CPU_DATA<21>	6C8<> 8C4<>
CPU_DATA<22>	6C8<> 8C4<>
CPU_DATA<23>	6C8<> 8C4<>
CPU_DATA<24>	6C8<> 8C4<>
CPU_DATA<25>	6C8<> 8C4<>
CPU_DATA<26>	6C8<> 8C4<>
CPU_DATA<27>	6C8<> 8C4<>
CPU_DATA<28>	6C8<> 8C4<>
CPU_DATA<29>	6C8<> 8C4<>
CPU_DATA<30>	6C8<> 8C4<>
CPU_DATA<31>	6C8<> 8C4<>
CPU_DATA<32>	6C8<> 8C4<> 8D8<
CPU_DATA<32..63>	37D5>
CPU_DATA<33>	6C8<> 8C4<> 8D8<
CPU_DATA<34>	6C8<> 8C4<> 8D8<
CPU_DATA<35>	6C8<> 8C4<> 8D8<
CPU_DATA<36>	6B8<> 8C4<> 8D8<
CPU_DATA<37>	6B8<> 8C4<> 8D8<
CPU_DATA<38>	6B8<> 8B4<> 8D8<
CPU_DATA<39>	6B8<> 8B4<> 8D8<
CPU_DATA<40>	6B8<> 8B4<> 8C8<
CPU_DATA<41>	6B8<> 8B4<> 8C8<
CPU_DATA<42>	6B8<> 8B4<> 8C8<
CPU_DATA<43>	6B8<> 8B4<> 8C8<
CPU_DATA<44>	6B8<> 8B4<> 8C8<
CPU_DATA<45>	6B8<> 8B4<> 8B8<
CPU_DATA<46>	6B8<> 8B4<> 8B8<
CPU_DATA<47>	6B8<> 8B4<> 8B8<
CPU_DATA<48>	6B8<> 8A8< 8B4<>
CPU_DATA<49>	6B8<> 8A8< 8B4<>
CPU_DATA<50>	6B8<> 8A8< 8B4<>
CPU_DATA<51>	6B8<> 8A8< 8B4<>
CPU_DATA<52>	6B8<> 8A8< 8B4<>
CPU_DATA<53>	6B8<> 8A8< 8B4<>
CPU_DATA<54>	6B8<> 8A8< 8B4<>
CPU_DATA<55>	6B8<> 8A8< 8B4<>
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CPU_DATA<57>	6B8<> 8B3< 8B4<>
CPU_DATA<58>	6B8<> 8B3< 8B4<>
CPU_DATA<59>	6B8<> 8B3< 8B4<>
CPU_DATA<60>	6B8<> 8B3< 8B4<>
CPU_DATA<61>	6B8<> 8B3< 8B4<>
CPU_DATA<62>	6A8<> 8B3< 8B4<>
CPU_DATA<63>	6A8<> 8B3< 8B4<>
CPU_DBG_L	5C4< 8A4<> 8C2< 37D5>
CPU_DRDY_L	5C4> 8A4< 8C2< 37D5>
CPU_DRDY_L_UF	37D5>
CPU_DTI<0>	5C4< 8A4<>
CPU_DTI<0..2>	37D5>
CPU_DTI<1>	5C4< 8A4<>
CPU_DTI<2>	5C4< 8A4<>
CPU_EDTI	5B2< 5C4<
CPU_EMODE0_L	5A4< 7A4<
CPU_EMODE1_L	5A4< 5C2<
CPU_GBL_L	5A7<> 8B6<> 37D5>
CPU_HIT_L	5A7> 8B6< 8D2< 37D5>
CPU_HRESET_INV	7A7<>
CPU_HRESET_L	5B4< 5C2< 6A1<> 7A5< 7A8< 40C8>
CPU_L1TSTCLK	5B2< 5B4<
CPU_L2TSTCLK	5B4< 5C2<
CPU_LSSD_MODE	5B4< 5C2<
CPU_MCP_L	5B4< 5D2<
CPU_M_DM	26A7< 26B6<
CPU_M_DP	26A7< 26B6<
CPU_PLL_CFG<0>	5C4< 7D3<
CPU_PLL_CFG<1>	5C4< 7D3<
CPU_PLL_CFG<2>	5C4< 7D3<
CPU_PLL_CFG<3>	5C4< 7D3<
CPU_PLL_CFG<4>	5C4< 7D3<>
CPU_PLL_CFGEXT	7D4<>
CPU_PLL_FS00	7C4<>
CPU_PLL_FS01	7C4<
CPU_PLL_FS10	7C4<
CPU_PLL_STOP_BASE	7C7<
CPU_PLL_STOP_OC	7C4<> 7C8<> 31B6<>
CPU_PMONIN_L	5A4< 5C2<
CPU_PULLDOWN	5A2< 5A4< 5A4< 5C7<>
CPU_PULLUP	5A4< 5A4< 5C2<
CPU_QACK_L	5B4< 8B6<> 37D5>
CPU_QREQ_L	5B4> 8B6< 8C2< 37D5>
CPU_SHD0_L	5A7<> 5D2<
CPU_SHD1_L	5A7<> 5D2<
CPU_SMI_L	5B4< 5C2< 31C4<>
CPU_SRESET_L	5B2< 5B4< 40C8>
CPU_SRWX_L	5A4< 5C2<
CPU_TA_L	5B4< 8A4<> 8D2< 37D5>
CPU_TBEN	5B4< 5D2< 8A6<>
CPU_TBST_L	5A7> 8B6<> 37D5>
CPU_TEA_L	5B4< 8A4<> 8C2< 37D5>
CPU_THERM_DM	6A6<> 26A6<
CPU_THERM_DP	6A6<> 26A6<
CPU_TSIZ<0>	5A7> 8B6<>
CPU_TSIZ<0..2>	37D5>
CPU_TSIZ<1>	5A7> 8B6<>
CPU_TSIZ<2>	5A7> 8B6<>
CPU_TS_L	5C7<> 8D2< 8D6<> 37D5>
CPU_TT<0>	5A7<> 8B6<>
CPU_TT<0..4>	37C5>
CPU_TT<1>	5A7<> 8B6<>
CPU_TT<2>	5A7<> 8B6<>
CPU_TT<3>	5A7<> 8B6<>
CPU_TT<4>	5A7<> 8B6<>
CPU_VCORE_HI_OC	7B8< 31D4<> 35C8< 35D7<
CPU_VCORE_PWR_SEQ	35D8<>
CPU_VCORE_SEQ	35D8<
CPU_VCORE_SEQ_L	35D8<
CPU_VCORE_SLEEP	5C3< 5D8<> 6C6<> 35C1< 35D2< 39D3> 40B2>
CPU_VCORE_SLEEP_F	35C2<>
CPU_VCORE_SNUB	35B3<
CPU_WT_L	5A7> 8B6<> 37C5>
CSLOT_ADDR3_SPN	13B7>
CSLOT_ADDR4_SPN	13B7>
CSLOT_ADDR5_SPN	13B7>
CSLOT_ADDR6_SPN	13B7>
CSLOT_ADDR7_SPN	13B7>
CSLOT_ADDR8_SPN	13B7>
CSLOT_ADDR9_SPN	13B7>
CSLOT_CE1_L_SPN	13C7>
CSLOT_CE2_L_SPN	13C7>
CSLOT_IORD_L_SPN	13C7>
CSLOT_IOWAIT_L_PU	13C7<
CSLOT_IOWR_L_SPN	13C7>
CSLOT_OE_L_SPN	13C7>
CSLOT_WE_L_SPN	13C7>
CURRENT_THRESHOLD	32C4<
CY25811_S0	18B2<
CY25811_S1	18B2<
DCDC_EN	19A7<> 30C8< 34B6<> 35C8<> 40C1>
DCDC_EN_CTRL	30C8<>
DCDC_EN_L	34B6< 34B7<> 36C7<>
DDC_CLK_ISO	22D4<>
DDR_VREF	11D1< 11D3<> 11D5<> 11D6<> 11D8<> 39D3>
DVI_DDC_CLK	22D4<>
DVI_DDC_CLK_UF	22C5<> 22D3<> 40C7>
DVI_DDC_DATA	22C4<>
DVI_DDC_DATA_UF	22C5<> 40C7>
DVI_HPD	22C4<>
DVI_HPD_DIV	22C3<
DVI_HPD_UF	22C3< 22C5<> 40C7>
DVI_TRUN_ON_ILIM	22D2<
DVI_TURN_ON	22D3<>
DVI_TURN_ON_BASE	22D2<
EEPROM_WP_PD	6D2<>
EIDE_ADDR<0>	13B7> 25B8<
EIDE_ADDR<2..0>	38B5>
EIDE_ADDR<1>	13B7> 25B8<
EIDE_ADDR<2>	13B7> 25B8<
EIDE_CS0_L	13B7> 25B8< 38B5>
EIDE_CS1_L	13B7> 25B8< 38B5>
EIDE_DATA<0>	13C7<> 25C8<
EIDE_DATA<15..0>	38B5>
EIDE_DATA<1>	13C7<> 25C8<
EIDE_DATA<2>	13C7<> 25C8<
EIDE_DATA<3>	13C7<> 25C8<
EIDE_DATA<4>	13C7<> 25C8<
EIDE_DATA<5>	13B7<> 25B8<
EIDE_DATA<6>	13B7<> 25C8<
EIDE_DATA<7>	13B7<> 25C8<
EIDE_DATA<8>	13B7<> 25D8<
EIDE_DATA<9>	13B7<> 25D8<
EIDE_DATA<10>	13B7<> 25D8<
EIDE_DATA<11>	13B7<> 25D8<
EIDE_DATA<12>	13B7<> 25D8<
EIDE_DATA<13>	13B7<> 25C8<
EIDE_DATA<14>	13B7<> 25C8<
EIDE_DATA<15>	13B7<> 25C8<
EIDE_DMACK_L	13A7<> 25A8< 38B5>
EIDE_DMARQ	13A7< 25B8< 38B5>
EIDE_INT	13A7< 25A8< 38B5>
EIDE_IOCHRDY	13B7< 25A8< 38B5>
EIDE_OPTICAL_ADDR<0>	25A5<> 25B7< 40A4>
EIDE_OPTICAL_ADDR<2..0>	38B5>
EIDE_OPTICAL_ADDR<1>	25A5<> 25B7< 40A4>
EIDE_OPTICAL_ADDR<2>	25A6<> 25B7< 40A4>
EIDE_OPTICAL_CS0_L	25A5<> 25B7< 38B5> 40D4>
EIDE_OPTICAL_CS1_L	25A6<> 25B7< 38B5> 40D4>
EIDE_OPTICAL_DATA<0>	25A5<> 25C7< 40C4>
EIDE_OPTICAL_DATA<15..0>	38B5>
EIDE_OPTICAL_DATA<1>	25A5<> 25C7< 40C4>
EIDE_OPTICAL_DATA<2>	25A5<> 25C7< 40C4>
EIDE_OPTICAL_DATA<3>	25A5<> 25C7< 40C4>
EIDE_OPTICAL_DATA<4>	25A5<> 25C7< 40C4>
EIDE_OPTICAL_DATA<5>	25A5<> 25B7< 40C4>
EIDE_OPTICAL_DATA<6>	25A5<> 25C7< 40C4>
EIDE_OPTICAL_DATA<7>	25A5<> 25C7< 40B4>
EIDE_OPTICAL_DATA<8>	25A6<> 25D7< 40B4>
EIDE_OPTICAL_DATA<9>	25A6<> 25D7< 40B4>
EIDE_OPTICAL_DATA<10>	25A6<> 25D7< 40B4>
EIDE_OPTICAL_DATA<11>	25A6<> 25D7< 40B4>
EIDE_OPTICAL_DATA<12>	25A6<> 25D7< 40B4>
EIDE_OPTICAL_DATA<13>	25A6<> 25C7< 40B4>
EIDE_OPTICAL_DATA<14>	25A6<> 25C7< 40B4>
EIDE_OPTICAL_DATA<15>	25A6<> 25C7< 40B4>
EIDE_OPTICAL_DMAACK_L	25A6<> 25A7< 38A5> 40A4>
EIDE_OPTICAL_DMA_RQ	25A6<> 25B7< 38A5> 40A4>
EIDE_OPTICAL_INT	25A5<> 25A7< 38A5> 40D4>
EIDE_OPTICAL_IOCHRDY	25A5<> 25A7< 38A5> 40D3>
EIDE_OPTICAL_RD_L	25A6<> 25A7< 38B5> 40A4>
EIDE_OPTICAL_RST_L	25A7< 25B5<> 38A5> 40D4>
EIDE_OPTICAL_WR_L	25A5<> 25A7< 38A5> 40D4>
EIDE_RD_L	13A7> 25A8< 38B5>
EIDE_RST_L	13B7> 25A8< 38B5>
EIDE_WR_L	13A7> 25A8< 38B5>
ENET_COL	13C5< 28B7> 38A5>
ENET_COMA	28B7<>
ENET_CRS	13C5< 28B7> 38A5>
ENET_CTAP_CHGND	28A1< 39A6>
ENET_ENERGY_DET	14B5<> 28B7<>
ENET_HSDACM	28A7<>
ENET_HSDACP	28A7<>
ENET_LINK_RXD<0>	13C5< 28C7>
ENET_LINK_RXD<7..0>	38A5>
ENET_LINK_RXD<1>	13C5< 28C7>
ENET_LINK_RXD<2>	13C5< 28C7>
ENET_LINK_RXD<3>	13C5< 28B7>
ENET_LINK_RXD<4>	13C5< 28B7>
ENET_LINK_RXD<5>	13C5< 28B7>
ENET_LINK_RXD<6>	13C5< 28B7>
ENET_LINK_RXD<7>	13C5< 28B7>
ENET_LINK_TXD<0>	13B4< 13D5>
ENET_LINK_TXD<7..0>	38A5>
ENET_LINK_TXD<1>	13B4< 13D5>
ENET_LINK_TXD<2>	13B4< 13D5>
ENET_LINK_TXD<3>	13B4< 13D5>
ENET_LINK_TXD<4>	13B4< 13D5>
ENET_LINK_TXD<5>	13B4< 13D5>
ENET_LINK_TXD<6>	13A4< 13D5>
ENET_LINK_TXD<7>	13A4< 13D5>
ENET_LINK_TX_EN	13D5<> 38A5>
ENET_LINK_TX_ER	13D5<> 38A5>
ENET_MDC	13C5> 28B7< 38A5>
ENET_MDIO	13C5<> 28B7<> 38A5>
ENET_PHY_TXD<0>	13B5< 28C7<
ENET_PHY_TXD<7..0>	38A5>
ENET_PHY_TXD<1>	13B5< 28C7<
ENET_PHY_TXD<2>	13B5< 28C7<
ENET_PHY_TXD<3>	13B5< 28C7<
ENET_PHY_TXD<4>	13B5< 28C7<
ENET_PHY_TXD<5>	13B5< 28C7<
ENET_PHY_TXD<6>	13A5< 28C7<
ENET_PHY_TXD<7>	13A5< 28C7<
ENET_PHY_TX_EN	13D6< 28C7< 38A5>
ENET_PHY_TX_ER	13D6< 28C7< 38A5>
ENET_RSET	28A5<
ENET_RST_L	28B7<
ENET_RX_DV	13D5< 28B7> 38A5>
ENET_RX_ER	13C5< 28B7> 38A5>
ENET_VSSC	28A7<>
ESP_EN_L	6C1<> 6D2<
FAN1_PWM	26A4<>
FAN1_PWM_L	26A5<> 26B2<>
FAN1_TACH	26A4<> 26B2<
FAN2_PWM	26A3<>
FAN2_PWM_L	26A4<> 26B2<>
FAN2_TACH	26A3<> 26B2<
FANL_GND	39B6> 40B3>
FANL_PWM	40B3>
FANL_TACH	40B3>
FANR_GND	39B6> 40B3>
FANR_PWM	40B3>
FB_4_85V_BU	33A5<
FP_PWR_EN	19C6<> 22A6< 22B3<>
FP_PWR_EN_L	22B3<>
FWB_TPB0	29A3<
FWB_TPB1	29A4<
FWPLL_BYP	29C8<>
FW_BIAS0	29A5<>
FW_BIAS1	29A5<>
FW_BMODE	29B7<
FW_CORE_ADJ	29C8<
FW_CORE_BYP	29C7<>
FW_CPS	29B7<
FW_INPUT_PD	29A7<
FW_LINK_CNTL<0>	13C3<> 29C3<
FW_LINK_CNTL<1..0>	38A5>
FW_LINK_CNTL<1>	13C3<> 29C3<
FW_LINK_DATA<0>	13D3<> 29B8<
FW_LINK_DATA<7..0>	38A5>
FW_LINK_DATA<1>	13D3<> 29B8<
FW_LINK_DATA<2>	13D3<> 29B8<
FW_LINK_DATA<3>	13D3<> 29A8<
FW_LINK_DATA<4>	13C3<> 29A8<
FW_LINK_DATA<5>	13C3<> 29A8<
FW_LINK_DATA<6>	13C3<> 29A8<
FW_LINK_DATA<7>	13C3<> 29A8<
FW_LINK_LREQ	13C3<> 38A5>
FW_LKON	13C3<> 29B5<>
FW_OSC	29A4< 37A1>
FW_OSC_EN	29A3<
FW_PC_PD	29B7<
FW_PC_PU	29B7<
FW_PHY_CNTL<0>	29B4<> 29C3<
FW_PHY_CNTL<1..0>	38A5>
FW_PHY_CNTL<1>	29B4<> 29C3<
FW_PHY_DATA<0>	29B8<>
FW_PHY_DATA<7..0>	38A5>
FW_PHY_DATA<1>	29B8<>
FW_PHY_DATA<2>	29B8<>
FW_PHY_DATA<3>	29A8<>
FW_PHY_DATA<4>	29A8<>
FW_PHY_DATA<5>	29A8<>
FW_PHY_DATA<6>	29A8<>
FW_PHY_DATA<7>	29A8<>
FW_PHY_LPS	13C3<> 29B8<
FW_PHY_LREQ	13C2< 29B8< 38A5>
FW_PHY_PD	14C5< 29B8<
FW_PHY_PD_INT	14A7< 14C5<>
FW_PHY_RESET_L	29A8<
FW_PINT	13C3<> 29B4> 38A5>
FW_PLL_ADJ	29C7<
FW_PORT1_SEL	29B6<
FW_PWREN_L	30C6<>
FW_PWR_GATE	30D6<>
FW_R0	29A5<>
FW_R1	29A5<>
FW_TESTM	29A7<
FW_TPA0N	29B1<> 30C4<> 38D2>
FW_TPA0N_CONN	30C3<>
FW_TPA0P	29B1<> 30C4<> 38D2>
FW_TPA0P_CONN	30C3<>
FW_TPA1N	29B1<> 30A4<> 38C2>
FW_TPA1P	29B1<> 30A4<> 38C2>
FW_TPB0N	29B1<> 30C4<> 38D2>
FW_TPB0N_CONN	30C3<>
FW_TPB0P	29B1<> 30C4<> 38D2>
FW_TPB0P_CONN	30C3<>
FW_TPB1N	29B1<> 30A4<> 38C2>
FW_TPB1P	29B1<> 30A4<> 38C2>
FW_TPB2_PD	29A5<>
FW_TPI0N	38C2>
FW_TPI0P	38C2>
FW_TPI1N	30A3<> 38C2> 40D2>
FW_TPI1P	30A3<> 38C2> 40D2>
FW_TPO0N	38C2>
FW_TPO0P	38C2>
FW_TPO0R	30C2<> 39A3> 40A3>
FW_TPO1N	30A3<> 38C2> 40D2>
FW_TPO1P	30A3<> 38C2> 40D2>
FW_VGND0	30C2<> 39A3>
FW_VGND1	30A3<> 39A3>
FW_VREG_PD	29A7<
FW_XI	29A5<> 37A1>
GAIN_SETTING2	23C7<>
GPU_AGP_TEST	18D6<
GPU_AUXWIN	19C5<>
GPU_B	19D6<> 22D8<
GPU_C	19D6<> 22A8<
GPU_CLK27M_OUT	37C1>
GPU_CLK27M_UF	37C1>
GPU_COMP	19C6<> 22A8<
GPU_CORE_OK	19A6<> 19D4<> 21D2<> 21D7<>
GPU_DVI_DDC_CLK	19C5<> 22D3<>
GPU_DVI_DDC_DATA	19C5<> 22C3<>
GPU_DVOD<0>	19D7<> 20C8<
GPU_DVOD<0..23>	38D5>
GPU_DVOD<1>	19D7<> 20C8<
GPU_DVOD<2>	19D7<> 20C8<
GPU_DVOD<3>	19D7<> 20C8<
GPU_DVOD<4>	19D7<> 20B8<
GPU_DVOD<5>	19D7<> 20B8<
GPU_DVOD<6>	19D7<> 20B8<
GPU_DVOD<7>	19D7<> 20B8<
GPU_DVOD<8>	19D7<> 20B8<
GPU_DVOD<9>	19D7<> 20B8<
GPU_DVOD<10>	19D7<> 20B8<
GPU_DVOD<11>	19D7<> 20B8<
GPU_DVOD<12>	19D7<> 20B7<
GPU_DVOD<13>	19D7<> 20B7<
GPU_DVOD<14>	19D7<> 20B7<
GPU_DVOD<15>	19D7<> 20B7<
GPU_DVOD<16>	19D7<> 20B7<
GPU_DVOD<17>	19D7<> 20B7<
GPU_DVOD<18>	19C7<> 20B7<
GPU_DVOD<19>	19C7<> 20B7<
GPU_DVOD<20>	19C7<> 20A7<
GPU_DVOD<21>	19C7<> 20A7<
GPU_DVOD<22>	19C7<> 20A7<
GPU_DVOD<23>	19C7<> 20A7<
GPU_DVOD_DE	19C7<> 20A7< 20A8<
GPU_DVO_CLKP	19C7<> 37B1>
GPU_DVO_CLKP_R	19C8<
GPU_DVO_CLKP_R1	19C8< 20B8<
GPU_DVO_CLKP_R2	19C8< 20A7<
GPU_DVO_HSYNC	19C7<> 20B8< 38C5>
GPU_DVO_VSYNC	19C7<> 20A7< 20B8< 38C5>
GPU_FBCLK0	37B1>
GPU_FBCLK0_L	37B1>
GPU_FBCLK1	37B1>
GPU_FBCLK1_L	37B1>
GPU_G	19D6<> 22D8<
GPU_HPD	19C5< 22C3<>
GPU_MEM_IO	39C3>
GPU_MEM_IO_FLT	21C2< 39C3>
GPU_R	19D6<> 22D8<
GPU_SSCLK_IN	37B1>
GPU_SSCLK_UF	37C1>
GPU_THERM_DM_TP	18A6<>
GPU_THERM_DP_TP	18A6<>
GPU_TV_GND1	22B8<> 39B6>
GPU_TV_GND2	22A8<> 39B6>
GPU_VCORE	18A6< 19A3<> 19B5<> 19D4< 39C3> 40B2>
GPU_VCORE_CNTL	19A3<>
GPU_VCORE_CNTL_L	19A4< 19B7<>
GPU_VCORE_NECK	19B5<> 39B3>
GPU_VCORE_PWR_SEQ	19A8<>
GPU_VCORE_SEQ	19A8<
GPU_VCORE_SEQ_L	19A8<
GPU_VCORE_SW	19A4<> 39B1>
GPU_VCORE_VDDCI	18A5< 39C3>
GPU_Y	19D6<> 22B8<
HD_ADDR<0>	25C2<> 25C3<
HD_ADDR<2..0>	38C5>
HD_ADDR<1>	25C2<> 25C3<
HD_ADDR<2>	25B3< 25C1<>
HD_CS0_L	25C2<> 25C3< 38B5>
HD_CS1_L	25B3< 25C1<> 38B5>
HD_DATA<0>	25C2<> 25D3<
HD_DATA<15..0>	38C5>
HD_DATA<1>	25C2<> 25D3<
HD_DATA<2>	25D2<> 25D3<
HD_DATA<3>	25D2<> 25D3<
HD_DATA<4>	25C3< 25D2<>
HD_DATA<5>	25C3< 25D2<>
HD_DATA<6>	25C3< 25D2<>
HD_DATA<7>	25C3< 25D2<>
HD_DATA<8>	25C3< 25D1<>
HD_DATA<9>	25C3< 25D1<>
HD_DATA<10>	25C3< 25D1<>
HD_DATA<11>	25D1<> 25D3<
HD_DATA<12>	25B3< 25D1<>
HD_DATA<13>	25B3< 25D1<>
HD_DATA<14>	25C1<> 25C3<
HD_DATA<15>	25B3< 25C1<>
HD_DIOR_L	25A3< 25C2<> 38B5>
HD_DIOW_L	25A3< 25C1<> 38B5>
HD_DMACK_L	25A3< 25C2<> 38B5>
HD_DMARQ	13C6< 25C2<> 38B5>
HD_INTRQ	13C6< 25C1<> 38B5>
HD_IOCHRDY	25A3< 25C1<> 38B5>
HD_RESET_L	25A3< 25D2<> 38B5>
HIGH_VCORE	19A2<>
HIGH_VCORE_DIV	19A3<
HPD_4V_REF	22C3<
HPD_BASE	22C1<
HPD_ON	22C2<>
HPD_ON_RC	22C2<
HPD_PWR_SNS_EN	19C7<> 22C3<>
HPD_PWR_SW	22C2<>
I2S0_BITCLK_F	26B7< 26C7<>
I2S0_DEV_TO_SB_DTI_F	26C7<> 26C7<>
I2S0_MCLK_F	26C7< 26C7<>
I2S0_RESET_L_F	26B7< 26C5<>
I2S0_SB_TO_DEV_DTO_F	26C7< 26C7<>
I2S0_SYNC_F	26C7< 26C7<>
I2S1_BITCLK_F	26B7< 26C7<>
I2S1_DEV_TO_SB_DTI_F	26C5< 26C7<>
I2S1_RESET_L_F	26B5< 26C5<>
I2S1_SYNC_F	26B7< 26C7<>
IAC_FB	32D4<
IAC_RC_COMP	32D4<
ICT_TRST_L	6B1<> 6D2<
INTREPID_ACS_REF	8A6<
INT_AGPPVT	12D4<>
INT_AGP_FB_IN	12C4< 37C1>
INT_AGP_FB_OUT	12C4<> 37C1>
INT_AGP_VREF	12B4< 12D4<> 18D5< 39D3>
INT_AUDIO_TO_SND	14B2< 26C8< 40C6>
INT_CPUFB_IN	8A6< 8B6< 37D1>
INT_CPUFB_IN_NORM	8A4< 37D1>
INT_CPUFB_LONG	8A4< 37D1>
INT_CPUFB_OUT	8A6< 8A6<> 37D1>
INT_CPUFB_OUT_NORM	8A4< 37D1>
INT_CPUFB_OUT_SHORT	8A5< 37D1>
INT_DDRCLK2_N_TP	9B6<>
INT_DDRCLK2_P_TP	9B6<>
INT_DDRCLK5_N_TP	9B6<>
INT_DDRCLK5_P_TP	9B6<>
INT_ENET_RST_L	14B5<> 28B8<
INT_EXTINT8_PU	14B5<> 14C7<
INT_EXTINT10_PU	14A7< 14B5<>
INT_EXTINT13_PU	14B5<> 14B7<
INT_GPIO0	14C5<>
INT_GPIO1_PU	14C5<> 14C7< 35C8<
INT_GPIO9_PU	14A7< 14B5<>
INT_I2C_CLK0	6B3<> 6D2< 11A3<> 11A8<> 13C2< 13C3<> 23C4<> 40B8>
INT_I2C_CLK1	13C2< 13C3<> 14B7< 23A7<> 24C2<> 26B4< 40B8>
INT_I2C_CLK2	14A2<> 26C5<> 26D3<> 40C6>
INT_I2C_DATA0	6B3<> 6D2<> 11A3<> 11A8<> 13C2< 13C3<> 23C4<> 40B8>
INT_I2C_DATA1	13B2< 13C3<> 14B7< 23A7<> 24C2<> 26B4<> 40B8>
INT_I2C_DATA2	14A2<> 26C3<> 26C5<> 40C6>
INT_JTAG_TEI	13C2< 13C5<
INT_MEM_REF_H	9B6< 39D3>
INT_MEM_VREF	9A7< 9B6<> 39D3>
INT_MOD_BITCLK_UF	14A3<> 14A7<
INT_MOD_CLKOUT_UF	14A3<> 14B7<
INT_MOD_DTI	14A2< 26C6< 26D2< 40B1>
INT_MOD_DTI_UF	14A7<
INT_MOD_DTO_UF	14A3<> 14B7<
INT_MOD_SYNC_UF	14A3<> 14A7<
INT_PCI_FB_IN	12C7< 37C1>
INT_PCI_FB_OUT	12C7<> 37C1>
INT_PEND_PROC_INT	14A5> 31C4<>
INT_PROC_SLEEP_REQ_L	14A5< 31B4<>
INT_PU_RESET_L	13D3< 26D3<> 31A2< 31C4<>
INT_REF_CLK_IN	14A5< 14B5< 37C1>
INT_REF_CLK_OUT	14A5> 14B7< 37C1>
INT_RESET_L	9B3< 13D3< 31C7< 31D4<>
INT_ROM_CS_L	12A6< 12C7>
INT_ROM_OE_L	12A6< 12C7>
INT_ROM_RW_L	12A6< 12C7>
INT_SND_CLKOUT	14A3<>
INT_SND_SCLK	14A3<>
INT_SND_SYNC	14B3<>
INT_SND_TO_AUDIO	14B3<>
INT_SUSPEND_ACK_L	8B6> 31B6<>
INT_SUSPEND_REQ_L	8B6< 31B6<> 31C7<
INT_TST_MONIN_PD	13C2< 13C5<
INT_TST_MONOUT_TP	13C5>
INT_TST_PLLEN_PD	13C5< 13D2<
INT_WATCHDOG_L	14A5> 31C6<>
INV_ON_PWM	19C6<> 22A3<
IO_RESET_L	17A7< 23C6< 24C2< 27B8< 28B8< 31C6<> 31D7<
JTAG_ASIC_TCK	13C5< 13D2< 28A5< 40D8>
JTAG_ASIC_TDI	28A5< 28D7< 40D8>
JTAG_ASIC_TDO	13C5> 13D2< 14A7< 40D8>
JTAG_ASIC_TMS	13C5< 13D2< 28A5< 40D8>
JTAG_ASIC_TRST_L	13C2< 13C5< 28A5< 40D8>
JTAG_CPU_TCK	5B2< 5B4< 6A3> 40C8>
JTAG_CPU_TDI	5B2< 5C4< 6B1<> 40C8>
JTAG_CPU_TDO_TP	5C4> 40C8>
JTAG_CPU_TMS	5B2< 5B4< 6B1<> 40C8>
JTAG_CPU_TRST_L	5B4< 6B1<> 6C2< 40B1> 40C8>
JTAG_ENET_TDO	13C5< 13D2< 28A5>
KBDLED_ANODE	23A3< 23A7<> 39B6>
KBDLED_RETURN	23A3<> 23A7<> 39B6>
KBD_CAPSLOCK_LED	40B4>
KBD_COMMAND_L	23C2< 31C6<>
KBD_CONTROL_L	23C2< 31C6<> 40B4>
KBD_FUNCTION_L	23C2< 31B6<> 40B4>
KBD_ID	23D2< 31B6<>
KBD_LED1_OUT	40C2>
KBD_LED2_OUT	40C2>
KBD_NUMLOCK_LED	40C3>
KBD_OPTION_L	23C2< 31B6<> 40B4>
KBD_SHIFT_L	23C2< 31C6<> 40B4>
KBD_X<0>	23C2< 31C6<> 40B4>
KBD_X<1>	23C2< 31C6<> 40B4>
KBD_X<2>	23C2< 31C6<>
KBD_X<3>	23C2< 31C6<> 40B4>
KBD_X<4>	23C2< 31C6<>
KBD_X<5>	23C2< 31C6<>
KBD_X<6>	23D2< 31C6<>
KBD_X<7>	23D2< 31C6<>
KBD_X<8>	23D2< 31C6<>
KBD_X<9>	23D2< 31C6<>
KBD_Y<0>	31D6<> 40D3>
KBD_Y<1>	31D6<> 40D3>
KBD_Y<2>	31D6<>
KBD_Y<3>	31D6<> 40D3>
KBD_Y<4>	31D6<> 40D3>
KBD_Y<5>	31D6<>
KBD_Y<6>	31C6<> 40C3>
KBD_Y<7>	31C6<> 40C3>
LCD_DIGON_L	22A6<
LCD_PWREN_L	22A5<>
LED_LINK10	28B5<>
LED_LINK100	28B5<>
LED_RX_SPN	28B5>
LEFT_USB_DM	25B2<> 27B3< 38A2> 40D1>
LEFT_USB_DP	25B2<> 27A3< 38A2> 40D1>
LID_CLOSED_L	23A6<> 40C4>
LM2594_IN	29D8<> 39B3>
LT1962_INT_ADJ	14D6<
LT1962_INT_BYP	14D6<>
LTC1625_ITH	32D3<>
LTC1962_1V5_VIN	39A1>
LTC1962_1V5_VOUT	39A1>
LTC1962_INT_VIN	14D7<> 39A1>
LTC1962_L3_VIN	39A1>
LTC1962_L3_VOUT	39A1>
LTC3405_SW	28D4<> 39B3>
LTC3411_GND	39A1>
LTC3411_ITH	39A1>
LTC3411_ITH_RC	39A1>
LTC3411_SHDN	39A1>
LTC3411_SYNC	39A1>
LTC3411_VCC	39B1>
LTC3412_GND	36A6<>
LTC3412_ITH	36A6<>
LTC3412_ITH_RC	36A6<
LTC3412_PGOOD	36A4<>
LTC3412_RT	36A6<
LTC3412_RUNSS	36A6<>
LTC3412_SYNC	36A6<>
LTC3412_VFB	36A6<>
LTC3412_VFB_DIV	36A6<
LTC3707_START_RC	34B6<>
LVDS_DDC_CLK	19C5<> 22B5<> 40A7>
LVDS_DDC_DATA	19C5<> 22B5<> 40A7>
LVDS_L0N	19B5> 22B4<> 38C2> 40C7>
LVDS_L0P	19B5> 22B4<> 38C2> 40C7>
LVDS_L1N	19B5> 22B4<> 38C2> 40C7>
LVDS_L1P	19B5> 22B4<> 38C2> 40C7>
LVDS_L2N	19B5> 22B4<> 38C2> 40C7>
LVDS_L2P	19B5> 22B4<> 38C2> 40C7>
LVDS_L3N_TP	19B5>
LVDS_L3P_TP	19B5>
LVDS_U0N	19C5> 22A4<> 38C2> 40B7>
LVDS_U0P	19C5> 22A4<> 38C2> 40B7>
LVDS_U1N	19C5> 22A4<> 38C2> 40B7>
LVDS_U1P	19C5> 22A4<> 38C2> 40B7>
LVDS_U2N	19B5> 22A4<> 38B2> 40B7>
LVDS_U2P	19B5> 22A4<> 38B2> 40B7>
LVDS_U3N_TP	19B5>
LVDS_U3P_TP	19B5>
MAIN_RESET_L	14C7< 17A7< 17D5< 18C8< 20D7< 25D6<> 27B8< 31D4<> 31D7< 40C1>
MASTER_SWING	20B7<
MAX1715_FB2	36B1< 36B4<
MAX1715_GND	36B5<> 36C5< 39C1>
MAX1715_ON_RC	36C7<>
MAX1715_REF	36B5<> 39C1>
MAX1715_SKIP	36C4< 39C1>
MAX1715_TON	36C5< 39C1>
MAX1715_VCC	36D5< 39C1>
MAX1717_AB_SEL	35A7< 35C6<
MAX4172_OUT	32D4<>
MAX8860_CC	21A6<>
MAX8860_FAULT	21A6<>
MAXBUS_SLEEP	5D1< 5D5< 6B2< 6B4< 6C1< 7B7< 7D8< 8B8< 8C3< 8C8< 8D1< 8D8< 15D8< 16D8< 35D8< 39D3>
MDI0_PD	28B4<
MDI1_PD	28B4<
MDI2_PD	28B4<
MDI3_PD	28B3<
MDI_M<0>	28B5<> 38D2>
MDI_M<1>	28B5<> 38D2>
MDI_M<2>	28B5<> 38D2>
MDI_M<3>	28B5<> 38D2>
MDI_P<0>	28B5<> 38D2>
MDI_P<1>	28B5<> 38D2>
MDI_P<2>	28B5<> 38D2>
MDI_P<3>	28B5<> 38D2>
MEM_ADDR<0>	9B5< 9D6<>
MEM_ADDR<12..0>	37A5>
MEM_ADDR<1>	9B5< 9D6<>
MEM_ADDR<2>	9B5< 9D6<>
MEM_ADDR<3>	9B5< 9D6<>
MEM_ADDR<4>	9B5< 9D6<>
MEM_ADDR<5>	9B5< 9D6<>
MEM_ADDR<6>	9B5< 9D6<>
MEM_ADDR<7>	9B5< 9D6<>
MEM_ADDR<8>	9B5< 9D6<>
MEM_ADDR<9>	9A5< 9D6<>
MEM_ADDR<10>	9A5< 9D6<>
MEM_ADDR<11>	9A5< 9D6<>
MEM_ADDR<12>	9A5< 9D6<>
MEM_BA<0>	9A5< 9D6<>
MEM_BA<1..0>	37A5>
MEM_BA<1>	9A5< 9C6<>
MEM_CAS_L	9A5< 9C6<> 37A5>
MEM_CKE<0>	9B6<> 9C5<
MEM_CKE<3..0>	37A5>
MEM_CKE<1>	9B6<> 9C5<
MEM_CKE<2>	9B6<> 9C5<
MEM_CKE<3>	9B6<> 9C5<
MEM_CS_L<0>	9C5< 9C6<>
MEM_CS_L<3..0>	37A5>
MEM_CS_L<1>	9C5< 9C6<>
MEM_CS_L<2>	9C5< 9C6<>
MEM_CS_L<3>	9C5< 9C6<>
MEM_DATA<0>	9D8<> 10C7<>
MEM_DATA<7..0>	37C5>
MEM_DATA<1>	9D8<> 10C7<>
MEM_DATA<2>	9D8<> 10C7<>
MEM_DATA<3>	9D8<> 10C7<>
MEM_DATA<4>	9D8<> 10C7<>
MEM_DATA<5>	9D8<> 10C7<>
MEM_DATA<6>	9D8<> 10C7<>
MEM_DATA<7>	9D8<> 10C7<>
MEM_DATA<8>	9D8<> 10C7<>
MEM_DATA<15..8>	37C5>
MEM_DATA<9>	9D8<> 10C7<>
MEM_DATA<10>	9D8<> 10C7<>
MEM_DATA<11>	9D8<> 10C7<>
MEM_DATA<12>	9D8<> 10B7<>
MEM_DATA<13>	9C8<> 10B7<>
MEM_DATA<14>	9C8<> 10B7<>
MEM_DATA<15>	9C8<> 10B7<>
MEM_DATA<16>	9C8<> 10C5<>
MEM_DATA<31..16>	37C5>
MEM_DATA<17>	9C8<> 10C5<>
MEM_DATA<18>	9C8<> 10C5<>
MEM_DATA<19>	9C8<> 10C5<>
MEM_DATA<20>	9C8<> 10C5<>
MEM_DATA<21>	9C8<> 10C5<>
MEM_DATA<22>	9C8<> 10C5<>
MEM_DATA<23>	9C8<> 10C5<>
MEM_DATA<24>	9C8<> 10C5<>
MEM_DATA<25>	9C8<> 10C5<>
MEM_DATA<26>	9C8<> 10C5<>
MEM_DATA<27>	9C8<> 10C5<>
MEM_DATA<28>	9C8<> 10C5<>
MEM_DATA<29>	9C8<> 10B5<>
MEM_DATA<30>	9C8<> 10B5<>
MEM_DATA<31>	9C8<> 10B5<>
MEM_DATA<32>	9C8<> 10C3<>
MEM_DATA<47..32>	37B5>
MEM_DATA<33>	9C8<> 10C3<>
MEM_DATA<34>	9C8<> 10C3<>
MEM_DATA<35>	9C8<> 10C3<>
MEM_DATA<36>	9C8<> 10C3<>
MEM_DATA<37>	9C8<> 10C3<>
MEM_DATA<38>	9C8<> 10C3<>
MEM_DATA<39>	9B8<> 10C3<>
MEM_DATA<40>	9B8<> 10C3<>
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MEM_DATA<42>	9B8<> 10C3<>
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MEM_DATA<44>	9B8<> 10C3<>
MEM_DATA<45>	9B8<> 10B3<>
MEM_DATA<46>	9B8<> 10B3<>
MEM_DATA<47>	9B8<> 10B3<>
MEM_DATA<48>	9B8<> 10C1<>
MEM_DATA<55..48>	37B5>
MEM_DATA<49>	9B8<> 10C1<>
MEM_DATA<50>	9B8<> 10C1<>
MEM_DATA<51>	9B8<> 10C1<>
MEM_DATA<52>	9B8<> 10C1<>
MEM_DATA<53>	9B8<> 10C1<>
MEM_DATA<54>	9B8<> 10C1<>
MEM_DATA<55>	9B8<> 10C1<>
MEM_DATA<56>	9B8<> 10C1<>
MEM_DATA<63..56>	37A5>
MEM_DATA<57>	9B8<> 10C1<>
MEM_DATA<58>	9B8<> 10C1<>
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MEM_DATA<60>	9B8<> 10C1<>
MEM_DATA<61>	9B8<> 10B1<>
MEM_DATA<62>	9B8<> 10B1<>
MEM_DATA<63>	9B8<> 10B1<>
MEM_DQM<0>	9C6<> 10C7<> 37C5>
MEM_DQM<1>	9C6<> 10B7<> 37C5>
MEM_DQM<2>	9C6<> 10C5<>
MEM_DQM<3..2>	37B5>
MEM_DQM<3>	9C6<> 10B5<>
MEM_DQM<4>	9C6<> 10C3<>
MEM_DQM<5..4>	37B5>
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MEM_DQS<3>	9C6<> 10B5<>
MEM_DQS<4>	9C6<> 10C3<>
MEM_DQS<5..4>	37B5>
MEM_DQS<5>	9C6<> 10B3<>
MEM_DQS<6>	9C6<> 10C1<> 37B5>
MEM_DQS<7>	9C6<> 10B1<> 37A5>
MEM_MUXSEL_H<0>	9B6<> 10A6<
MEM_MUXSEL_H<1..0>	37A5>
MEM_MUXSEL_H<1>	9B6<> 10A4<
MEM_MUXSEL_L<0>	9B6<> 10A6<
MEM_MUXSEL_L<1..0>	37A5>
MEM_MUXSEL_L<1>	9B6<> 10A4<
MEM_RAS_L	9A5< 9C6<> 37A5>
MEM_WE_L	9A5< 9C6<> 37A5>
MLB_ALS_GAIN_SW	23C4<> 23C8<>
MLB_ALS_OP_COMP	23D7<
MLB_ALS_OP_IN	23D7<
MLB_ALS_OUT	23B4<> 23D6<
MLB_ALS_OUT_FB	23D7<>
MLB_PHOTODIODE	23D8<>
MMM_ACC_DETECT	24B8<> 24C2<>
MMM_ACC_PWRDOWN	24B8<> 24C1< 24C7<>
MMM_ACC_SELFTEST	24B8<> 24C2<> 24C7<> 40A4>
MMM_ACC_X_AXIS	24C5< 24C5> 24D2<> 40A4>
MMM_ACC_Y_AXIS	24C5< 24C5> 24D2<> 40A4>
MMM_ACC_Z_AXIS	24B5< 24C2<> 24C5> 40A4>
MMM_FFIRQ_L	14A7< 14B5<> 24C1<
MMM_PIC_AAC_PWRDOWN	24C3<>
MMM_PIC_AN2_PD	24D4<>
MMM_PIC_AN3_PU	24C4<>
MMM_PIC_FFIRQ_L	24C2<>
MMM_PIC_SIRQ_L	24C2<>
MMM_RESET_L	24C1< 24C3<>
MMM_SIRQ_L	14A7< 14B5<> 24C1<
MODEM_USB_DM	14C1< 26D2<> 38A2> 40B6>
MODEM_USB_DP	14C1< 26D2<> 38A2> 40B6>
MOD_BITCLK	14A2< 26B8< 26D2<> 40B1>
MOD_CLKOUT	14A2< 26D3<> 40A1>
MOD_DTO	14A2< 26D3<> 40A1>
MOD_SYNC	14A2< 26B8< 26D2<> 40A1>
MPIC_CPU_INT_L	5B2< 5B4< 14B5>
MSEN_PULL_UP_MASTER	20C6<>
MSEN_PULL_UP_SLAVE	20B5<>
NEC_AMC_TP	27A5<
NEC_AVDD	27D6< 39A3>
NEC_AVSS_F	27A5< 27B4<
NEC_CRUN_L	27A7<>
NEC_IDSEL	27B7<
NEC_IO_RESET_L	27B7< 27B7<
NEC_LEFT_USB_OVERCURRENT	25B2<> 27D1< 40D1>
NEC_LEFT_USB_PWREN	25B2<> 27B5<> 40D1>
NEC_LEGC	27A7<
NEC_MAIN_RESET_L	27A7< 27B7<
NEC_NANDTESTEN_TP	27A5<
NEC_NANDTESTOUT_TP	27A4<>
NEC_NC1_TP	27B5<>
NEC_NC2_TP	27B5<>
NEC_OCI<1>	27B5< 27D2<
NEC_OCI<2>	27B5< 27D2<
NEC_OCI<3>	27B5<
NEC_OCI<4>	27B5<
NEC_OCI<5>	27B5<
NEC_PCI_INTA_L	27A7< 27B7>
NEC_PCI_INTB_L	27A7< 27B7>
NEC_PCI_INTC_L	27A7< 27B7>
NEC_PCI_PERR_L	27B7<> 27C8<
NEC_PCI_SERR_L	27B7> 27C8<
NEC_PME_L	27A7> 27B7<
NEC_PPON3_TP	27B5>
NEC_PPON4_TP	27B5>

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NEC_PPONS_TP      27B5>
NEC_RIGHT_USB_OVERCURRENT  27D1< 33B7<> 40C1>
NEC_RIGHT_USB_PWREN  27B5<> 33A7<> 40C1>
NEC_RREF          27B5<>
NEC_SMI_L_TP      27A7>
NEC_USB_DAN       27B4< 27C2<> 38B2>
NEC_USB_DAP       27A4< 27C2<> 38B2>
NEC_USB_DBM       27A4< 27C2<> 38B2>
NEC_USB_DBP       27A4< 27C2<> 38B2>
NEC_USB_RSDM1     27C5<> 38B2>
NEC_USB_RSDM2     27C5<> 38B2>
NEC_USB_RSDP1     27C5<> 38B2>
NEC_USB_RSDP2     27C5<> 38B2>
NEC_XT1           27D5< 37B1>
NEC_XT2           27D5<> 37B1>
NEC_XT2_R         27D4<
NTEST1_TP         27B5<
NUMLOCK_LED_L     31D7<
OVER_18V_ADJ      32C3<>
PA2_PD            23B2< 23C4<>
PA3_PD            23B2< 23C4<>
PB2_PD            23B2< 23C4<>
PB3_PD            23B2< 23C4<>
PB4_PD            23B2< 23C4<>
PC0_PD            23B2< 23B4<>
PCI1510_VR_EN_L   17C7<
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                40B6>
PCI_AD<31..0>   3BC5>
PCI_AD<1>       9C3< 12D6<> 17C7<> 25B6<> 27D7<>
                40A6>
PCI_AD<2>       9C3< 12D6<> 17C7<> 25C5<> 27D7<>
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PCI_AD<3>       9C3< 12D6<> 17C7<> 25C6<> 27C7<>
                40A6>
PCI_AD<4>       9C3< 12D6<> 17C7<> 25C5<> 27C7<>
                40A6>
PCI_AD<5>       9C3< 12D6<> 17C7<> 25C6<> 27C7<>
                40A6>
PCI_AD<6>       9C3< 12C6<> 17C7<> 25C5<> 27C7<>
                40A6>
PCI_AD<7>       9C3< 12C6<> 17C7<> 25C6<> 27C7<>
                40B5>
PCI_AD<8>       9C3< 12C6<> 17C7<> 25C5<> 27C7<>
                40B5>
PCI_AD<9>       9C3< 12C6<> 17C7<> 25C5<> 27C7<>
                40B5>
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PCI_AD<18>      9C3< 12C6<> 17B7<> 25C5<> 25D4<
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PCI_AD<19>      9C3< 12C6<> 17B7<> 25C6<> 27C7<>
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PCI_AD<21>      12C6<> 17B7<> 25C6<> 27C7<> 40C5>
PCI_AD<22>      12C6<> 17B7<> 25C5<> 27C7<> 40B5>
PCI_AD<23>      12C6<> 17B7<> 25C6<> 27C7<> 40B5>
PCI_AD<24>      9C1<> 12C6<> 17B7<> 25C5<> 27C7<>
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PCI_AD<25>      9C1<> 12C6<> 17B7<> 25D6<> 27C7<>
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PCI_AD<26>      9C1<> 12C6<> 17B7<> 25C5<> 27C7<>
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PCI_AD<27>      9C1<> 12C6<> 17B7<> 25D6<> 27C8<>
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PCI_AD<28>      9C1<> 12C6<> 17B7<> 25D5<> 27C7<>
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PCI_AD<29>      9C1<> 12C6<> 17B7<> 25D6<> 27B7<>
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PCI_AD<30>      9C1<> 12C6<> 17B7<> 25D5<> 27B7<>
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PCI_AD<31>      9C1<> 12C6<> 17B7<> 25D6<> 27B7<>
                40A5>
PCI_CBE<0>      12C7<> 17B7<> 25C5<> 27B7<> 40D4>
PCI_CBE<3..0>   3BC5>
PCI_CBE<1>      12C7<> 17B7<> 25C6<> 27B7<> 40D4>
PCI_CBE<2>      12C7<> 17B7<> 25C6<> 27B7<> 40D4>
PCI_CBE<3>      12C7<> 17B7<> 25C6<> 27B7<> 40D4>
PCI_DEVSEL_L    12B7< 12C7<> 17A7<> 25C5<> 27B7<>
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PCI_FRAME_L     12B7< 12C7<> 17B7<> 25C5<> 27B7<>
                38C5> 40A5>
PCI_IRDY_L      12B7< 12C7<> 17B7<> 25C6<> 27B7<>
                38C5> 40A5>
PCI_PAR         12C7<> 17B7<> 25C5<> 27B7<> 38C5>
                40D4>
PCI_STOP_L      12A7< 12C7<> 17B7<> 25C5<> 27B7<>
                38C5> 40A5>
PCI_TRDY_L      12B7< 12C7<> 17A7<> 25C5<> 27B7<>
                38C5> 40A5>
PLL_STOP_L      7C4<> 7C8<>
PMU_ACK_L       14C2< 31C4<>
PMU_AC_DET      31A5< 31B4<>
PMU_AC_IN       31B4<>
PMU_BATT0_DET_L  31B4<>
PMU_BATT1_DET_L_PU  31B4<> 31D2<
PMU_BATT_DET_L   31A8<> 31B3< 31D2< 32A4<> 40C3>
PMU_BYTE         31B6< 31C7<
PMU_CAPSLOCK_LED_L  31C6<>
PMU_CHARGE_V     31C4<> 32B8<>
PMU_CHRG_BATT_B  31C4<> 32A8<>
PMU_CLK          14C2<> 31C4<>
PMU_CNVSS        31B6< 31C7<
PMU_CPU_HRESET_L  8A2< 6C3<> 31C4<>
PMU_CUSTOM_RESET  31A8<>
PMU_CUSTOM_RESET_L  31A7<> 31B8<
PMU_EPM          31D2< 31D4<>
PMU_FROM_INT     14C2<> 31C4<>
PMU_I2C_CLK      31B4<> 31C2<
PMU_I2C_DATA     31B4<> 31C2<
PMU_INT_L        14B5<> 14B7< 31B6<>
PMU_INT_NMI      14B5<> 14B7< 31D4<>
PMU_KB_RESET_L   40B2>
PMU_LID_CLOSED_L  23A8< 23B4<> 31B2< 31C4<>
PMU_NMI_BUTTON_L  26A1< 31C2< 31C4<>
PMU_NMI_L        31C2< 31C4<>
PMU_NUMLOCK_LED_L  31C6<>
PMU_OOPS         31B2< 31B4<>
PMU_PME_L        14B5<> 27B8< 31B2< 31C4<>
PMU_POWERUP_OK   31B4<> 31D2<
PMU_POWER_UP_L   30D8<> 31C6<> 31D7< 34B8<
PMU_RSQ_L        14B7< 14C2> 31C4<>
PMU_RESET_BUTTON_L  26A2< 31C4<> 31D2<
PMU_RESET_L      31B7<>
PMU_SELECT       31C6<>
PMU_SLEEP_LED    23B4<>
PMU_SLEEP_LED_L  23B3<> 31C4<>
PMU_SMB_CLK      31B4<> 31C2< 32A3<
PMU_SMB_DATA     31B4<> 31C2< 32A2<
PMU_TO_INT       14C2<> 31C4<>
POWER_UP         30D8<>
POWER_VALID      31B2< 31C4<>
PP3V3_MMM        24C8< 24D6<
PP3V3_MMM_PIC    24C1< 24D5<
PP3V3_SI_AVCC1   20D7< 39B3>
PP3V3_SI_AVCC2   20C5< 39B3>
PP3V3_SI_PVCC1   20C7< 39B3>
PP3V3_SI_PVCC2   20C5< 39B3>
PP3V3_SI_VCC1    20D7< 39B3>
PP3V3_SI_VCC2    20C5< 39B3>
PWR_BUTTON_L     23A7<> 26C1< 40B2>
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RAM_ADDR<12..0>  37A5>
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RAM_ADDR<2>      9B4< 11B5<> 11B6<>
RAM_ADDR<3>      9B4< 11B3<> 11B8<>
RAM_ADDR<4>      9B4< 11B5<> 11B6<>
RAM_ADDR<5>      9B4< 11B3<> 11B8<>
RAM_ADDR<6>      9B4< 11B5<> 11B6<>
RAM_ADDR<7>      9B4< 11B3<> 11B8<>
RAM_ADDR<8>      9B4< 11B5<> 11B6<>
RAM_ADDR<9>      9A4< 11B3<> 11B8<>
RAM_ADDR<10>     9A4< 11B3<> 11B8<>
RAM_ADDR<11>     9A4< 11B5<> 11B6<>
RAM_ADDR<12>     9A4< 11B3<> 11B8<>
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RAM_BA<1..0>     37A5>
RAM_BA<1>        9A4< 11B5<> 11B6<>
RAM_CAS_L        9A4< 11B5<> 11B6<> 37A5>
RAM_CKE<0>       9A3< 9C4< 11B6<>
RAM_CKE<3..0>    37A5>
RAM_CKE<1>       9A3< 9C4< 11B8<>
RAM_CKE<2>       9A3< 9C4< 11C5<>
RAM_CKE<3>       9A3< 9C4< 11C3<>
RAM_CS_L<0>      9C4< 11B8<>
RAM_CS_L<3..0>   37A5>
RAM_CS_L<1>      9C4< 11B6<>
RAM_CS_L<2>      9C4< 11B3<>
RAM_CS_L<3>      9C4< 11B5<>
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RAM_DATA_A<7..0>  37C5>
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RAM_DATA_A<2>    10C8<> 11D8<>
RAM_DATA_A<3>    10B8<> 11D8<>
RAM_DATA_A<4>    10B8<> 11D6<>
RAM_DATA_A<5>    10B8<> 11D6<>
RAM_DATA_A<6>    10B8<> 11D6<>
RAM_DATA_A<7>    10B8<> 11D6<>
RAM_DATA_A<8>    10B8<> 11D8<>
RAM_DATA_A<15..8>  37C5>
RAM_DATA_A<9>    10C7<> 11D8<>
RAM_DATA_A<10>   10C7<> 11D8<>
RAM_DATA_A<11>   10C7<> 11D6<>
RAM_DATA_A<12>   10C7<> 11D6<>
RAM_DATA_A<13>   10C7<> 11D6<>
RAM_DATA_A<14>   10C7<> 11D6<>
RAM_DATA_A<15>   10C7<> 11D6<>
RAM_DATA_A<16>   10C6<> 11D6<>
RAM_DATA_A<31..16>  37B5>
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RAM_DATA_A<18>   10C6<> 11C8<>
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RAM_DATA_A<21>   10B6<> 11C6<>
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RAM_DATA_A<24>   10B6<> 11C8<>
RAM_DATA_A<25>   10C6<> 11C8<>
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RAM_DATA_A<27>   10C5<> 11C8<>
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RAM_DATA_A<29>   10C5<> 11C6<>
RAM_DATA_A<30>   10C5<> 11C6<>
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RAM_DATA_A<47..32>  37B5>
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RAM_DATA_A<37>   10B4<> 11B6<>
RAM_DATA_A<38>   10B4<> 11B6<>
RAM_DATA_A<39>   10B4<> 11B6<>
RAM_DATA_A<40>   10B4<> 11B8<>
RAM_DATA_A<41>   10D3<> 11B8<>
RAM_DATA_A<42>   10C3<> 11A8<>
RAM_DATA_A<43>   10C3<> 11A6<>
RAM_DATA_A<44>   10C3<> 11B6<>
RAM_DATA_A<45>   10C3<> 11A8<>
RAM_DATA_A<46>   10C3<> 11A6<>
RAM_DATA_A<47>   10C3<> 11A6<>
RAM_DATA_A<48>   10C2<> 11A8<>
RAM_DATA_A<55..48>  37B5>
RAM_DATA_A<49>   10C2<> 11A8<>
RAM_DATA_A<50>   10C2<> 11A8<>
RAM_DATA_A<51>   10C2<> 11A8<>
RAM_DATA_A<52>   10B2<> 11A6<>
RAM_DATA_A<53>   10B2<> 11A6<>
RAM_DATA_A<54>   10B2<> 11A6<>
RAM_DATA_A<55>   10B2<> 11A6<>
RAM_DATA_A<56>   10B2<> 11A8<>
RAM_DATA_A<63..56>  37A5>
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RAM_DATA_A<58>   10C1<> 11A8<>
RAM_DATA_A<59>   10C1<> 11A6<>
RAM_DATA_A<60>   10C1<> 11A6<>
RAM_DATA_A<61>   10C1<> 11A6<>
RAM_DATA_A<62>   10C1<> 11A6<>
RAM_DATA_A<63>   10C2<> 11A5<>
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RAM_DQM_A<1>     10C7<> 11D6<> 37C5>
RAM_DQM_A<2>     10B6<> 11C6<>
RAM_DQM_A<3..2>  37B5>
RAM_DQM_A<3>     10C5<> 11C6<>
RAM_DQM_A<4>     10B4<> 11B6<>
RAM_DQM_A<5..4>  37B5>
RAM_DQM_A<5>     10C3<> 11A6<>
RAM_DQM_A<6>     10B2<> 11A6<> 37B5>
RAM_DQM_A<7>     10C1<> 11A6<> 37A5>
RAM_DQM_B<0>     10C8<> 11D5<> 37C5>
RAM_DQM_B<1>     10C8<> 11D5<> 37C5>
RAM_DQM_B<2>     10C6<> 11C5<>
RAM_DQM_B<3..2>  37B5>
RAM_DQM_B<3>     10C6<> 11C5<>
RAM_DQM_B<4>     10C4<> 11B5<>
RAM_DQM_B<5..4>  37B5>
RAM_DQM_B<5>     10C4<> 11B5<>
RAM_DQM_B<6>     10C2<> 11A5<> 37B5>
RAM_DQM_B<7>     10C2<> 11A3<> 37A5>
RAM_MUXSEL_H     10A3< 10A5< 10B1<> 10B3<> 37A5>
RAM_MUXSEL_L     10A3< 10A5< 10B5<> 10B7<> 37A5>
RAM_RAS_L        9A4< 11B5<> 11B6<> 37A5>
RAM_WE_L         9A4< 11B3<> 11B6<> 37A5>
RESET_VREF       6C3<>
RF_DISABLE_L_SPN  25D6<> 40C1>
RIGHT_USB_DM     27A3< 33A7<> 38A2> 40D1>
RIGHT_USB_DP     27A3< 33A7<> 38A2> 40D1>
RJ45_C0_PD       28B2<>
RJ45_C1_PD       28B2<>
RJ45_C2_PD       28B2<>
RJ45_C3_PD       28B2<>
RJ45_DN<0>       28B2<> 38D2> 40B3>
RJ45_DN<1>       28B2<> 38D2> 40B3>
RJ45_DN<2>       28B2<> 38D2> 40A3>
RJ45_DN<3>       28B2<> 38D2> 40A3>
RJ45_DP<0>       28B2<> 38D2> 40B3>
RJ45_DP<1>       28B2<> 38D2> 40B3>
RJ45_DP<2>       28B2<> 38D2> 40A3>
RJ45_DP<3>       28B2<> 38D2> 40A3>
ROM_CS_L         9B3< 12A5< 25B6<> 40B1>
ROM_OE_L         9B3< 12A5< 25C5<> 40B1>
ROM_ONBOARD_CS_L  9B3< 25C6<> 40B1>
ROM_RW_L         9B3< 12A5< 25C6<> 40B1>
ROM_WP_L         9B3<
RSDM3_TP         27C5>
RSDM4_TP         27C5>
RSDM5_TP         27C5>
RSDP3_TP         27C5>
RSDP4_TP         27C5>
RSDP5_TP         27C5>
RUN_OR_AC        30D7<>
SI_I2C_CLK       19C5<> 20B5< 20C7<>
SI_I2C_DATA      19C5<> 20B5<> 20C7<>
SI_MASTER        20B8<
SI_M_HTPLG       20B7<
SI_RESET_L       20B5< 20C7< 20D8<
SI_SECONDARY     20C8<
SI_S_HTPLG       20A5<
SI_TMDS_CLKN     20B7< 20C4<
SI_TMDS_CLKP     20B7< 20C4<
SI_TMDS_DN<0>    20B7< 20C4<
SI_TMDS_DN<1>    20B7< 20C4<
SI_TMDS_DN<2>    20B7< 20C4<
SI_TMDS_DN<3>    20A5< 20C2<
SI_TMDS_DN<4>    20A5< 20C2<
SI_TMDS_DN<5>    20A5< 20C2<
SI_TMDS_DP<0>    20B7< 20C4<
SI_TMDS_DP<1>    20B7< 20C4<
SI_TMDS_DP<2>    20B7< 20C4<
SI_TMDS_DP<3>    20A5< 20C2<
SI_TMDS_DP<4>    20A5< 20C2<
SI_TMDS_DP<5>    20A5< 20C2<
SI_VREF          20A5< 20B8<
SLAVE_SWING      20A5<
SLEEP            23C4<> 31B6<> 31D7< 34A4< 34A6<
                 34B3< 34B8<> 36B3< 36D2< 40A1>
SLEEP_ANODE      23C2< 26C5<>
SLEEP_LED        40B6>
SLEEP_LED_I      23C2<
SLEEP_LED_L      23C2<
SLEEP_LED_SW_L   23C3<>
SLEEP_LED_UF     23C2<
SLEEP_LS5        34A5<> 34AB<
SLEEP_LS5_EN_L   34A5<>
SLEEP_L_LS5      19A7<> 28A8<> 34A5<> 35C8<> 36C8<
SLEEP_L_LS5_EN_L  34A6<>
SLEEP_L_LS5_INV  36A3< 36C2< 36C8<>
SLEEP_L_LS5_NET  34B3<> 36C8<>
SLEEP_NET        34A3<>
SLEEP_NET_INV    34A3<>
SMC_TP           27B5<
SND_AGND         26C6<> 39B6>
SND_AMP_MUTE     26D4< 26D4<> 40A4>
SND_AMP_MUTE_INV  26C8< 26D4<
SND_AMP_MUTE_L   14C5<> 26D3<>
SND_CLKOUT       14B1< 26C8< 37B1> 40D6>
SND_HP_MUTE      26C4<>
SND_HP_MUTE_INV  40A4>
SND_HP_MUTE_L    14C5<> 26C4<>
SND_HP_SENSE_L   40C6>
SND_HW_RESET_L   14A7< 14B5<> 26B8< 40C6>
SND_LIN_SENSE_L  40C6>
SND_SCLK         14B1< 26B8< 37B1> 40C6>
SND_SYNC         14B1< 26C8< 40D6>
SND_TO_AUDIO     14B1< 26C8< 40D6>
SOFT_PWR_ON_L    22D1< 23A8< 31A8<> 31C6<> 31D7<
                 35A3<>
SOUND_SPDIF_GPO0  14C5< 26D8<
SPDIF_GPO0       26D7<> 26D7<
SRC1K_TP         27A5> 40A4>
SRMOD_TP         27A5< 40A4>
ST7_ICP_SEL_PD   23A2< 23C6<
ST7_KBD_LED_OUT  23A5<> 23C4<>
ST7_OSC1         23C6<
ST7_OSC2         23C6<>
ST7_PB6_PD       23A2< 23C4<>
ST7_RESET_L      23C6<>
ST7_SENSOR4_SCK_PD  23B2< 23C4<>
ST7_SENSOR4_SDA_PD  23B2< 23C4<>
ST7_SENSOR5_SCK  23B2< 23C4<>
ST7_SENSOR5_SDA  23B3< 23C4<>
ST7_SLEEP_LED_H  23B4<> 23C4<>
ST7_XTAL_IN      23C6<
STOP_AGP_L       12D2< 12D4<>
SUPPLY_M_DM      26A8< 26B6<
SUPPLY_M_DP      26A8< 26B6<
SUTRO_ALS_GAIN_SW  23C4<> 25B2<> 40C2>
SUTRO_ALS_OUT    23B4<> 25B2<> 40C2>
SYSCLK_CPU       5C4< 8A6< 37D1>
SYSCLK_CPU_UF    8A6<> 37D1>
SYSCLK_DDRCLK_A0  9D4< 11D8<> 37D1>
SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 37D1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A1  9D4< 11A6<> 37D1>
SYSCLK_DDRCLK_A1_L  9D4< 11A6<> 37D1>
SYSCLK_DDRCLK_A1_L_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A1_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_B0  9D4< 11D3<> 37D1>
SYSCLK_DDRCLK_B0_L  9C4< 11D3<> 37C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 37D1>
SYSCLK_DDRCLK_B0_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_B1  9D4< 11A5<> 37C1>
SYSCLK_DDRCLK_B1_L  9D4< 11A5<> 37C1>
SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_B1_UF  9B6<> 9D5< 37D1>
SYSCLK_LA_TP     8A6<>
SYSTEM_CLK_EN    14A5< 14A7< 31C4<>
SYS_BATT_ISNS    24A2< 31C2<
SYS_BATT_ISNS1   31B4<> 31C3<
SYS_BATT_ISNS2   31B4<> 31C3<
TEB_TP           27A5< 40A4>
TEST_TP          27A5< 40A4>
THERM1_A_DM      26A6< 26A8< 38A2>
THERM1_A_DP      26A6< 26A8< 38A2>
THERM1_DM        26A5< 26A5< 26B5<> 26B5< 38A2>
THERM1_DP        26A5< 26A5< 26B5<> 26B5< 38A2>
THERM1_M_DM      38A2>
THERM1_M_DP      38A2>
THERM2_A_DM      26A6< 26A7< 38A2>
THERM2_A_DP      26A6< 26A7< 38A2>
THERM2_DM        26A5< 26B5<> 26B5< 38A2>
THERM2_DP        26A5< 26B5<> 26B5< 38A2>
THERM2_M_DM      38A2>
THERM2_M_DP      38A2>
THERM_INV        26B2<>
THERM_L_OC       26B1<> 31B4<>
THERM_L_OC_CONN  23A7<>
TMDS_CLKN        20B2< 20C3< 20D4< 22B7<> 38B2>
TMDS_CLKP        20B3< 20C3< 20D4< 22C7<> 38B2>
TMDS_CLK_CMF     20B3<
TMDS_CONN_CLKN   22B6<> 22C7<> 38B2> 40A8>
TMDS_CONN_CLKP   22C6<> 22C7<> 38B2> 40D7>
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TMDS_CONN_DP<1>  22B7<> 22D5<>
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TMDS_CONN_DP<5>  20D1<> 22C7<>
TMDS_D0_CMF      20B3<
TMDS_D1_CMF      20A3<
TMDS_D2_CMF      20A3<
TMDS_D3_CMF      20B2<
TMDS_D4_CMF      20B1<
TMDS_D5_CMF      20A1<
TMDS_DN<0>       20B2< 20C3< 20D4< 22C8<> 38B2>
                 40B8>
TMDS_DN<1>       20A2< 20C3< 20D2< 22B8<> 38B2>
                 40A8>
TMDS_DN<2>       20A2< 20C3< 20D2< 22B7<> 38B2>
                 40A8>
TMDS_DN<3>       20B1< 20C1< 20D2<>
TMDS_DN<4>       20B1< 20C1< 20D2<>
TMDS_DN<5>       20A1< 20C1< 20D2<>
TMDS_DP<0>       20B3< 20C3< 20D4< 22B8<> 38B2>
                 40A8>
TMDS_DP<1>       20A3< 20C3< 20D2< 22B8<> 38B2>
                 40A8>
TMDS_DP<2>       20A3< 20C3< 20D2< 22B7<> 38B2>
                 40A8>
TMDS_DP<3>       20B2< 20C1< 20D2<>
TMDS_DP<4>       20B2< 20C1< 20D2<>
TMDS_DP<5>       20A2< 20C1< 20D2<>
TMDS_MASTER      20B8<
TMDS_SYNC        20A7< 20B8<
TPAD_F_RXD       40C4>
TPAD_F_TXD       40C4>
TPAD_RXD         31C2< 31C4<>
TPAD_TXD         31B2< 31C4<>
TPS2211_SHDN_L_PU  17C4<
TP_BB_XTAL       6C3<>
TP_MMM_ICSP_PGC  24C3<>
TP_MMM_ICSP_PGD  24C3<>
TP_MMM_ICSP_PGM  24C3<>
TV_C             22A6<> 40D6>
TV_COMP          22A6<> 40D6>
TV_GND1          22B6<> 39B6> 40A7>
TV_GND2          22A6<> 39B6> 40A7>
TV_Y             22A6<> 40D6>
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UIDE_ADDR<2..0>  38C5>
UIDE_ADDR<1>     13D7<> 25C4<
UIDE_ADDR<2>     13D7<> 25B4<
UIDE_CS0_L       13C7<> 25C4< 38C5>
UIDE_CS1_L       13C7<> 25B4< 38C5>
UIDE_DATA<0>     13D7<> 25D4<
UIDE_DATA<6..0>  38C5>
UIDE_DATA<1>     13D7<> 25D4<
UIDE_DATA<2>     13D7<> 25D4<
UIDE_DATA<3>     13D7<> 25D4<
UIDE_DATA<4>     13D7<> 25C4<
UIDE_DATA<5>     13D7<> 25C4<
UIDE_DATA<6>     13D7<> 25C4<
UIDE_DATA<7>     13D7<> 25C4< 38C5>
UIDE_DATA<8>     13D7<> 25C4<
UIDE_DATA<15..8>  38C5>
UIDE_DATA<9>     13D7<> 25C4<
UIDE_DATA<10>    13D7<> 25C4<
UIDE_DATA<11>    13D7<> 25D4<
UIDE_DATA<12>    13D7<> 25B4<
UIDE_DATA<13>    13D7<> 25B4<
UIDE_DATA<14>    13D7<> 25C4<
UIDE_DATA<15>    13D7<> 25B4<
UIDE_DIOR_L      13C7<> 25A4< 38C5>
UIDE_DIOW_L      13C7<> 25A4< 38C5>
UIDE_DMACK_L     13C7<> 25A4< 38C5>
UIDE_DMARQ       13C7<> 38C5>
UIDE_INTRQ       13C7< 38C5>
UIDE_IOCHRDY     13C7< 25A4< 38C5>
UIDE_REF         13C7<> 39D3>
UIDE_RST_L       13C7<> 25A4< 38C5>
USB2_PCI_GNT_L   12C7<> 27B7<
USB2_PCI_INT_L   14B5<> 14C7< 27A8<
USB2_PCI_REQ_L   12A7< 12D7<> 27B7>
USB_D1M          14D1< 27A5> 27B4<
USB_D1P          14D1< 27A4< 27A5>
USB_D2M          27A5>
USB_D2P          27A5>
USB_DAM          14B2<> 14D2< 27A5>
USB_DAP          14B2<> 14D2< 27A5>
USB_DBM          14B2<> 14D1<
USB_DBP          14B2<> 14D1<
USB_DCM          14B2<> 14D2< 27A5>
USB_DCP          14B2<> 14D2< 27A5>
USB_DDM          14B2<> 14C2<
USB_DDP          14B2<> 14C2<
USB_DEM          14B2<> 14C2< 38B2>
USB_DEP          14B2<> 14C2< 38B2>
USB_DFM          14B2<> 14B2< 38B2>
USB_DFP          14B2< 14B2<> 38B2>
USB_OC_AB_L      14B2< 14C7<
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	43	45

*** Part Cross-Reference for the entire design ***

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FL3 FILTER_LC 22
G1 OSC 29
G2 OSC 18
J1 CON_FIST_S2MT_SM 14
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J3 CON_F14RT_S2MT_SM 25
J4 CON_4RT_WRIB 26
J5 CON_12 35
J6 CON_F30RT_S2MT_SM 22
J7 CON_4RT_WRIB 22
J8 CON_F16ST_D_SMA 26
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J11 CON_F14RT_S2MT_SM 33
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RP7	RPAK4P	14
RP8	RPAK4P	14
RP9	RPAK4P	25
RP10	RPAK4P	25
RP11	RPAK4P	25
RP12	RPAK4P	13
RP13	RPAK4P	25
RP14	RPAK4P	13
RP15	RPAK4P	13
RP16	RPAK4P	13
RP17	RPAK4P	12
RP18	RPAK4P	12
RP19	RPAK4P	12
RP20	RPAK4P	12
RP21	RPAK4P	8
RP22	RPAK4P	12
RP23	RPAK4P	8
RP24	RPAK4P	8 14
RP25	RPAK4P	9
RP26	RPAK4P	9
RP27	RPAK4P	23
RP29	RPAK4P	14
RP30	RPAK4P	9
RP31	RPAK4P	9
RP33	RPAK4P	9
RP34	RPAK4P	9
RP35	RPAK4P	9
RP36	RPAK4P	9
RP37	RPAK4P	29
RP38	RPAK4P	29
RP39	RPAX10P2C	17
RP40	RPAK4P	31
RP41	RPAK4P	31
RP42	RPAX10P2C	23
RP43	RPAX10P2C	23
RP45	RPAK4P	27
RP47	RPAK4P	14
RP48	RPAK4P	14
RP49	RPAK4P	25
RP50	RPAK4P	25
RP51	RPAK4P	14
RP52	RPAK4P	23 27
RP53	RPAK4P	23
RP54	RPAK4P	27
RP55	RPAK4P	27
RP56	RPAK4P	14
RP62	RPAK2P	20
RP63	RPAK2P	20
RP64	RPAK2P	20
RP65	RPAK2P	20
RP66	RPAK2P	20
RP67	RPAK2P	20
RP68	RPAK2P	20
SH1	SHLD_3P_EMI	4
SP1	SPKR_CLIP_P84	4

SP2	SPKR_CLIP_P84	4
SP3	SPKR_CLIP_P84	4
SP4	SPKR_CLIP_P84	4
SP5	SPKR_CLIP_P84	4
SP6	SPKR_CLIP_P84	4
T1	XFR_ENET_1000BT	28
U1	SN74AUC1G04	7
U2	SN74AUC1G08	6
U3	AOT7407	26
U4	SN74AUC1G08	6
U5	KXM52	24
U6	FAN2558	5
U7	VREG_LT1962	14
U8	MAX8860	21
U9	CBTV4020	10
U10	CBTV4020	10
U11	PI3B3257	35
U12	CBTV4020	10
U13	CBTV4020	10
U14	LTC3405	28
U15	COMPARATOR_LMC7211	32
U16	LTC1778	19
U17	FEPR_1MX8	9
U18	LTC1625	33
U19	PWR_CNTRL_TPS2211	17
U20	MAX1717	35
U21	COMPARATOR_LMC7211	33
U22	MAX1715	36
U23	AMP_MAX4172	32
U24	7432	22
U25	VREG_LP2951	33
U26	PCI5519GGU	17
U27	COMPARATOR_LMC7211	31
U28	LTC3707	34
U29	TSB81BA3A	29
U30	VREG_LP2951	33
U31	MAX1772	32
U32	EEPROM_32KX8_M24256B	6
U33	M16C62	31
U34	VREG_LM2594	29
U35	SIL178	20
U36	LTC1761	29
U37	VREG_LT1962	29
U38	COMPARATOR_LMC7211	32
U39	UPD720101_FBGA	27
U40	OPAMP_MAX4236EUTT	23
U41	MAX6804	31
U42	CLK_GEN_CY28512	14
U43	APOLLO_MPC7447A_360	5 6
U44	RAGE_MBLTY_M11_CSP64_667	18 19 21
U45	INTREPID	8 9 12 13 14 15
U46	COMPARATOR_LMC7211	22
U47	CLK_GEN_CY25811	18
U48	SIL178	20
U49	TRANSCEIVER_88E1111	28
U50	OPAMP_LMC7111	32
U51	INA138	24
U52	FEPR_256KX8_ST72264_BGA	23
U53	PIC16F818_QFN	24
U54	VREG_MM1571J	21
U55	VREG_MM1571J	21
U56	741G32	22
U57	741G32	22
U58	LTC3412	36
U59	MM3120	23
U60	LIS3L02AQ	24
U61	ATTINY2313	6
U62	COMPARATOR_LMC7211	30
XW1	SHORT	36
XW2	SHORT	19
XW3	SHORT	35
XW4	SHORT	33
XW5	SHORT	35
XW6	SHORT	36
XW7	SHORT	35
XW8	SHORT	34
XW9	SHORT	26
XW10	SHORT	26
XW11	SHORT	26
XW12	SHORT	22
XW13	SHORT	22
XW14	SHORT	24
XW15	SHORT	35
XW16	SHORT	24
XW17	SHORT	24
XW18	SHORT	32
XW19	SHORT	32
XW20	SHORT	19
XW21	SHORT	19
XW22	SHORT	19
XW23	SHORT	19
XW24	SHORT	19
XW27	SHORT	21
XW28	SHORT	21
XW29	SHORT	21
XW30	SHORT	21
XW31	SHORT	5
Y1	CRYSTAL	14
Y3	CRYSTAL	28
Y4	CRYSTAL	23
Y5	CRYSTAL	27
Y6	CRYSTAL	31
Y7	CRYSTAL_4PIN	31
ZT1	HOLE_VIA	4
ZT2	MTGHOLE	4
ZT3	HOLE_VIA	4
ZT4	MTGHOLE	4
ZT5	MTGHOLE	4
ZT6	MTGHOLE	4
ZT7	HOLE_VIA	4
ZT8	HOLE_VIA	4
ZT9	HOLE_VIA	4
ZT10	MTGHOLE	4
ZT11	MTGHOLE	4
ZT12	HOLE_VIA	4
ZT13	HOLE_VIA	4
ZT14	HOLE_VIA	4
ZT15	HOLE_VIA	4
ZT16	MTGHOLE	4
ZT17	HOLE_VIA	4
ZT18	HOLE_VIA	4
ZT19	HOLE_VIA	4
ZT20	HOLE_VIA	4
ZT21	HOLE_VIA	4
ZT22	HOLE_VIA	4
ZT23	HOLE_VIA	4
ZT24	HOLE_VIA	4
ZT25	HOLE_VIA	4
ZT26	HOLE_VIA	4
ZT27	HOLE_VIA	4
ZT28	HOLE_VIA	4
ZT29	HOLE_VIA	4
ZT30	HOLE_VIA	4
ZT31	HOLE_VIA	4
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ZT36	HOLE_VIA	4
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ZT38	HOLE_VIA	4
ZT39	HOLE_VIA	4
ZT40	HOLE_VIA	4
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ZT46	HOLE_VIA	4
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ZT60	HOLE_VIA	4
ZT61	HOLE_VIA	4
ZT62	HOLE_VIA	4
ZT63	HOLE_VIA	4
ZT64	HOLE_VIA	4
ZT65	HOLE_VIA	4
ZT66	HOLE_VIA	4
ZT67	HOLE_VIA	4
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ZT78	HOLE_VIA	4
ZT79	HOLE_VIA	4
ZT80	HOLE_VIA	4
ZT81	HOLE_VIA	4
ZT82	HOLE_VIA	4
ZT83	MTGHOLE	4