1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
C		480849	PRODUCTION RELEASED	01/10/07	?

SCHEM,MLB,PB17"
01/04/2007

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23	LMU, LIGHT SENSOR, BOOTBANGER, SLEEP LED SPIDEY - KBD,TPAD,HALL EFFECT,PWR BUTTON
24	INTERNAL CONNECTORS - DVD, CARDSLOT, HARD DRIVE, LEFT USB/BLUETOOTH
25	FAN CONTROLLER, MODEM, SOUND SERIAL DEBUG (JOLLY ROGER, PWR/NMI/RESET)
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36	SIGNAL CONSTRAINTS (1 OF 3) - DIGITAL/CLK
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41-42	SIGNAL NAMES
43-44	COMPONENT LOCATIONS

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG		✓
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG	✓	
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS	✓	
INT_TMDS		✓
NO_4XVCORE	✓	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6582	1	SCHEM,MLB,PB17 INCH	SCH1	
820-1524	1	PCBF,MLB,PB17 INCH	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

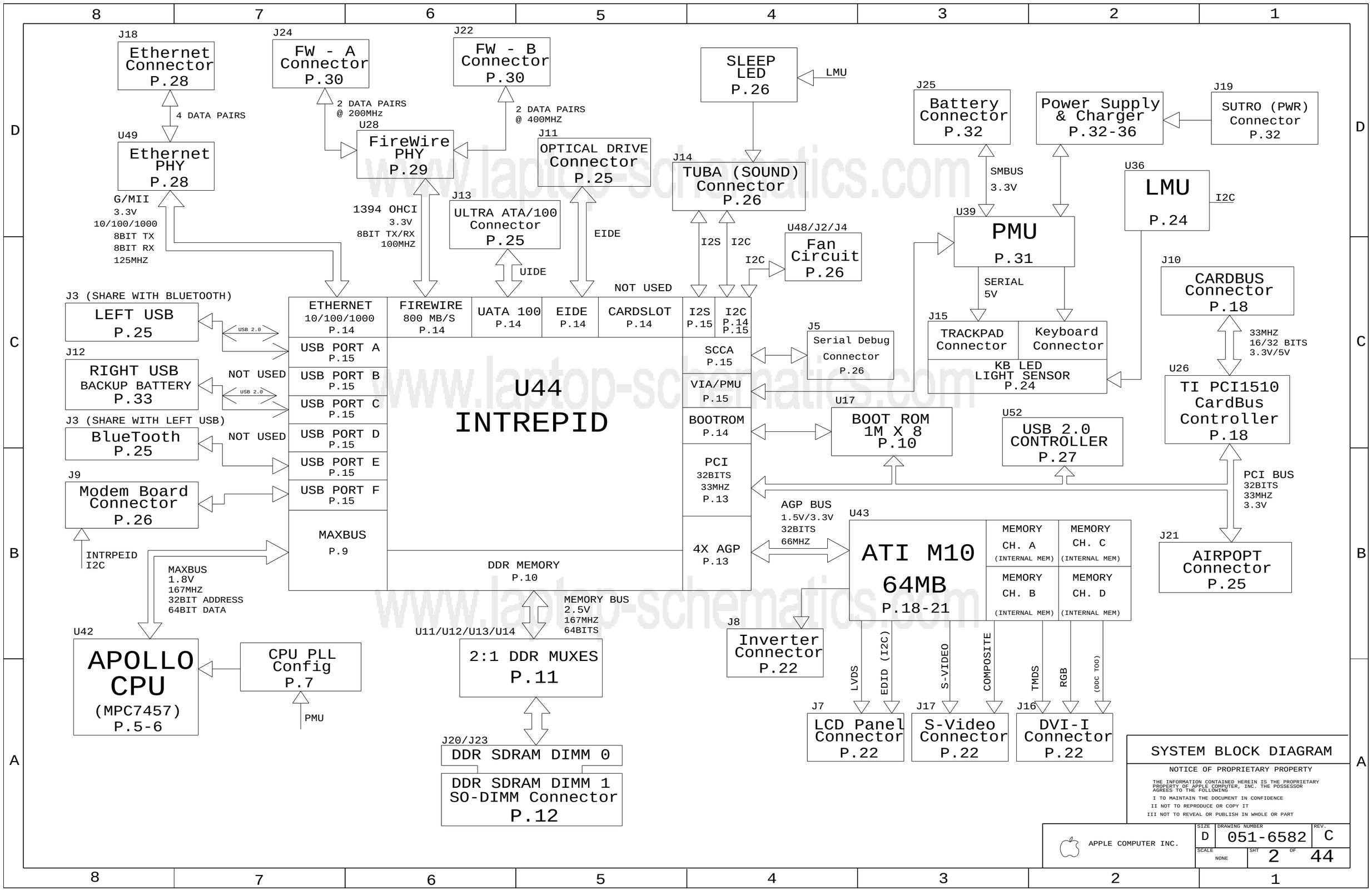
MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,PB17 INCH

DRAWING NUMBER 051-6582 REV. C

SHT 1 OF 44



SYSTEM BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C

SCALE	SHT	OF
NONE	2	44

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 31

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF
U21 PG 31
>-13.44V TURNS-ON
<-13.44V SHUTS-OFF

RUN/SS
BUCK REGULATOR (LTC1625) PG 32
VCC
AC: 12.8V
NO AC: BATTERY VOLTAGE 1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS (12.8V)

14V_PBUS

+3V_PMU LDO PG 32

+BATT

+5V_MAIN

+3V_PMU

+4_6V_BU

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V
MAIN 3V/5V DC/DC (LTC3707) PG 33
VCC
PGOOD
STBYMD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN

3V_5V_OK

HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND

TURNS CONTROL TO RUN/SS WHEN IT'S OPEN

+3.3V_MAIN

+PBUS

BACKUP BATTERY

12.8V CHARGES BACKUP BATTERY

24V IS OUTPUT ONLY FROM BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT PG 32

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+24V_PBUS

DC/DC (LTC3411) PG 35
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

+1.8V_MAIN

MAXBUS
BROADCOM

BATTERY CHARGER (MAX1772) PG 31

+BATT

3S 3P PRISMATIC CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 31

+PBUS

BACKLIGHT INVERTER

+5V_MAIN

VCC
MAIN 2.5V/1.5V DC/DC (MAX1715) PG 35
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP31 DDR I/O
MAP31 DDR CORE
DDR POWER
+2.5V_MAIN

1_5V_2_5V_OK

+1.5V_MAIN
INTREPID CORE
AGP I/O

+5V_MAIN

DCDC_EN_L

AFTER PMU IS UP AND RUNNING DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

+PBUS (12.8V)

+5V_MAIN

EXT_VCC
VCC
DC/DC (LTC1778) PG 20
SHUTDOWN: STOPPED
SLEEP: D3HOT/D3COLD
RUN: RUNNING
TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE
RUN/SS

GPU_VCORE
+1.2V/+1.0V

DCDC_EN
SLEEP
D3_COLD
GPU_VCORE SEQUENCING

1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER

1_5V_2_5V_OK

D3_HOT

DCDC_EN_L
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON

HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

+PBUS

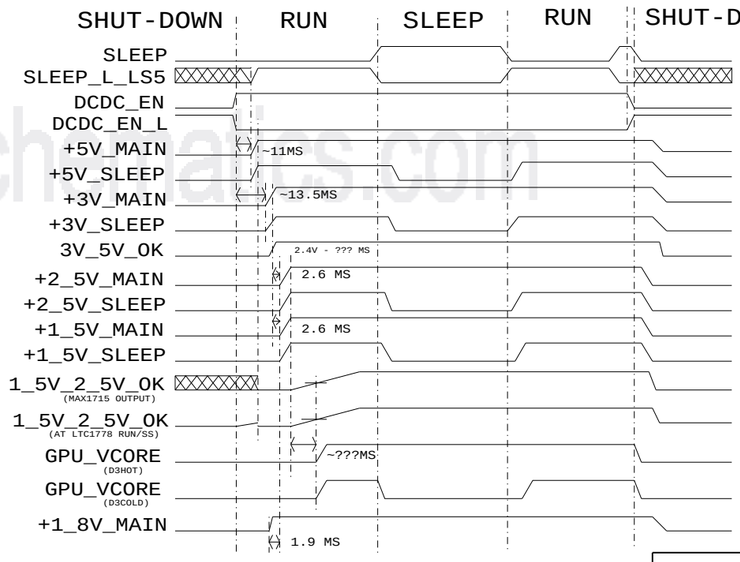
DCDC_EN
SLEEP

MAXBUS SEQUENCING

+5V_MAIN

VCC
SHDN
DC/DC (MAX1717) PG 34
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

CPU_VCORE
(+1.4V/+1.5V)



POWER BLOCK DIAGRAM

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 3 OF 44	

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES

ASICS HEATSINK MOUNTS

OMIT ZT10 255R158
OMIT ZT2 255R158
OMIT ZT11 255R158
OMIT ZT6 235R126
OMIT ZT16 235R126

CONDUCTIVE MOUNTS

OMIT ZT4 235R126

CHASSIS MOUNTS

I/O AREA

OMIT ZT5 146R126 — CHGND5
BS1 STDOFF-217ODX150IDX35H-TH — CHGND1
OMIT ZT83 146R126 — CHGND6

INVERTER

SH1 OG-503040 SHLD-SM — CHGND2

SPEAKER CLIPS

SP6 SPKR_CLIP_P84
SP1 SPKR_CLIP_P84
SP3 SPKR_CLIP_P84
SP5 SPKR_CLIP_P84
SP2 SPKR_CLIP_P84
SP4 SPKR_CLIP_P84

GROUND VIAS

ZT77 HOLE-VIA-20R10
ZT81 HOLE-VIA-20R10
ZT24 HOLE-VIA-20R10
ZT38 HOLE-VIA-20R10
ZT36 HOLE-VIA-20R10
ZT27 HOLE-VIA-20R10
ZT40 HOLE-VIA-20R10
ZT39 HOLE-VIA-20R10
ZT37 HOLE-VIA-20R10
ZT28 HOLE-VIA-20R10
ZT30 HOLE-VIA-20R10
ZT34 HOLE-VIA-20R10
ZT33 HOLE-VIA-20R10
ZT43 HOLE-VIA-20R10
ZT46 HOLE-VIA-20R10

ZT35 HOLE-VIA-20R10
ZT50 HOLE-VIA-20R10
ZT44 HOLE-VIA-20R10
ZT66 HOLE-VIA-20R10
ZT67 HOLE-VIA-20R10
ZT52 HOLE-VIA-20R10
ZT53 HOLE-VIA-20R10
ZT70 HOLE-VIA-20R10
ZT71 HOLE-VIA-20R10
ZT78 HOLE-VIA-20R10
ZT69 HOLE-VIA-20R10
ZT65 HOLE-VIA-20R10
ZT47 HOLE-VIA-20R10
ZT45 HOLE-VIA-20R10
ZT49 HOLE-VIA-20R10

ZT48 HOLE-VIA-20R10
ZT56 HOLE-VIA-20R10
ZT72 HOLE-VIA-20R10
ZT55 HOLE-VIA-20R10
ZT29 HOLE-VIA-20R10
ZT74 HOLE-VIA-20R10
ZT82 HOLE-VIA-20R10
ZT79 HOLE-VIA-20R10
ZT68 HOLE-VIA-20R10
ZT60 HOLE-VIA-20R10
ZT58 HOLE-VIA-20R10
ZT41 HOLE-VIA-20R10
ZT9 HOLE-VIA-20R10
ZT7 HOLE-VIA-20R10
ZT8 HOLE-VIA-20R10

ZT57 HOLE-VIA-20R10
ZT1 HOLE-VIA-20R10
ZT80 HOLE-VIA-20R10
ZT73 HOLE-VIA-20R10
ZT75 HOLE-VIA-20R10
ZT63 HOLE-VIA-20R10
ZT61 HOLE-VIA-20R10
ZT54 HOLE-VIA-20R10
ZT51 HOLE-VIA-20R10
ZT42 HOLE-VIA-20R10
ZT64 HOLE-VIA-20R10
ZT76 HOLE-VIA-20R10
ZT62 HOLE-VIA-20R10
ZT59 HOLE-VIA-20R10
ZT21 HOLE-VIA-20R10

ZT22 HOLE-VIA-20R10
ZT25 HOLE-VIA-20R10
ZT3 HOLE-VIA-20R10
ZT32 HOLE-VIA-20R10
ZT31 HOLE-VIA-20R10
ZT26 HOLE-VIA-20R10
ZT23 HOLE-VIA-20R10
ZT19 HOLE-VIA-20R10
ZT17 HOLE-VIA-20R10
ZT15 HOLE-VIA-20R10
ZT13 HOLE-VIA-20R10
ZT12 HOLE-VIA-20R10
ZT14 HOLE-VIA-20R10
ZT18 HOLE-VIA-20R10
ZT20 HOLE-VIA-20R10

BOARD INFORMATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 4 OF 44	

CPU_VCORE DECOUPLING NETWORK

CPU_VCORE_SLEEP 5 34 38 39

R241 470 5% 1/16W MF 402

C25 10uF 20% 6.3V CERM 805 · C342 10uF 20% 6.3V CERM 805 · C344 10uF 20% 6.3V CERM 805

C346 10uF 20% 6.3V CERM 805 · C8 10uF 20% 6.3V CERM 805 · C153 0.1uF 20% 10V CERM 402

C12 2.2uF 20% 10V CERM 805 · C340 2.2uF 20% 10V CERM 805 · C193 0.1uF 20% 10V CERM 402

C223 0.1uF 20% 10V CERM 402 · C91 0.1uF 20% 10V CERM 402 · C114 0.1uF 20% 10V CERM 402 · C104 0.1uF 20% 10V CERM 402 · C103 0.1uF 20% 10V CERM 402 · C110 0.1uF 20% 10V CERM 402 · C190 0.1uF 20% 10V CERM 402 · C189 0.1uF 20% 10V CERM 402

C138 0.1uF 20% 10V CERM 402 · C191 0.1uF 20% 10V CERM 402 · C112 0.1uF 20% 10V CERM 402 · C168 0.1uF 20% 10V CERM 402 · C149 0.1uF 20% 10V CERM 402 · C111 0.1uF 20% 10V CERM 402 · C150 0.1uF 20% 10V CERM 402 · C105 0.1uF 20% 10V CERM 402

C154 0.1uF 20% 10V CERM 402 · C115 0.1uF 20% 10V CERM 402 · C113 0.1uF 20% 10V CERM 402 · C152 0.1uF 20% 10V CERM 402 · C151 0.1uF 20% 10V CERM 402 · C202 0.1uF 20% 10V CERM 402 · C201 0.1uF 20% 10V CERM 402 · C192 0.1uF 20% 10V CERM 402

MAXBUS_SLEEP 5 7 8 15 16 23 34 38

CPU_OVDD DECOUPLING NETWORK

R206 470 5% 1/16W MF 402

C72 0.1uF 20% 10V CERM 402 · C48 0.1uF 20% 10V CERM 402 · C38 0.1uF 20% 10V CERM 402 · C74 0.1uF 20% 10V CERM 402 · C275 0.1uF 20% 10V CERM 402 · C46 0.1uF 20% 10V CERM 402 · C47 0.1uF 20% 10V CERM 402 · C170 0.1uF 20% 10V CERM 402

C73 0.1uF 20% 10V CERM 402 · C39 0.1uF 20% 10V CERM 402 · C107 0.1uF 20% 10V CERM 402 · C90 0.1uF 20% 10V CERM 402 · C257 0.1uF 20% 10V CERM 402 · C272 0.1uF 20% 10V CERM 402 · C188 0.1uF 20% 10V CERM 402 · C155 0.1uF 20% 10V CERM 402 · C92 0.1uF 20% 10V CERM 402

C224 0.1uF 20% 10V CERM 402 · C40 0.1uF 20% 10V CERM 402 · C194 0.1uF 20% 10V CERM 402 · C203 0.1uF 20% 10V CERM 402 · C273 0.1uF 20% 10V CERM 402 · C41 0.1uF 20% 10V CERM 402 · C169 0.1uF 20% 10V CERM 402 · C139 0.1uF 20% 10V CERM 402 · C106 0.1uF 20% 10V CERM 402

MORE 0805 10UF CAPS ON VCORE
POWER SUPPLY PAGE (PG 33)

PLCAE SHORT CLOSE TO CENTER OF CPU

XW31 SM OMIT

25 ADT7460_VCORE_MON 1 2

C195 10UF 20% 6.3V CERM 805 · C347 10UF 20% 6.3V CERM 805 · C258 10UF 20% 6.3V CERM 805 · C345 10UF 20% 6.3V CERM 805

C156 10UF 20% 6.3V CERM 805 · C341 10UF 20% 6.3V CERM 805 · C225 10UF 20% 6.3V CERM 805 · C343 10UF 20% 6.3V CERM 805

PLACE BELOW CPU
IN FORMER L3 AREA

VDD: H8 H10 H12 J7 J9 J11 J13 K8 K10 K12 K14 L7 L9 L11 L13 M8 M10 M12

OVDD: B4 C2 C12 D5 E18 F2 G18 H3 J5 K2 L5 M3 N6 P2 P8 P11 R4 R13 R16 T6 T9 U2 U12 U16 V4 V7 V10 V14

AVDD: A8

CPU_BR_L (36)	D2	BR*
CPU_BG_L (36)	M1	BG*
NC	L4	TS*
CPU_PULLDOWN (5)	E11	A0
	H1	A1
	C11	A2
	G3	A3
CPU_ADDR<0> (36)	F10	A4
CPU_ADDR<1> (36)	L2	A5
CPU_ADDR<2> (36)	D11	A6
CPU_ADDR<3> (36)	D1	A7
CPU_ADDR<4> (36)	C10	A8
CPU_ADDR<5> (36)	G2	A9
CPU_ADDR<6> (36)	D12	A10
CPU_ADDR<7> (36)	L3	A11
CPU_ADDR<8> (36)	G4	A12
CPU_ADDR<9> (36)	T2	A13
CPU_ADDR<10> (36)	F4	A14
CPU_ADDR<11> (36)	V1	A15
CPU_ADDR<12> (36)	J4	A16
CPU_ADDR<13> (36)	R2	A17
CPU_ADDR<14> (36)	K5	A18
CPU_ADDR<15> (36)	W2	A19
CPU_ADDR<16> (36)	J2	A20
CPU_ADDR<17> (36)	K4	A21
CPU_ADDR<18> (36)	N4	A22
CPU_ADDR<19> (36)	J3	A23
CPU_ADDR<20> (36)	M5	A24
CPU_ADDR<21> (36)	P5	A25
CPU_ADDR<22> (36)	N3	A26
CPU_ADDR<23> (36)	T1	A27
CPU_ADDR<24> (36)	V2	A28
CPU_ADDR<25> (36)	U1	A29
CPU_ADDR<26> (36)	N5	A30
CPU_ADDR<27> (36)	W1	A31
CPU_ADDR<28> (36)	B12	A32
CPU_ADDR<29> (36)	C4	A33
CPU_ADDR<30> (36)	G10	A34
CPU_ADDR<31> (36)	B11	A35
NC	C1	AP0
NC	E3	AP1
NC	H6	AP2
NC	F5	AP3
NC	G7	AP4
CPU_TT<0> (36)	E5	TT0
CPU_TT<1> (36)	E6	TT1
CPU_TT<2> (36)	F6	TT2
CPU_TT<3> (36)	E9	TT3
CPU_TT<4> (36)	C5	TT4
CPU_TBST_L (36)	F11	TBST*
CPU_TSIZ<0> (36)	G6	TSIZ0
CPU_TSIZ<1> (36)	F7	TSIZ1
CPU_TSIZ<2> (36)	E7	TSIZ2
CPU_GBL_L (36)	E2	GBL*
CPU_WT_L (36)	D3	WT*
CPU_CI_L (36)	J1	CI*
CPU_AACK_L (36)	R1	AACK*
CPU_ARTRY_L (36)	N2	ARTRY*
CPU_SHD0_L (5)	E4	SHD0*
CPU_SHD1_L (5)	H5	SHD1*
CPU_HIT_L (36)	B2	HIT*

BVSEL	B7	CPU_BUS_VSEL (7)
SYSCLK	A10	SYSCLK_CPU (8 36)
CLKOUT	H2	CPU_CLKOUT_SPN
PLLCFG0	B8	CPU_PLL_CFG<0> (7)
PLLCFG1	C8	CPU_PLL_CFG<1> (7)
PLLCFG2	C7	CPU_PLL_CFG<2> (7)
PLLCFG3	D7	CPU_PLL_CFG<3> (7)
PLL_EXT	A7	CPU_PLL_CFG<4> (7)
DBG*	M2	CPU_DBG_L (8 36)
DRDY*	R3	CPU_DRDY_L (8 36)
DTI0	G1	CPU_EDTI (5)
DTI1	K1	CPU_DTI<0> (8 36)
DTI2	P1	CPU_DTI<1> (8 36)
DTI3	N1	CPU_DTI<2> (8 36)
TDI	B9	JTAG_CPU_TDI (5 23 39)
TDO	A4	JTAG_CPU_TDO_TP (39)
TMS	F1	JTAG_CPU_TMS (5 23 39)
TCK	C6	JTAG_CPU_TCK (5 23 39)
TRST*	A5	JTAG_CPU_TRST_L (5 23 39)
LSSDMODE*	E8	CPU_LSSD_MODE (5)
L1TSTCLK	G8	CPU_L1TSTCLK (5)
L2TSTCLK	B3	CPU_L2TSTCLK (5)
TA*	K6	CPU_TA_L (8 36)
TEA*	L1	CPU_TEA_L (8 36)
TBEN	E1	CPU_TBEN (5 8)
QREQ*	P4	CPU_QREQ_L (8 36)
QACK*	G5	CPU_QACK_L (8 36)
CKSTP_IN*	A3	
CKSTP_OUT*	B1	CPU_CHKSTP_OUT_L (5 39)
INT*	D4	MPIC_CPU_INT_L (5 14)
SMI*	F9	CPU_SMI_L (5 30)
MCP*	C9	CPU_MCP_L (5)
SRESET*	A2	CPU_SRESET_L (5 39)
HRESET*	D8	CPU_HRESET_L (5 7 23 39)
PMON_IN*	D9	CPU_PMONIN_L (5)
PMON_OUT*	A9	NC
BMODE0*	G9	CPU_EMODE0_L (7)
BMODE1*	F8	CPU_EMODE1_L (5)
EXT_QUAL	A11	CPU_PULLDOWN (5)
TEST0	A12	CPU_CHKS_L (5)
TEST1	B6	CPU_PULLUP (5)
TEST2	B10	
TEST3	E10	CPU_SRWX_L (5)
TEST4	D10	CPU_PULLDOWN (5)

GND: B5 C3 D6 D13 E17 F3 G17 H4 H7 H9 H11 H13 J6 J8 J10 J12 K7 K9 K11 K13 L6 L8 L10 L12 M4 M7 M9 M11 M13 N7 P3 P9 P12 R5 R14 R17 T7 T10 U3 U13 U17 V5 V8 V11 V15

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2733	1	IC,APOLLO7,1.X,1.3GHZ,1.XV CORE,85C	U43	CRITICAL	1_30_VCORE
337S2807	1	IC,APOLLO7,1.X,1.33GHZ,1.32V VCORE,85C	U43	CRITICAL	1_32_VCORE

OMIT
U43
1.33GHZ
APOLLO_MPC7447_360
BGA
(1 OF 3)
MPC7447

CPU INTERNAL PLL FILTERING

CPU_VCORE_SLEEP 5 34 38 39

R106 402 1% 1/16W MF 402

38 CPU_AVDD

C137 0.1uF 20% 10V CERM 402 · C136 2.2uF 20% 10V CERM 805

MPC7447 PULL-UPS

1_5V_MAXBUS
+1_5V_SLEEP
R702 0 5% 1/16W MF 603

1_8V_MAXBUS
+1_8V_SLEEP
R693 0 5% 1/16W MF 603

38 34 23 16 15 8 7 5 MAXBUS_SLEEP

8 5 CPU_TBEN	R58 10K	5% 1/16W MF 402
5 CPU_CHKS_L	R160 10K	5% 1/16W MF 402
5 CPU_SHD0_L	R73 10K	5% 1/16W MF 402
5 CPU_SHD1_L	R87 10K	5% 1/16W MF 402
5 CPU_MCP_L	R139 10K	5% 1/16W MF 402
5 CPU_LSSD_MODE	R108 10K	5% 1/16W MF 402
5 CPU_L2TSTCLK	R72 10K	5% 1/16W MF 402
39 5 CPU_CHKSTP_OUT_L	R57 1K	5% 1/16W MF 402
5 CPU_SRWX_L	R148 10K	5% 1/16W MF 402
5 CPU_PMONIN_L	R120 10K	5% 1/16W MF 402
5 CPU_EMODE1_L	R109 10K	5% 1/16W MF 402
5 CPU_PULLUP	R98 1K	5% 1/16W MF 402
39 23 7 5 CPU_HRESET_L	R107 10K	5% 1/16W MF 402
30 5 CPU_SMI_L	R129 10K	5% 1/16W MF 402
470OHM FOR BOOT BANGER 39 23 5 JTAG_CPU_TMS	R59 470	5% 1/16W MF 402
470OHM FOR BOOT BANGER 39 23 5 JTAG_CPU_TDI	R128 470	5% 1/16W MF 402
14 5 MPIC_CPU_INT_L	R79 10K	5% 1/16W MF 402
39 5 CPU_SRESET_L	R65 10K	5% 1/16W MF 402
5 CPU_L1TSTCLK	R130 10K	5% 1/16W MF 402
5 CPU_EDTI	R60 10K	5% 1/16W MF 402
39 23 5 JTAG_CPU_TCK	R97 10K	5% 1/16W MF 402
5 CPU_PULLDOWN	R61 470	5% 1/16W MF 402

MAXBUS_SLEEP 5 7 8 15 16 23 34 38

BBANG
470OHM FOR BOOT BANGER
R86 470 5% 1/16W MF 402

39 23 5 JTAG_CPU_TRST_L

NO_BBANG
R85 200 5% 1/16W MF 402

MPC7447 MAXBUS

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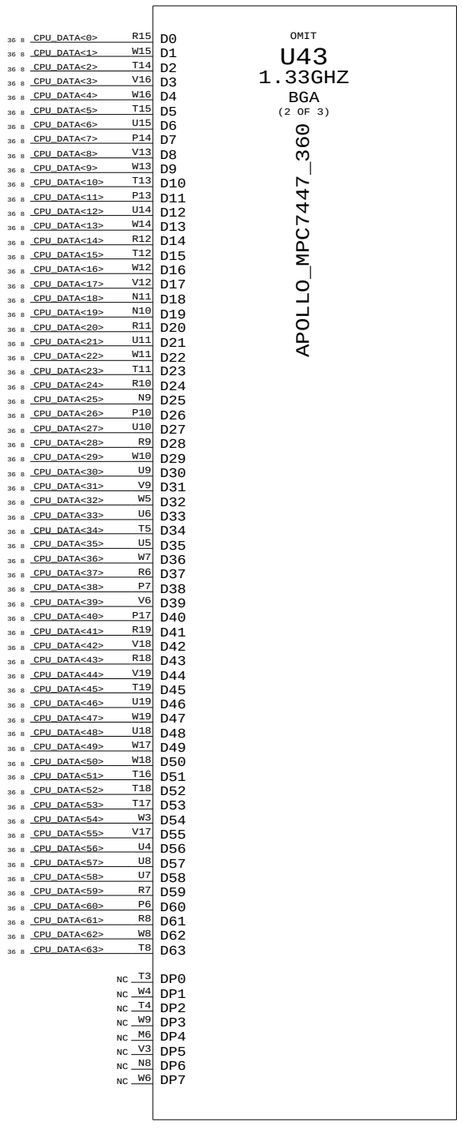
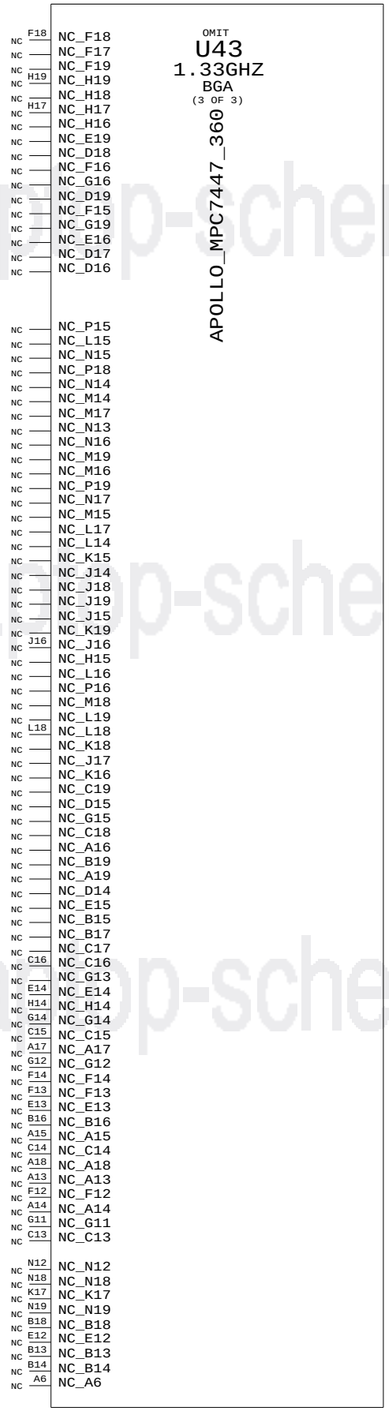
SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 5 OF 44	

BOOT BANGER - LMU PERORMS THIS FUNCTION IF NEEDED
SEE PAGE 22





MPC7447/BBANG

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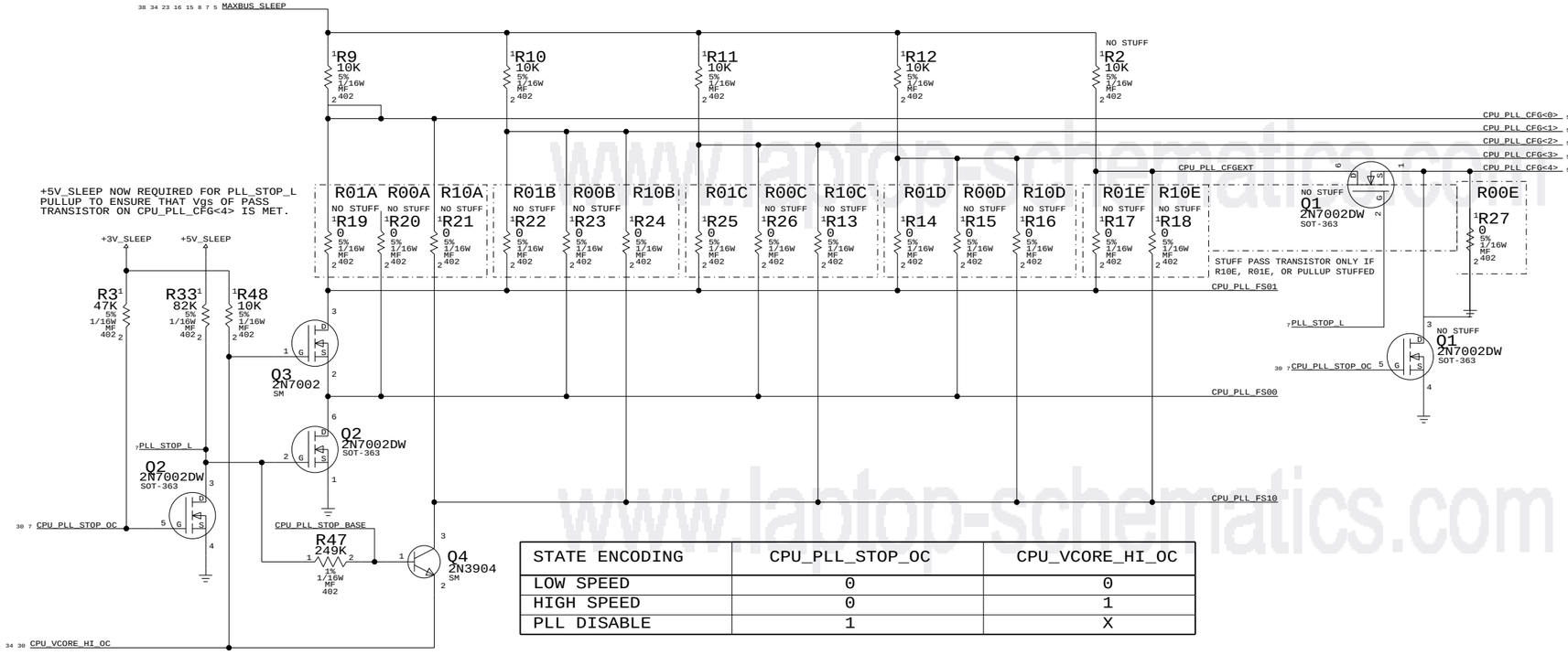
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 6 OF 44	

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

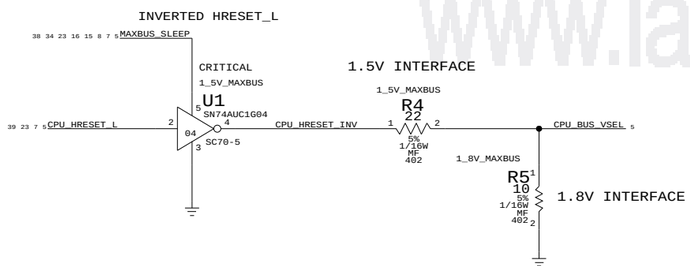
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 E	0123 ABCD HEX
0.0X	PLL OFF		0	1111 0F
1.0X	PLL BYPASS		0	0011 03
2.0X	333	267	0	0100 04
3.0X	500	400	0	1000 08
4.0X	667	533	0	1010 0A
5.0X	833	667	0	1011 0B
5.5X	917	733	0	1001 09
6.0X	1000	800	0	1101 0D
6.5X	1083	867	0	0101 05
7.0X	1167	933	0	0010 02
7.5X	1250	1000	0	0001 01
8.0X	1333	1067	0	1100 0C
8.5X	1417	1133	0	0110 06
9.0X	1500	1200	1	0111 17
9.5X	1583	1267	0	0111 07
10.0X	1667	1333	1	1010 1A
10.5X	1750	1400	1	1000 18
11.0X	1833	1467	1	1001 19
11.5X	1917	1533	0	0000 00
12.0X	2000	1600	1	1011 1B
12.5X	2083	1667	1	1111 1F
13.0X	2167	1733	1	0101 15
13.5X	2250	1800	0	1110 0E
14.0X	2333	1867	1	1100 1C
15.0X	2500	2000	1	0001 11
16.0X	2667	2133	1	1101 1D
17.0X	2833	2267	1	0000 10
18.0X	3000	2400	1	0010 12
20.0X	3333	2667	1	0011 13
21.0X	3500	2800	1	0100 14
24.0X	4000	3200	1	0110 16
28.0X	4667	3733	1	1110 1E

CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT

APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6582 | REV. C

SCALE NONE | SHT 7 OF 44

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

NO STUFF R642 10K	NO STUFF R135 10K	NO STUFF R123 10K	NO STUFF R153 10K	NO STUFF R166 10K	NO STUFF R179 10K	NO STUFF R651 10K	NO STUFF R178 10K
CPU_DATA<32>	CPU_DATA<33>	CPU_DATA<34>	CPU_DATA<35>	CPU_DATA<36>	CPU_DATA<37>	CPU_DATA<38>	CPU_DATA<39>
R136 10K	R643 10K	R639 10K	R657 10K	R664 10K	R673 10K	R143 10K	R674 10K
0: Disable Pull 1: Enable Pull (Default)	Analog_clk_en_h 0: Active 1: Active	DDR_IF_Drive_Pull 0: Active Low 1: Active High	ExtPLL_SDwn_Pol 0: Active High 1: Active Low	Spare	Spare	Spare	Spare

BIT 40 TO 47

MAXBUS_SLEEP

NO STUFF R122 10K	NO STUFF R142 10K	NO STUFF R164 10K	SSCG R134 10K	NO STUFF R184 10K	NO_SSCG R177 10K	NO_SSCG R152 10K	NO_SSCG R165 10K
CPU_DATA<40>	CPU_DATA<41>	CPU_DATA<42>	CPU_DATA<43>	CPU_DATA<44>	CPU_DATA<45>	CPU_DATA<46>	CPU_DATA<47>
R640 10K	R652 10K	R665 10K	NO_SSCG R644 10K	R683 10K	SSCG R675 10K	SSCG R658 10K	SSCG R666 10K
Spare	Spare	BIT2	BIT1	BIT0	Internal_spreadEn 0: PLL1 Active 1: Active	PCI1_Source_Clock 0: PLL1 (NO SPREAD) 1: PLL1 (SPREAD)	PCI0_Source_Clock 0: PLL0 (NO SPREAD) 1: PLL0 (SPREAD)

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

MAXBUS_SLEEP

SSCG R133 10K	SSCG R121 10K	NO STUFF R163 10K	NO STUFF R151 10K	NO STUFF R162 10K	NO STUFF R141 10K	NO STUFF R183 10K	NO STUFF R176 10K
CPU_DATA<48>	CPU_DATA<49>	CPU_DATA<50>	CPU_DATA<51>	CPU_DATA<52>	CPU_DATA<53>	CPU_DATA<54>	CPU_DATA<55>
NO_SSCG R645 10K	NO_SSCG R641 10K	NO STUFF R668 10K	R659 10K	R667 10K	R653 10K	NO STUFF R684 10K	R676 10K
BUF_REF_CLK_OUTEnable_h 1: Active	SelPLL4ExtSrc 1: External source	Spare	TI 1394b_workaround 1: TI PHY workaround	BIT2	BIT1	BIT0	Spare

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

R227 4.7 1/16W MF 402 5%
+1.5V_INTREPID_PLL → +1.5V_INTREPID_PLL7
C308 0.22UF 20% 6.3V CERM 402

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

VDD15A_7 (PLL6) H26 — CRITICAL

U45 INTREPID-REV2.1 BGA (1 OF 9)

CPU_BR_L	E29	BR	INPUT
CPU_BG_L	E26	BG	NO BUS KEEPER
CPU_TS_L	B27	TS	NO BUS KEEPER
CPU_ADDR<0>	D24	A_0	
CPU_ADDR<1>	D25	A_1	
CPU_ADDR<2>	A27	A_2	
CPU_ADDR<3>	E24	A_3	
CPU_ADDR<4>	G23	A_4	
CPU_ADDR<5>	B26	A_5	
CPU_ADDR<6>	A26	A_6	
CPU_ADDR<7>	D23	A_7	
CPU_ADDR<8>	A25	A_8	
CPU_ADDR<9>	E23	A_9	
CPU_ADDR<10>	J22	A_10	
CPU_ADDR<11>	B25	A_11	
CPU_ADDR<12>	H22	A_12	
CPU_ADDR<13>	G22	A_13	
CPU_ADDR<14>	D22	A_14	
CPU_ADDR<15>	B24	A_15	
CPU_ADDR<16>	B23	A_16	
CPU_ADDR<17>	E22	A_17	
CPU_ADDR<18>	J21	A_18	
CPU_ADDR<19>	G21	A_19	
CPU_ADDR<20>	E21	A_20	
CPU_ADDR<21>	A24	A_21	
CPU_ADDR<22>	D21	A_22	
CPU_ADDR<23>	A23	A_23	
CPU_ADDR<24>	H20	A_24	
CPU_ADDR<25>	B22	A_25	
CPU_ADDR<26>	H21	A_26	
CPU_ADDR<27>	A22	A_27	
CPU_ADDR<28>	E20	A_28	
CPU_ADDR<29>	B21	A_29	
CPU_ADDR<30>	D20	A_30	
CPU_ADDR<31>	A21	A_31	
CPU_CI_L	G26	CI	
CPU_GBL_L	A29	GBL	
CPU_TBST_L	A28	TBST	
CPU_TSIZ<0>	G24	TSIZ_0	
CPU_TSIZ<1>	H24	TSIZ_1	
CPU_TSIZ<2>	D26	TSIZ_2	
CPU_TT<0>	E25	TT_0	
CPU_TT<1>	G25	TT_1	
CPU_TT<2>	B28	TT_2	
CPU_TT<3>	D27	TT_3	
CPU_TT<4>	J25	TT_4	
CPU_WT_L	D28	WT	
CPU_AACK_L	B29	AACK	NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY	NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT	INPUT - PU
CPU_QREQ_L	A32	QREQ	INPUT - PD
CPU_QACK_L	G27	QACK	NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ	
INT_SUSPEND_ACK_L	AM8	SUSPENDACK	
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - ?
SYSCLK_CPU_UF	J15	CPU_CLK	NO BUS KEEPER - ?
CPU_TBEN	A31	TBEN	NO BUS KEEPER - PU
INT_CPUFB_IN	J24	CPU_FB_IN	
INT_CPUFB_OUT	H16	CPU_FB_OUT	NO BUS KEEPER - PU
SYSCLK_LA_TP	G8	ANALYZER_CLK	
CPU_CLK_EN	AH9	STOPCPUCLK	INPUT - PU
		DTI_0	NO BUS KEEPER - ?
		DTI_1	NO BUS KEEPER - ?
		DTI_2	NO BUS KEEPER - ?
		TA	NO BUS KEEPER - PU
		TEA	NO BUS KEEPER - PU

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)
INTREPID OUTPUTS HIGH BY DEFAULT
VSSA_7 (PLL6) H25

MAXBUS INTERFACE

D_0	D10	CPU_DATA<0>	6 36
D_1	G12	CPU_DATA<1>	6 36
D_2	E11	CPU_DATA<2>	6 36
D_3	H11	CPU_DATA<3>	6 36
D_4	B9	CPU_DATA<4>	6 36
D_5	B8	CPU_DATA<5>	6 36
D_6	A9	CPU_DATA<6>	6 36
D_7	A8	CPU_DATA<7>	6 36
D_8	E12	CPU_DATA<8>	6 36
D_9	D11	CPU_DATA<9>	6 36
D_10	B10	CPU_DATA<10>	6 36
D_11	J13	CPU_DATA<11>	6 36
D_12	A10	CPU_DATA<12>	6 36
D_13	D12	CPU_DATA<13>	6 36
D_14	E13	CPU_DATA<14>	6 36
D_15	G13	CPU_DATA<15>	6 36
D_16	B11	CPU_DATA<16>	6 36
D_17	D13	CPU_DATA<17>	6 36
D_18	A11	CPU_DATA<18>	6 36
D_19	G14	CPU_DATA<19>	6 36
D_20	H14	CPU_DATA<20>	6 36
D_21	E14	CPU_DATA<21>	6 36
D_22	B12	CPU_DATA<22>	6 36
D_23	G15	CPU_DATA<23>	6 36
D_24	B13	CPU_DATA<24>	6 36
D_25	H15	CPU_DATA<25>	6 36
D_26	D14	CPU_DATA<26>	6 36
D_27	B14	CPU_DATA<27>	6 36
D_28	A12	CPU_DATA<28>	6 36
D_29	G16	CPU_DATA<29>	6 36
D_30	E15	CPU_DATA<30>	6 36
D_31	J16	CPU_DATA<31>	6 36
D_32	D15	CPU_DATA<32>	6 8 36
D_33	A14	CPU_DATA<33>	6 8 36
D_34	A13	CPU_DATA<34>	6 8 36
D_35	D16	CPU_DATA<35>	6 8 36
D_36	E16	CPU_DATA<36>	6 8 36
D_37	G17	CPU_DATA<37>	6 8 36
D_38	B15	CPU_DATA<38>	6 8 36
D_39	H17	CPU_DATA<39>	6 8 36
D_40	A15	CPU_DATA<40>	6 8 36
D_41	B16	CPU_DATA<41>	6 8 36
D_42	E17	CPU_DATA<42>	6 8 36
D_43	A16	CPU_DATA<43>	6 8 36
D_44	J18	CPU_DATA<44>	6 8 36
D_45	H18	CPU_DATA<45>	6 8 36
D_46	D17	CPU_DATA<46>	6 8 36
D_47	G18	CPU_DATA<47>	6 8 36
D_48	A17	CPU_DATA<48>	6 8 36
D_49	B17	CPU_DATA<49>	6 8 36
D_50	E18	CPU_DATA<50>	6 8 36
D_51	B18	CPU_DATA<51>	6 8 36
D_52	D18	CPU_DATA<52>	6 8 36
D_53	A18	CPU_DATA<53>	6 8 36
D_54	A19	CPU_DATA<54>	6 8 36
D_55	H19	CPU_DATA<55>	6 8 36
D_56	B19	CPU_DATA<56>	6 8 36
D_57	J19	CPU_DATA<57>	6 8 36
D_58	A20	CPU_DATA<58>	6 8 36
D_59	D19	CPU_DATA<59>	6 8 36
D_60	E19	CPU_DATA<60>	6 8 36
D_61	G19	CPU_DATA<61>	6 8 36
D_62	B20	CPU_DATA<62>	6 8 36
D_63	G20	CPU_DATA<63>	6 8 36
DBG	A30	CPU_DBG_L	5 8 36
DRDY	G28	CPU_DRDY_L	5 8 36
DTI_0	K25	CPU_DTI<0>	5 36
DTI_1	D29	CPU_DTI<1>	5 36
DTI_2	B30	CPU_DTI<2>	5 36
TA	E27	CPU_TA_L	5 8 36
TEA	E28	CPU_TEA_L	5 8 36

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

R197 511 1% 1/16W MF 402
R144 0 5% 1/16W MF 402 (SYSCLK_CPU → SYSCLK_CPU_UF)
R137 1K 1% 1/16W MF 402

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

INT_CPUFB_OUT	R167 0	INT_CPUFB_OUT_SHORT	R215 0	INT_CPUFB_OUT_NORM
			NO STUFF R225 0	INT_CPUFB_IN
			R226 0	
			R208 0	INT_CPUFB_IN_NORM
			NO STUFF R196 0	
			NO STUFF R207 0	INT_CPUFB_LONG

MAXBUS PULL-UPS

MAXBUS_SLEEP

CPU_TS_L	CPU_TA_L	CPU_ARTRY_L	CPU_BR_L	CPU_HIT_L	CPU_DRDY_L	CPU_TEA_L	CPU_AACK_L
RP21 10K	RP21 10K	RP21 10K	RP23 10K	RP24 10K	RP23 10K	RP23 10K	RP23 10K
CPU_DBG_L	CPU_BG_L	CPU_AREQ_L					
RP24 10K	RP21 10K	RP24 10K					

5% 1/16W SM1

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

NO STUFF R140 10K	NO STUFF R161 10K	NO STUFF R175 10K	NO STUFF R132 10K	NO STUFF R131 10K	NO STUFF R150 10K	R174 10K	NO STUFF R182 10K
CPU_DATA<56>	CPU_DATA<57>	CPU_DATA<58>	CPU_DATA<59>	CPU_DATA<60>	CPU_DATA<61>	CPU_DATA<62>	CPU_DATA<63>
R654 10K	R669 10K	R677 10K	R646 10K	R647 10K	R660 10K	NO STUFF R678 10K	R685 10K
Spare	Spare	Spare	PCI1_REQ2_L / PCI1_GNT2_L 0: GPIO 1: GPIO	PCI1_REQ1_L / PCI1_GNT1_L 0: GPIO 1: GPIO	PCI1_REQ0_L / PCI1_GNT0_L 0: GPIO 1: GPIO	Firewire PHY interface 0: Legacy interface 1: B-mode interface	Processor Bus Mode 0: 60X Bus (63) 1: GPIO

5% 1/16W MF 402

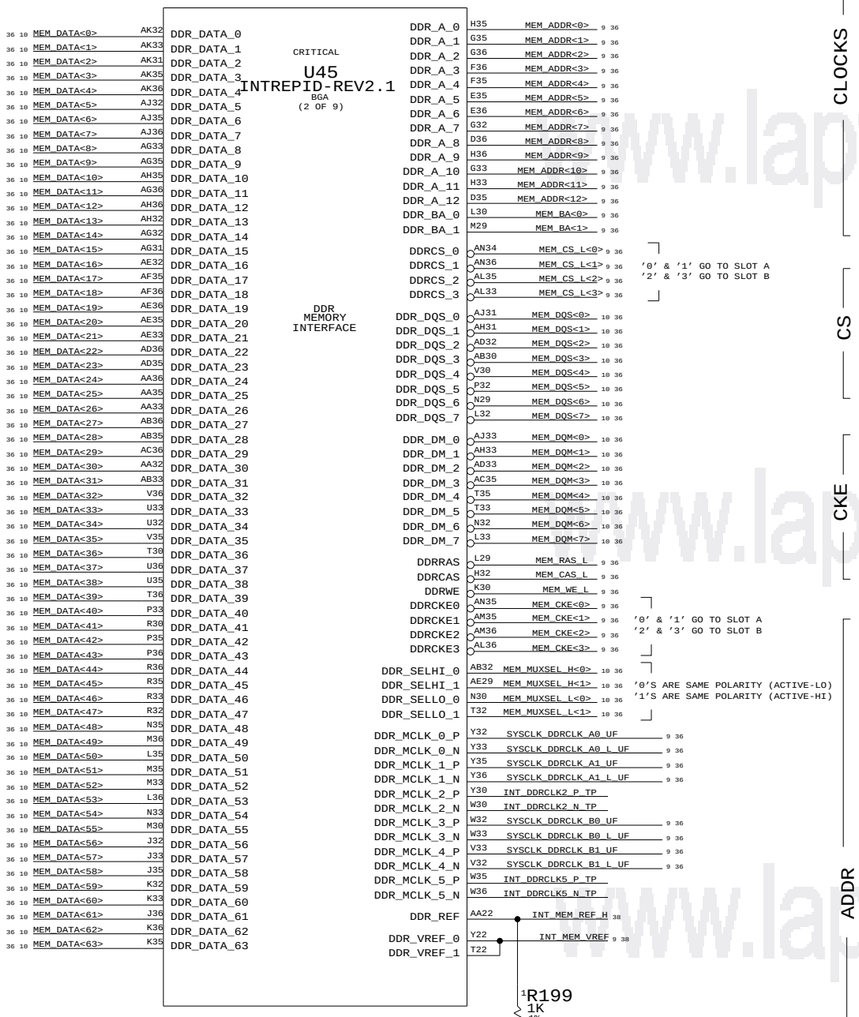
Intrepid MaxBus

APPLE COMPUTER INC.

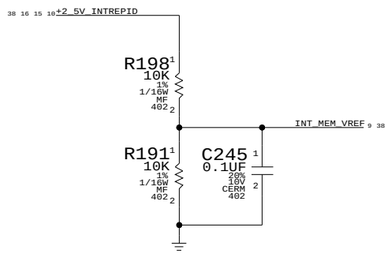
SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 8 OF 44	

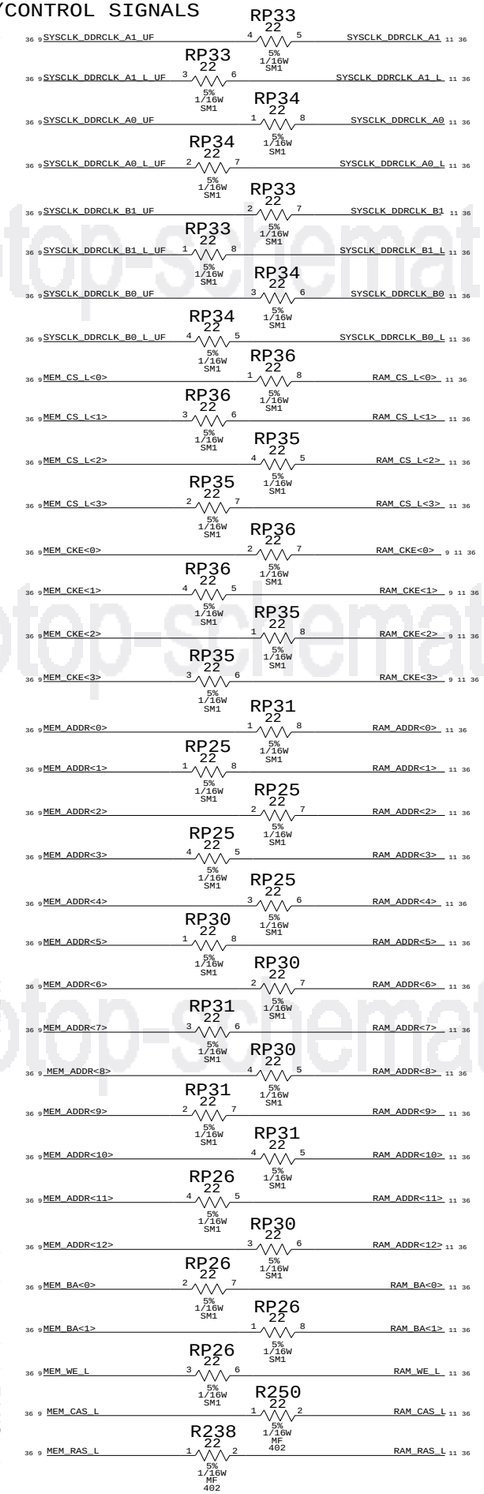
SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

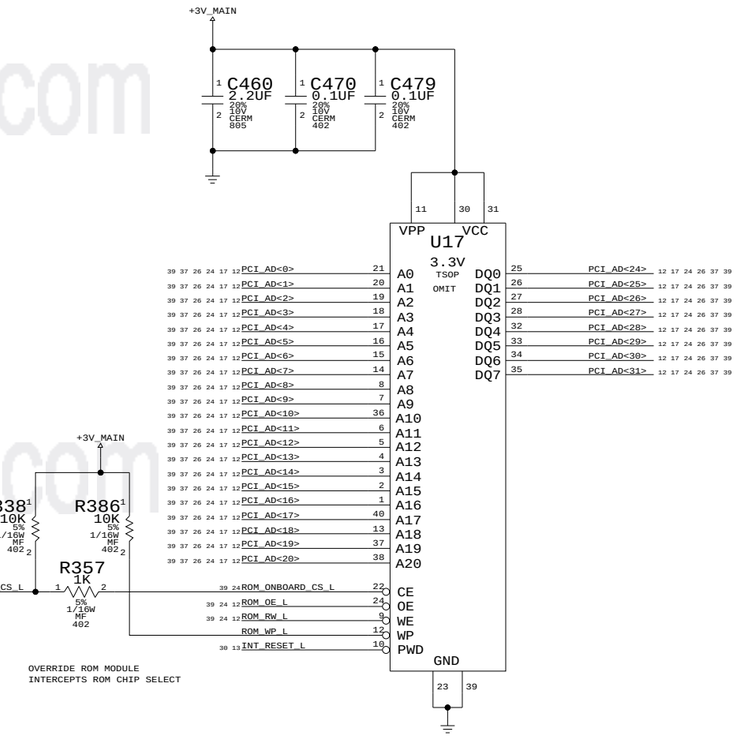


MEM_VREF



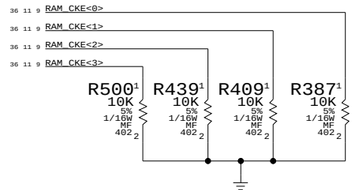


1MB BOOT ROM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2103	1	IC, BOOTROM,Q16, SERVICE_BOM	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF



INT - DDR/BOOTROM

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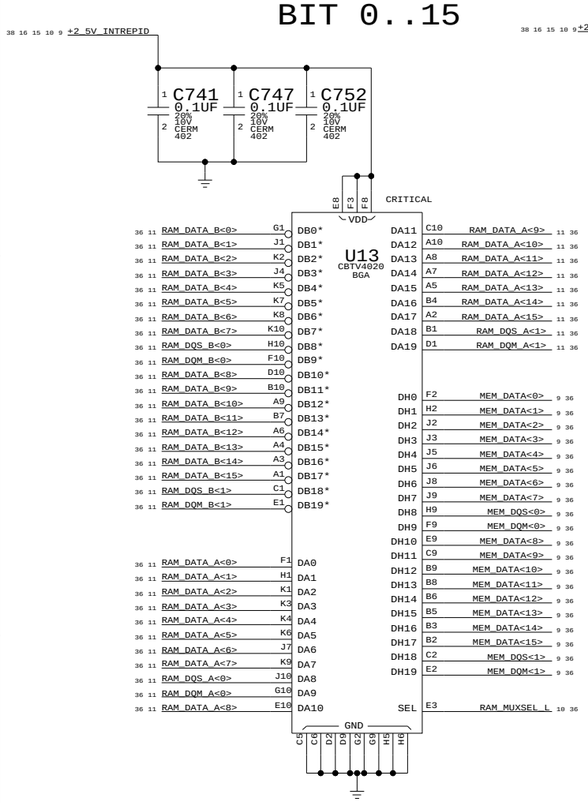
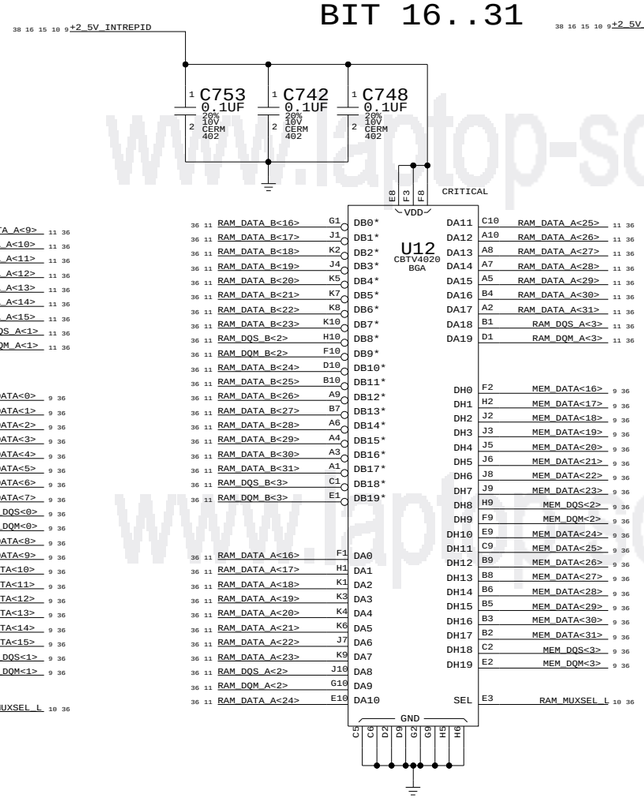
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 9 OF 44	

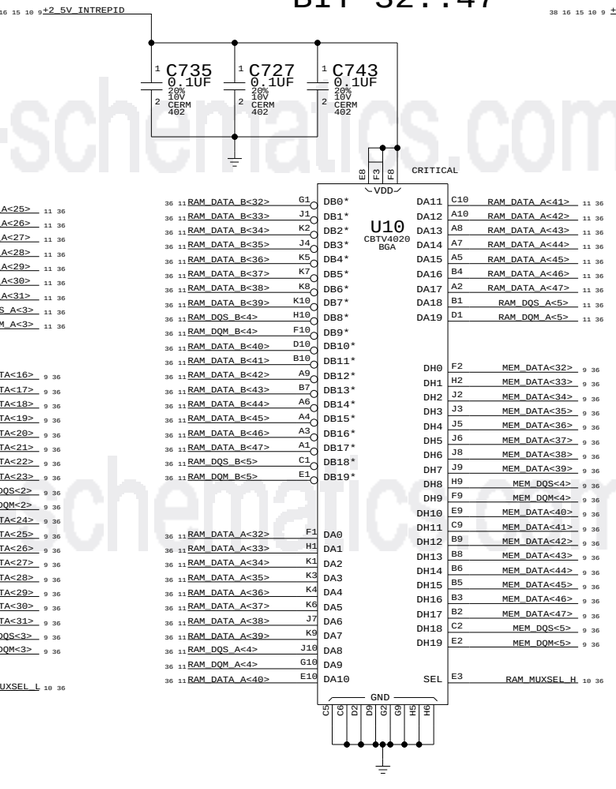
BIT 0..15



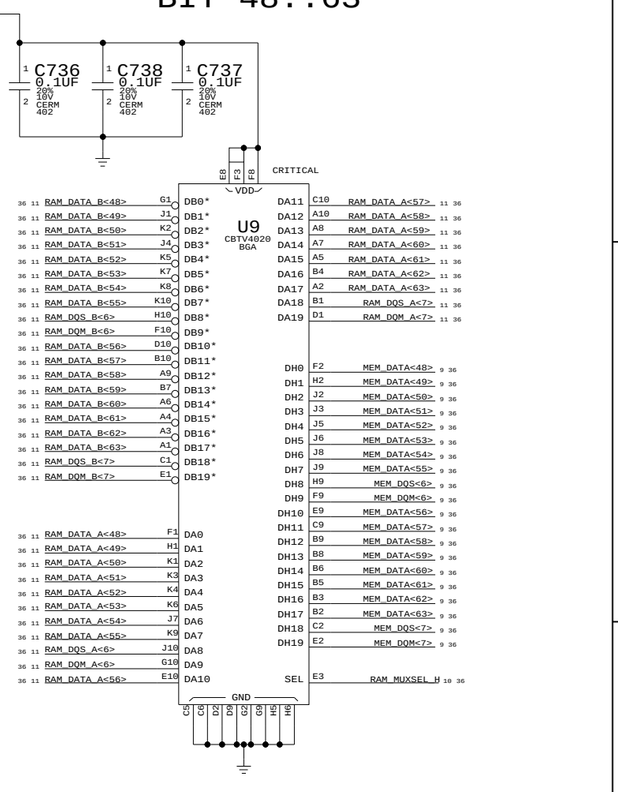
BIT 16..31



BIT 32..47



BIT 48..63



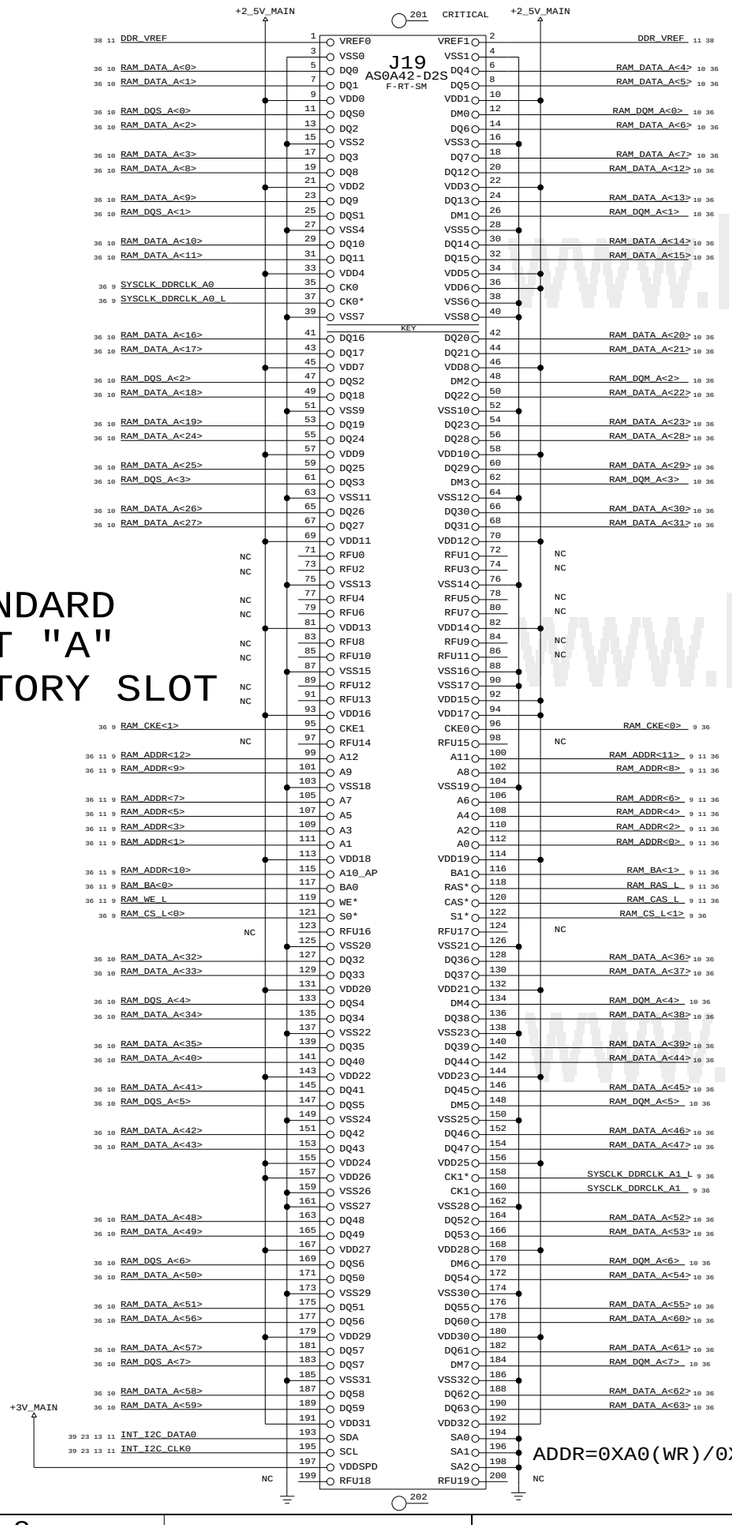
SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

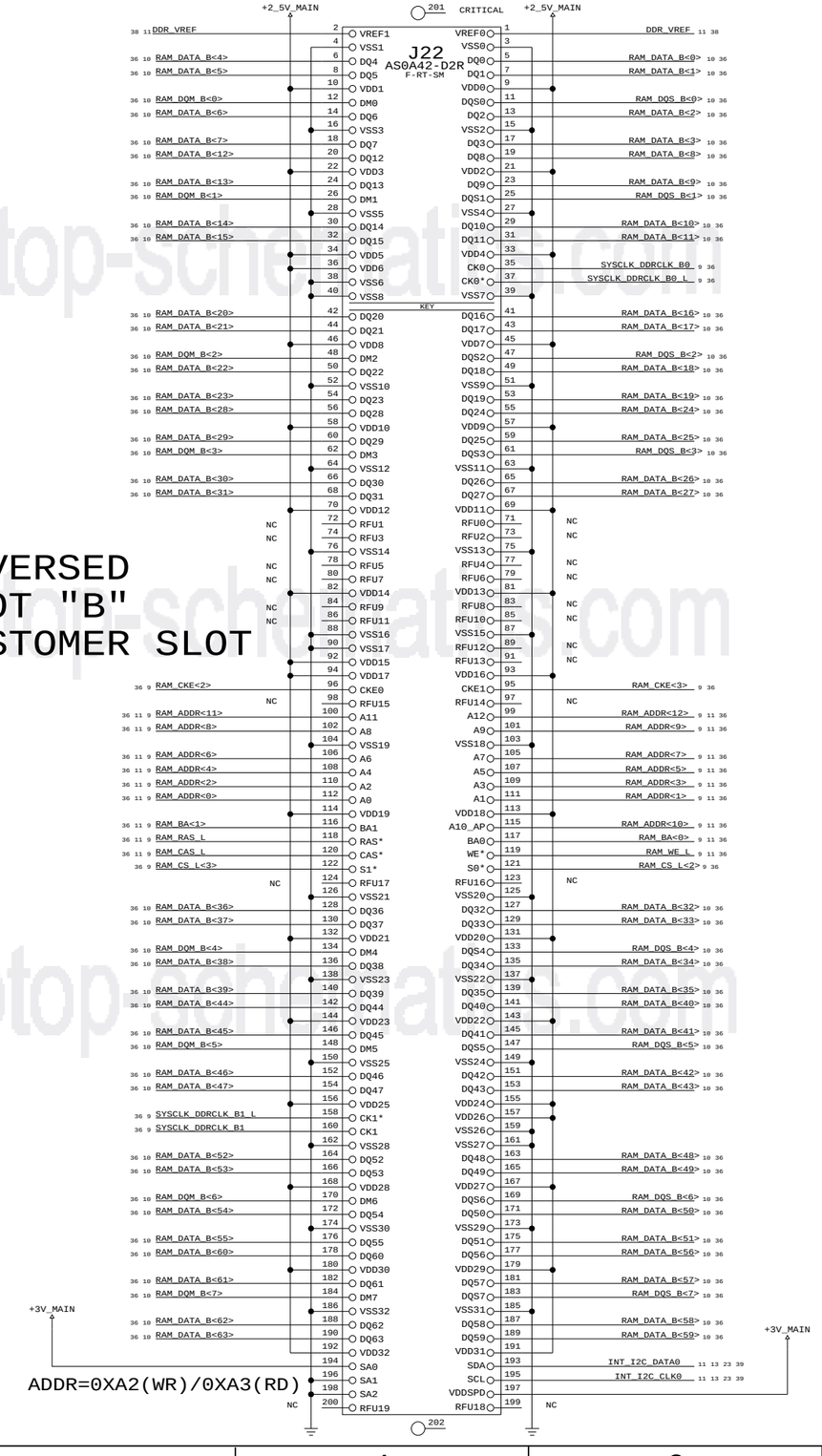
ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG

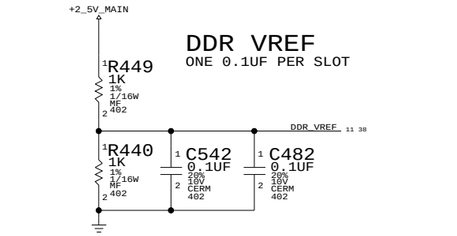
16BIT 2:1 DDR MUXES

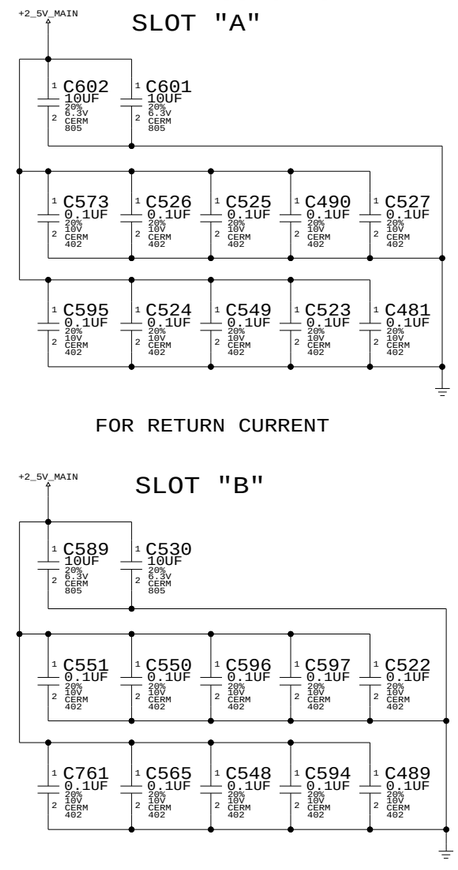
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 10 OF 44	









DDR SODIMM CONNS

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SIZE	DRAWING NUMBER	REV.
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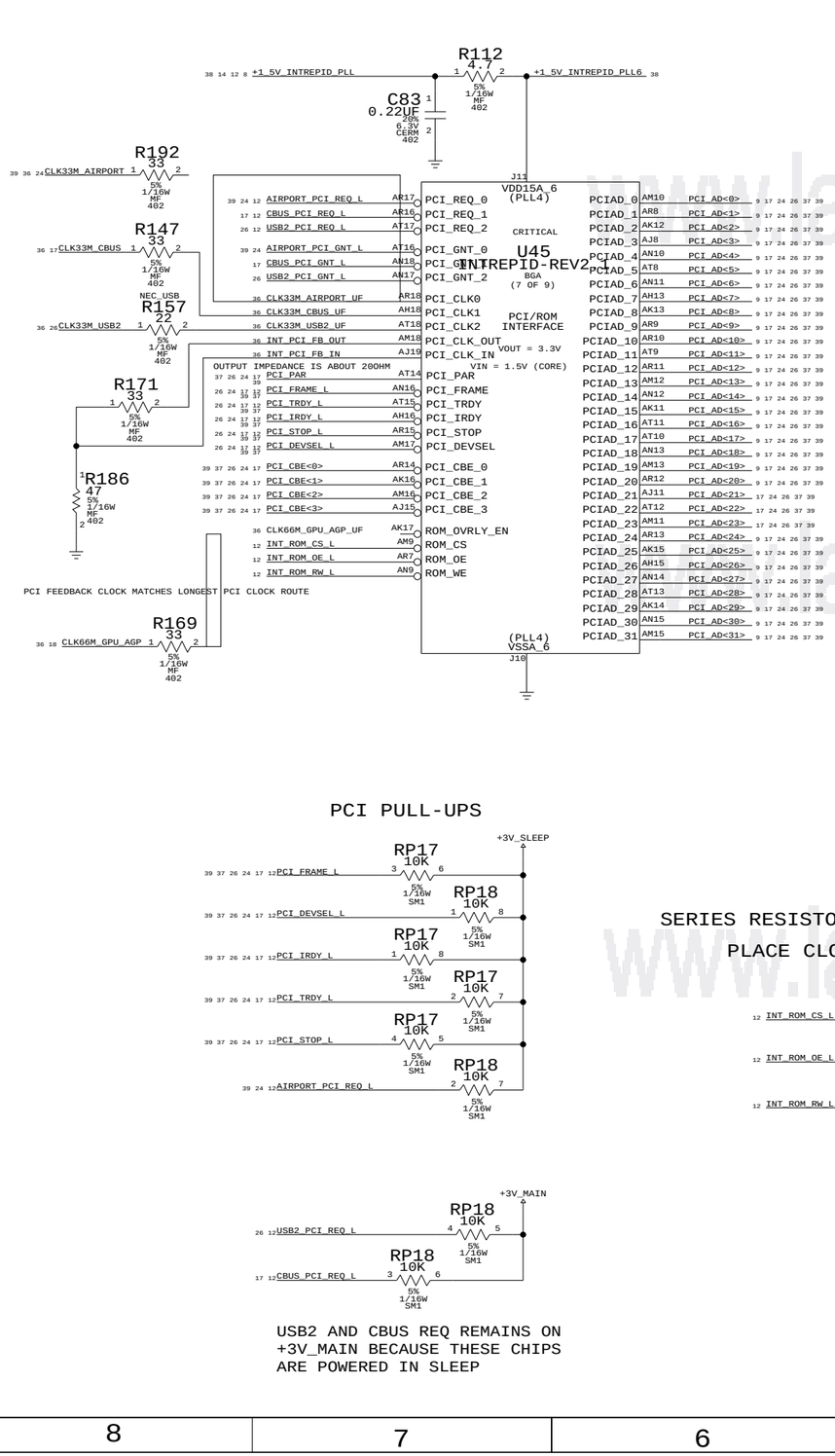
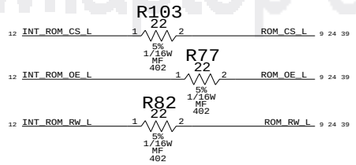
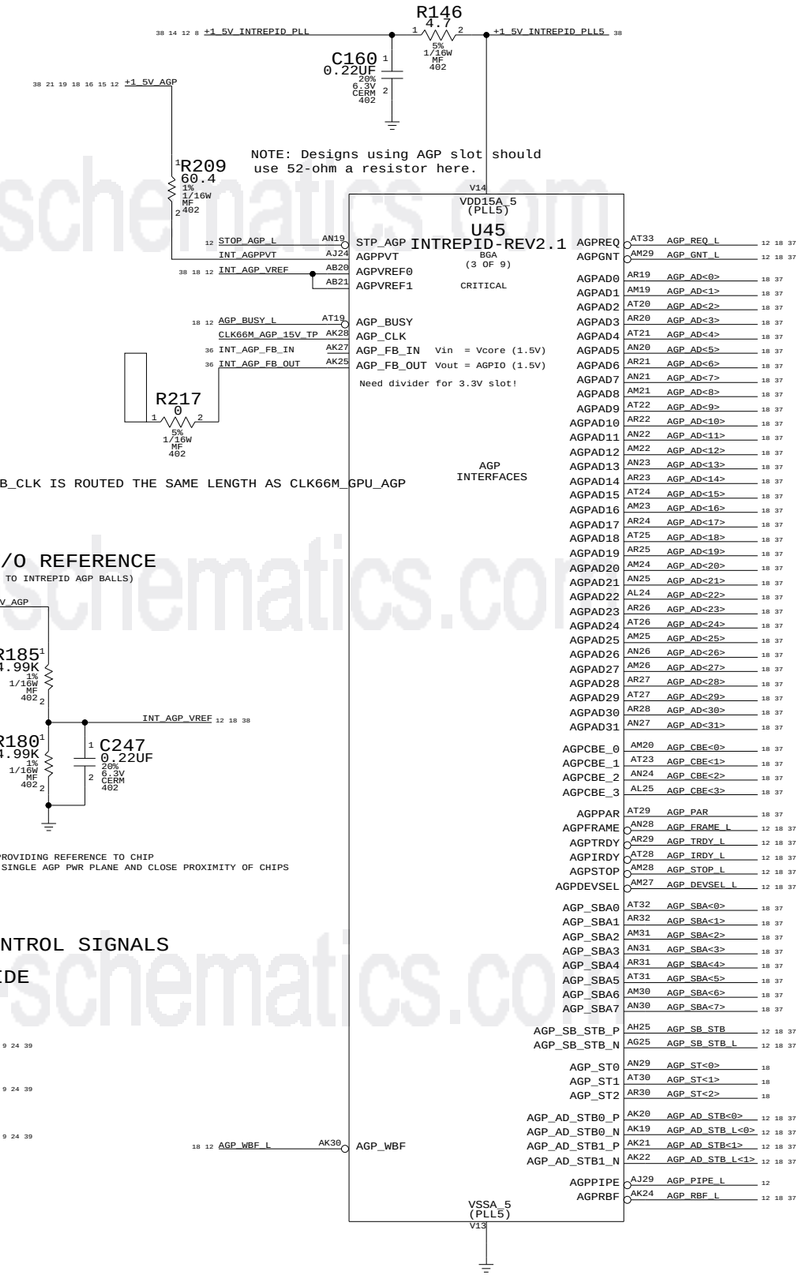
SCALE NONE

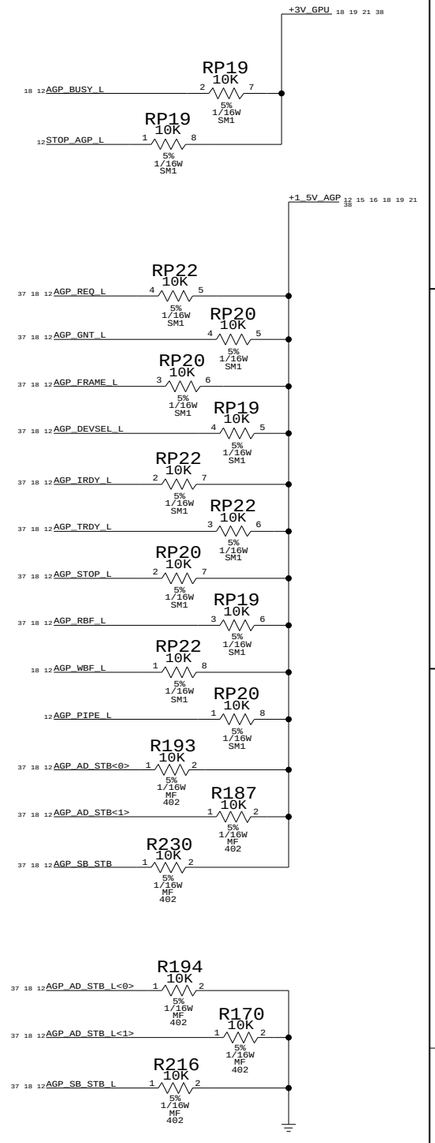
SHT 11 OF 44



USB2 AND CBUS REQ REMAINS ON +3V_MAIN BECAUSE THESE CHIPS ARE POWERED IN SLEEP







INTREPID AGP/PCI

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SIZE	DRAWING NUMBER	REV.
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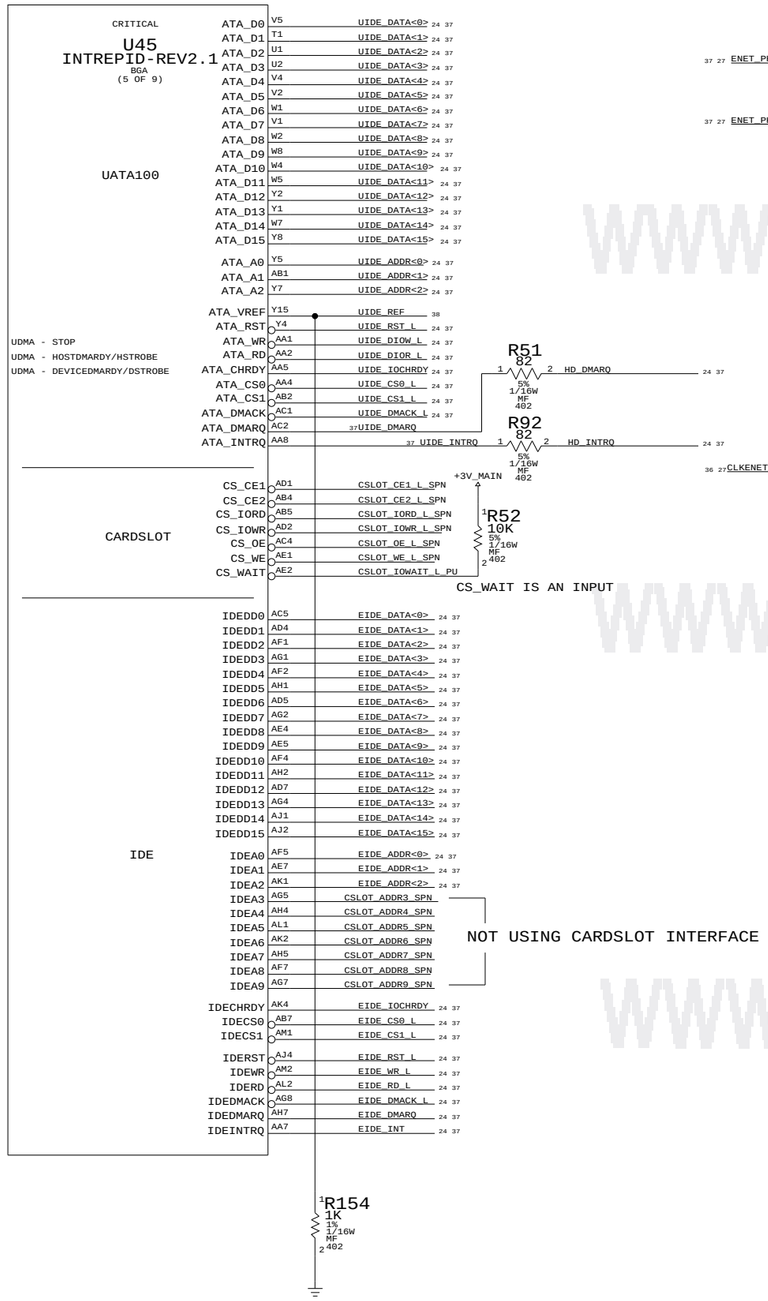
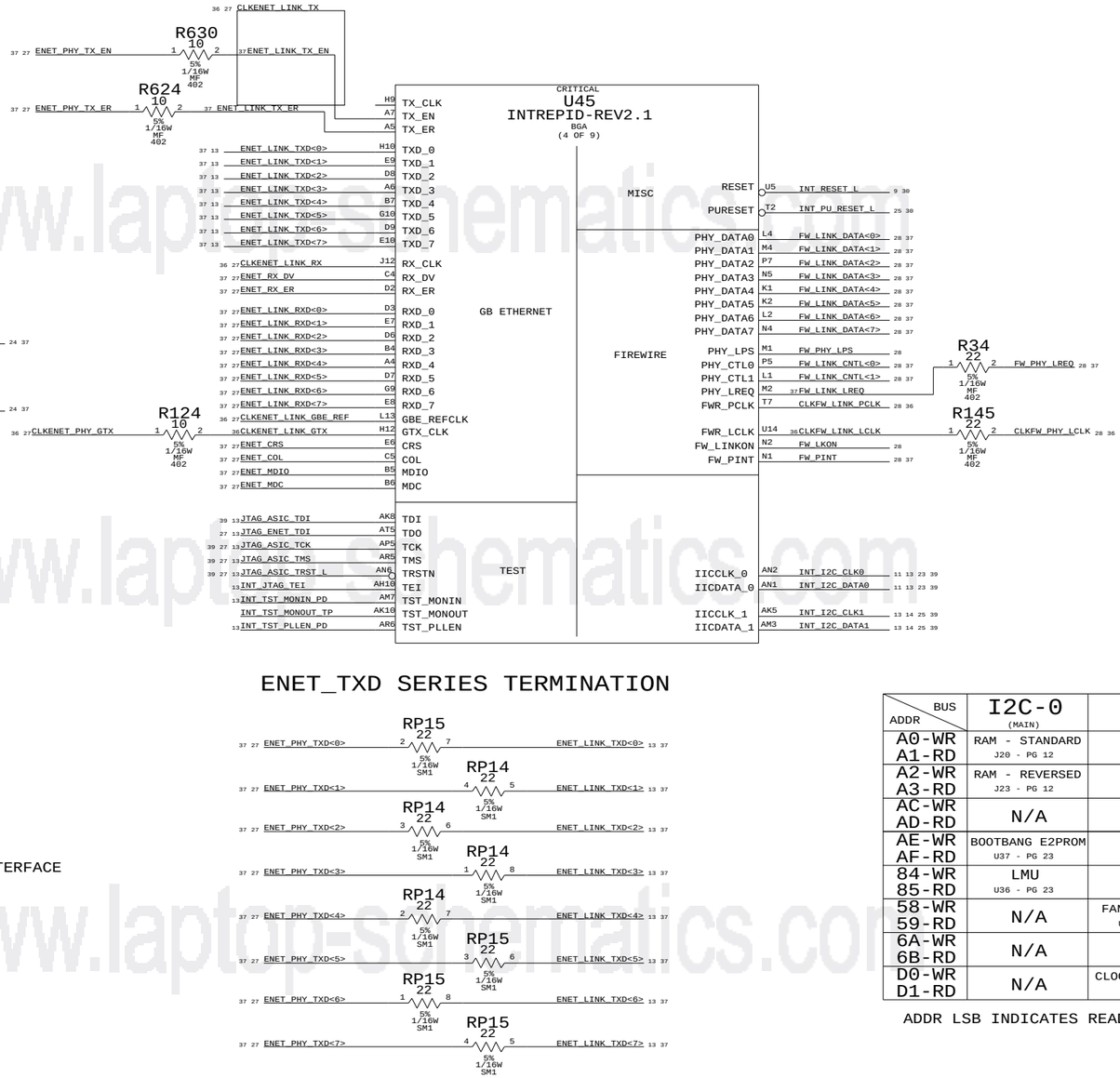
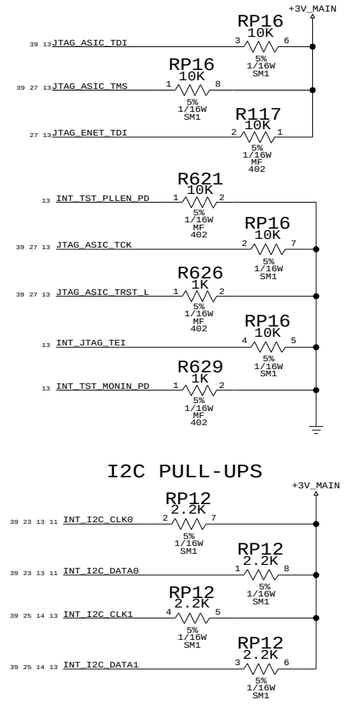
SCALE: NONE	SHT 12 OF 44	







ENET_TXD SERIES TERMINATION

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

ADDR \ BUS	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U3 - PG 24	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J12 - PG 24	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A

ADDR LSB INDICATES READ (’1’) OR WRITE (’0’) MODES

INT - ENET/FW/UATA EIDE/I2C

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SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 13 OF 44	

USB PORT ASSIGNMENTS

PORT A - RIGHT USB 1

PORT B - UNUSED

PORT C - LEFT USB

PORT D - UNUSED

PORT E - BLUETOOTH

PORT F - MODEM

USB POWER FAULT SIGNALS

HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R100	NO_SSCG

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y1	ALT FOR SIWARD

INT - USB/GPIOS/I2S

APPLE COMPUTER INC.

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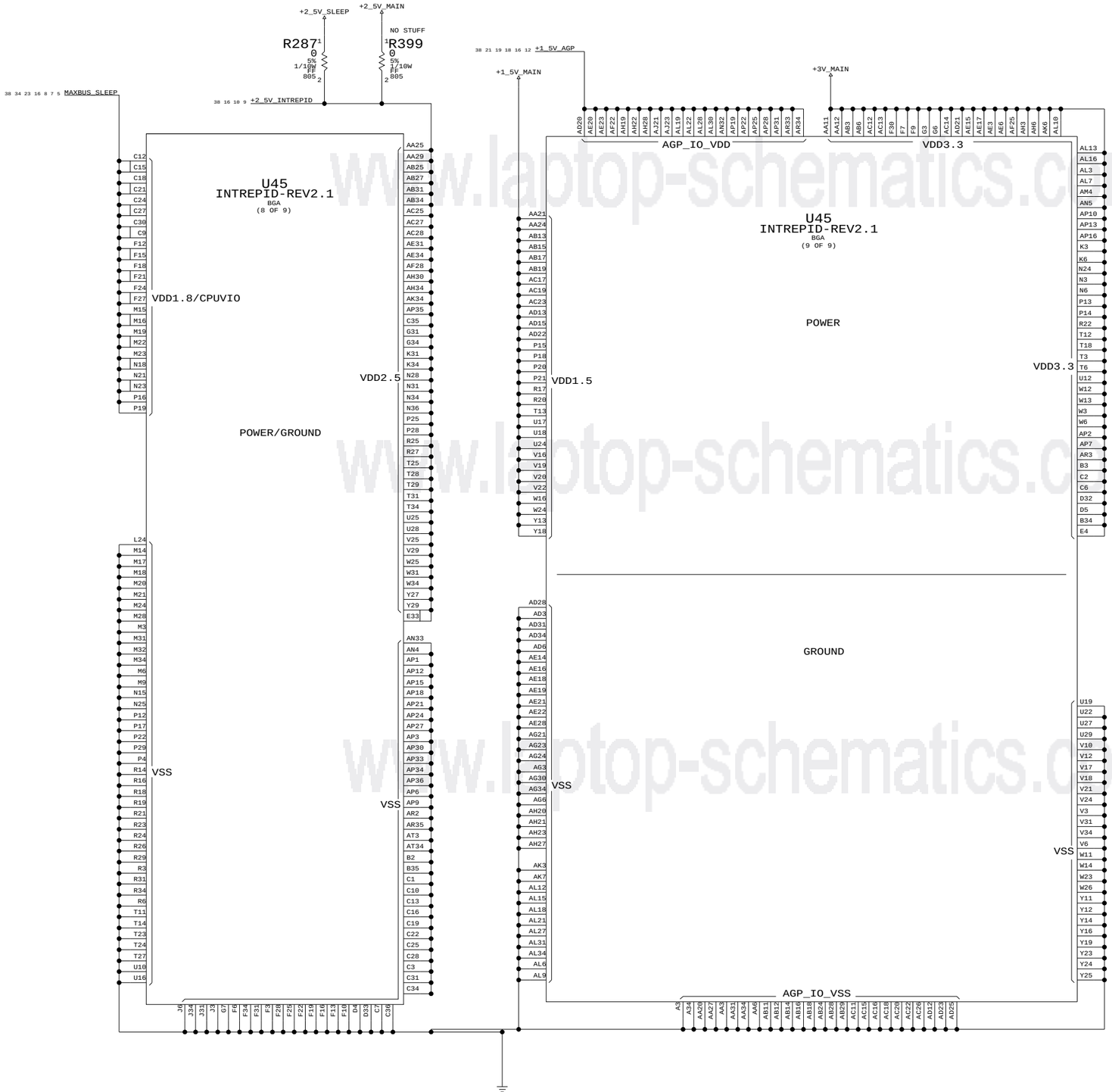

Intrepid Power

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SCALE	SHT	OF
NONE	15	44

INTREPID MAXBUS DECOUPLING

38 34 23 15 8 7 6 MAXBUS_SLEEP

24 Balls
4 X 10UF (0805)
32 X 0.22UF (0402)

C204 10uF 20% 6.3V CERM 805 · C348 10uF 20% 6.3V CERM 805 · C236 10uF 20% 6.3V CERM 805 · C196 10uF 20% 6.3V CERM 805

C239 0.22uF 20% 6.3V CERM 402 · C240 0.22uF 20% 6.3V CERM 402 · C350 0.22uF 20% 6.3V CERM 402 · C312 0.22uF 20% 6.3V CERM 402 · C176 0.22uF 20% 6.3V CERM 402 · C288 0.22uF 20% 6.3V CERM 402 · C313 0.22uF 20% 6.3V CERM 402 · C94 0.22uF 20% 6.3V CERM 402 · C286 0.22uF 20% 6.3V CERM 402 · C158 0.22uF 20% 6.3V CERM 402

C174 0.22uF 20% 6.3V CERM 402 · C206 0.22uF 20% 6.3V CERM 402 · C259 0.22uF 20% 6.3V CERM 402 · C237 0.22uF 20% 6.3V CERM 402 · C238 0.22uF 20% 6.3V CERM 402 · C95 0.22uF 20% 6.3V CERM 402 · C117 0.22uF 20% 6.3V CERM 402 · C241 0.22uF 20% 6.3V CERM 402 · C260 0.22uF 20% 6.3V CERM 402 · C314 0.22uF 20% 6.3V CERM 402

C173 0.22uF 20% 6.3V CERM 402 · C171 0.22uF 20% 6.3V CERM 402 · C175 0.22uF 20% 6.3V CERM 402 · C226 0.22uF 20% 6.3V CERM 402 · C172 0.22uF 20% 6.3V CERM 402 · C207 0.22uF 20% 6.3V CERM 402 · C118 0.22uF 20% 6.3V CERM 402 · C287 0.22uF 20% 6.3V CERM 402 · C119 0.22uF 20% 6.3V CERM 402 · C349 0.22uF 20% 6.3V CERM 402

C205 0.22uF 20% 6.3V CERM 402 · C209 0.22uF 20% 6.3V CERM 402

INTREPID CORE DECOUPLING

+1_5V_MAIN

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

C128 10uF 20% 6.3V CERM 805 · C101 10uF 20% 6.3V CERM 805 · C157 10uF 20% 6.3V CERM 805 · C315 10uF 20% 6.3V CERM 805

C147 0.22uF 20% 6.3V CERM 402 · C243 0.22uF 20% 6.3V CERM 402 · C262 0.22uF 20% 6.3V CERM 402 · C242 0.22uF 20% 6.3V CERM 402 · C227 0.22uF 20% 6.3V CERM 402 · C181 0.22uF 20% 6.3V CERM 402 · C142 0.22uF 20% 6.3V CERM 402 · C215 0.22uF 20% 6.3V CERM 402 · C278 0.22uF 20% 6.3V CERM 402 · C264 0.22uF 20% 6.3V CERM 402

C244 0.22uF 20% 6.3V CERM 402 · C212 0.22uF 20% 6.3V CERM 402 · C178 0.22uF 20% 6.3V CERM 402 · C179 0.22uF 20% 6.3V CERM 402 · C177 0.22uF 20% 6.3V CERM 402 · C159 0.22uF 20% 6.3V CERM 402 · C161 0.22uF 20% 6.3V CERM 402 · C162 0.22uF 20% 6.3V CERM 402 · C280 0.22uF 20% 6.3V CERM 402 · C279 0.22uF 20% 6.3V CERM 402

C144 0.22uF 20% 6.3V CERM 402 · C246 0.22uF 20% 6.3V CERM 402 · C211 0.22uF 20% 6.3V CERM 402 · C263 0.22uF 20% 6.3V CERM 402 · C180 0.22uF 20% 6.3V CERM 402 · C213 0.22uF 20% 6.3V CERM 402 · C197 0.22uF 20% 6.3V CERM 402 · C208 0.22uF 20% 6.3V CERM 402 · C214 0.22uF 20% 6.3V CERM 402

INTREPID AGP I/O DECOUPLING

38 21 19 18 15 12 +1_5V_AGP

21 Balls
4 X 10UF (0805)
24 X 0.22UF (0402)

C371 10uF 20% 6.3V CERM 805 · C231 10uF 20% 6.3V CERM 805 · C281 10uF 20% 6.3V CERM 805 · C394 10uF 20% 6.3V CERM 805

C356 0.22uF 20% 6.3V CERM 402 · C297 0.22uF 20% 6.3V CERM 402 · C268 0.22uF 20% 6.3V CERM 402 · C217 0.22uF 20% 6.3V CERM 402 · C355 0.22uF 20% 6.3V CERM 402 · C267 0.22uF 20% 6.3V CERM 402 · C250 0.22uF 20% 6.3V CERM 402 · C298 0.22uF 20% 6.3V CERM 402 · C377 0.22uF 20% 6.3V CERM 402 · C216 0.22uF 20% 6.3V CERM 402

C228 0.22uF 20% 6.3V CERM 402 · C230 0.22uF 20% 6.3V CERM 402 · C265 0.22uF 20% 6.3V CERM 402 · C378 0.22uF 20% 6.3V CERM 402 · C357 0.22uF 20% 6.3V CERM 402 · C229 0.22uF 20% 6.3V CERM 402 · C325 0.22uF 20% 6.3V CERM 402 · C393 0.22uF 20% 6.3V CERM 402 · C324 0.22uF 20% 6.3V CERM 402 · C323 0.22uF 20% 6.3V CERM 402

C251 0.22uF 20% 6.3V CERM 402 · C266 0.22uF 20% 6.3V CERM 402 · C249 0.22uF 20% 6.3V CERM 402

INTREPID 3.3V DECOUPLING

+3V_MAIN

57 Balls
4 X 10UF (0805)
72 X 0.22UF (0402)

C164 10uF 20% 6.3V CERM 805 · C395 10uF 20% 6.3V CERM 805 · C10 10uF 20% 6.3V CERM 805 · C9 10uF 20% 6.3V CERM 805

C375 0.22uF 20% 6.3V CERM 402 · C351 0.22uF 20% 6.3V CERM 402 · C53 0.22uF 20% 6.3V CERM 402 · C42 0.22uF 20% 6.3V CERM 402 · C21 0.22uF 20% 6.3V CERM 402 · C185 0.22uF 20% 6.3V CERM 402 · C31 0.22uF 20% 6.3V CERM 402 · C143 0.22uF 20% 6.3V CERM 402 · C123 0.22uF 20% 6.3V CERM 402 · C121 0.22uF 20% 6.3V CERM 402

C33 0.22uF 20% 6.3V CERM 402 · C184 0.22uF 20% 6.3V CERM 402 · C43 0.22uF 20% 6.3V CERM 402 · C35 0.22uF 20% 6.3V CERM 402 · C261 0.22uF 20% 6.3V CERM 402 · C60 0.22uF 20% 6.3V CERM 402 · C52 0.22uF 20% 6.3V CERM 402 · C199 0.22uF 20% 6.3V CERM 402 · C57 0.22uF 20% 6.3V CERM 402 · C19 0.22uF 20% 6.3V CERM 402

C16 0.22uF 20% 6.3V CERM 402 · C108 0.22uF 20% 6.3V CERM 402 · C55 0.22uF 20% 6.3V CERM 402 · C32 0.22uF 20% 6.3V CERM 402 · C125 0.22uF 20% 6.3V CERM 402 · C45 0.22uF 20% 6.3V CERM 402 · C76 0.22uF 20% 6.3V CERM 402 · C277 0.22uF 20% 6.3V CERM 402 · C28 0.22uF 20% 6.3V CERM 402 · C26 0.22uF 20% 6.3V CERM 402

C34 0.22uF 20% 6.3V CERM 402 · C23 0.22uF 20% 6.3V CERM 402 · C120 0.22uF 20% 6.3V CERM 402 · C146 0.22uF 20% 6.3V CERM 402 · C141 0.22uF 20% 6.3V CERM 402 · C30 0.22uF 20% 6.3V CERM 402 · C145 0.22uF 20% 6.3V CERM 402 · C96 0.22uF 20% 6.3V CERM 402 · C54 0.22uF 20% 6.3V CERM 402 · C50 0.22uF 20% 6.3V CERM 402

C75 0.22uF 20% 6.3V CERM 402 · C122 0.22uF 20% 6.3V CERM 402 · C51 0.22uF 20% 6.3V CERM 402 · C59 0.22uF 20% 6.3V CERM 402 · C163 0.22uF 20% 6.3V CERM 402 · C126 0.22uF 20% 6.3V CERM 402 · C98 0.22uF 20% 6.3V CERM 402 · C109 0.22uF 20% 6.3V CERM 402 · C56 0.22uF 20% 6.3V CERM 402 · C27 0.22uF 20% 6.3V CERM 402

C296 0.22uF 20% 6.3V CERM 402 · C248 0.22uF 20% 6.3V CERM 402 · C210 0.22uF 20% 6.3V CERM 402 · C58 0.22uF 20% 6.3V CERM 402 · C22 0.22uF 20% 6.3V CERM 402 · C20 0.22uF 20% 6.3V CERM 402 · C61 0.22uF 20% 6.3V CERM 402 · C44 0.22uF 20% 6.3V CERM 402 · C29 0.22uF 20% 6.3V CERM 402 · C24 0.22uF 20% 6.3V CERM 402

C183 0.22uF 20% 6.3V CERM 402 · C18 0.22uF 20% 6.3V CERM 402 · C49 0.22uF 20% 6.3V CERM 402 · C36 0.22uF 20% 6.3V CERM 402 · C17 0.22uF 20% 6.3V CERM 402 · C99 0.22uF 20% 6.3V CERM 402 · C396 0.22uF 20% 6.3V CERM 402 · C124 0.22uF 20% 6.3V CERM 402 · C127 0.22uF 20% 6.3V CERM 402 · C100 0.22uF 20% 6.3V CERM 402

INTREPID DDR DECOUPLING

38 15 10 9 +2_5V_INTREPID

44 Balls
4 X 10UF (0805)
51 X 0.22UF (0402)

C422 10uF 20% 6.3V CERM 805 · C417 10uF 20% 6.3V CERM 805 · C418 10uF 20% 6.3V CERM 805 · C423 10uF 20% 6.3V CERM 805

C407 0.22uF 20% 6.3V CERM 402 · C391 0.22uF 20% 6.3V CERM 402 · C310 0.22uF 20% 6.3V CERM 402 · C317 0.22uF 20% 6.3V CERM 402 · C480 0.22uF 20% 6.3V CERM 402 · C390 0.22uF 20% 6.3V CERM 402 · C370 0.22uF 20% 6.3V CERM 402 · C320 0.22uF 20% 6.3V CERM 402 · C365 0.22uF 20% 6.3V CERM 402 · C366 0.22uF 20% 6.3V CERM 402

C367 0.22uF 20% 6.3V CERM 402 · C292 0.22uF 20% 6.3V CERM 402 · C295 0.22uF 20% 6.3V CERM 402 · C403 0.22uF 20% 6.3V CERM 402 · C291 0.22uF 20% 6.3V CERM 402 · C352 0.22uF 20% 6.3V CERM 402 · C322 0.22uF 20% 6.3V CERM 402 · C392 0.22uF 20% 6.3V CERM 402 · C385 0.22uF 20% 6.3V CERM 402 · C376 0.22uF 20% 6.3V CERM 402

C321 0.22uF 20% 6.3V CERM 402 · C318 0.22uF 20% 6.3V CERM 402 · C399 0.22uF 20% 6.3V CERM 402 · C410 0.22uF 20% 6.3V CERM 402 · C335 0.22uF 20% 6.3V CERM 402 · C369 0.22uF 20% 6.3V CERM 402 · C384 0.22uF 20% 6.3V CERM 402 · C294 0.22uF 20% 6.3V CERM 402 · C406 0.22uF 20% 6.3V CERM 402 · C405 0.22uF 20% 6.3V CERM 402

C404 0.22uF 20% 6.3V CERM 402 · C400 0.22uF 20% 6.3V CERM 402 · C386 0.22uF 20% 6.3V CERM 402 · C289 0.22uF 20% 6.3V CERM 402 · C387 0.22uF 20% 6.3V CERM 402 · C401 0.22uF 20% 6.3V CERM 402 · C354 0.22uF 20% 6.3V CERM 402 · C389 0.22uF 20% 6.3V CERM 402 · C309 0.22uF 20% 6.3V CERM 402 · C398 0.22uF 20% 6.3V CERM 402

C337 0.22uF 20% 6.3V CERM 402 · C290 0.22uF 20% 6.3V CERM 402 · C402 0.22uF 20% 6.3V CERM 402 · C397 0.22uF 20% 6.3V CERM 402 · C368 0.22uF 20% 6.3V CERM 402 · C334 0.22uF 20% 6.3V CERM 402 · C388 0.22uF 20% 6.3V CERM 402 · C293 0.22uF 20% 6.3V CERM 402 · C319 0.22uF 20% 6.3V CERM 402 · C336 0.22uF 20% 6.3V CERM 402

C316 0.22uF 20% 6.3V CERM 402

Intrepid Decoupling

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SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 16 OF 44	

PCI1510 PULL-UPS

+3V_MAIN

R757 10K 5% 1/16W MF 402 — CBUS_PCI_PERR_L 17
R756 10K 5% 1/16W MF 402 — CBUS_PCI_SERR_L 17
R753 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU 17

+3V_MAIN

C813 10UF 20% 6.3V CERM 805
C795 0.22UF 20% 6.3V CERM 402
C798 0.22UF 20% 6.3V CERM 402
C790 0.22UF 20% 6.3V CERM 402
C796 0.22UF 20% 6.3V CERM 402
C797 0.22UF 20% 6.3V CERM 402
C791 0.22UF 20% 6.3V CERM 402

R762 10K 5% 1/16W MF 402

+2_5V_MAIN

C789 0.22UF 20% 6.3V CERM 402

VCC: A7, C13, D5, E1, M1, N7, N11

39 30 26 24 20 18 17 14 MAIN_RESET_L

THIS PROPERLY SHUTS DOWN
CARDBUS POWER FOR PSUEDO-D3COLD

R348 47 5% 1/16W MF 402

+3V_MAIN

NO STUFF
R373 10K 5% 1/16W MF 402

+5V_MAIN

U19
TPS2211
NC — V_12 — SSOI — AVPP
V_5_1
V_5_2 — AVCC0
V_3_1 — AVCC1
V_3_2 — AVCC2
VCCD0
VCCD1
VPPD0
VPPD1
SHTDWN
GND — OC — NC
CRITICAL

TPS2211_SHDN_L_PU

+VPP_CBUS_SW 17 38
+VCC_CBUS_SW 17 38

C773 0.1UF 20% 10V CERM 402
C467 0.1UF 20% 10V CERM 402

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES
TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

PCI1510_VR_EN_L

U26
PCI1510GGU
BGA
CRITICAL

CLAMP FOR PC-CARD
CLAMP FOR PCI

NC	H10	CLK_48_RSVD/NC
	D4	VR_EN*
	L8	VR_PORT
PCI_AD<0>	N8	AD0
PCI_AD<1>	M7	AD1
PCI_AD<2>	L7	AD2
PCI_AD<3>	N6	AD3
PCI_AD<4>	K4	AD4
PCI_AD<5>	M6	AD5
PCI_AD<6>	L6	AD6
PCI_AD<7>	N5	AD7
PCI_AD<8>	N4	AD8
PCI_AD<9>	M2	AD9
PCI_AD<10>	M5	AD10
PCI_AD<11>	L4	AD11
PCI_AD<12>	N3	AD12
PCI_AD<13>	K5	AD13
PCI_AD<14>	L5	AD14
PCI_AD<15>	M4	AD15
PCI_AD<16>	J4	AD16
PCI_AD<17>	H1	AD17
PCI_AD<18>	H3	AD18
PCI_AD<19>	H2	AD19
PCI_AD<20>	G2	AD20
PCI_AD<21>	G4	AD21
PCI_AD<22>	F1	AD22
PCI_AD<23>	C3	AD23
PCI_AD<24>	F3	AD24
PCI_AD<25>	E2	AD25
PCI_AD<26>	F4	AD26
PCI_AD<27>	B1	AD27
PCI_AD<28>	D2	AD28
PCI_AD<29>	E4	AD29
PCI_AD<30>	D3	AD30
PCI_AD<31>	E3	AD31
PCI_CBE<0>	K6	C/BE0*
PCI_CBE<1>	M3	C/BE1*
PCI_CBE<2>	J2	C/BE2*
PCI_CBE<3>	A1	C/BE3*
PCI_PAR	N1	PAR
PCI_IRDY_L	K1	IRDY
CBUS_PCI_SERR_L	L2	SERR
CBUS_PCI_IDSEL	F2	IDSEL
CBUS_PCI_PERR_L	K3	PERR
PCI_FRAME_L	J1	FRAME
PCI_STOP_L	L1	STOP
PCI_TRDY_L	J3	TRDY
PCI_DEVSEL_L	K2	DEVSEL
CBUS_PCI_RESET_L	G3	PRST
CBUS_PCI_REQ_L	C2	REQ
CBUS_PCI_GNT_L	C1	GNT
CLK33M_CBUS	G1	PCLK
NC	M9	SPKROUT
NC	M8	RI_OUT/PME
CBUS_SUSPEND_PU	N10	SUSPEND
CBUS_INT_L	K7	MFUNC0
CBUS_MFUNC1_PD	N9	MFUNC1
CBUS_MFUNC2_PD	L9	MFUNC2
CBUS_MFUNC3_PD	K10	MFUNC3
CBUS_MFUNC4_PD	M10	MFUNC4
CBUS_MFUNC5_PD	N12	MFUNC5
CBUS_MFUNC6_PD	L10	MFUNC6
	L11	GRST
	B11	VCCCB
	L3	VCCP
	N13	VCCD0*
	L12	VCCD1*
	K9	VPPD0
	M11	VPPD1
	L13	CD1*/CCD1*
	B5	CD2*/CCD2*
	F12	IORD*/CAD13
	C11	IOWR*/CAD15
	G10	OE*/CAD11
	H13	CE1*/CC/BE0*
	B2	VS1*/CVS1
	A9	VS2*/CVS2
	D13	WE*/CGNT*
	A6	RDY/IREQ*/CINT*
	D8	RESET/CRST*
	A8	REG*/CC/BE3*
	C6	BVD1/CSTSCHG/STSCHG*/RI*
	D6	BVD2/SPKR*/CAUDIO
	A5	WP/IOIS16*/CCLKRUN*
	G13	CE2/CAD10*
	B8	INPACK/CREQ*
	B6	WAIT/CSERR*
	C7	A0/CAD26
	D7	A1/CAD25
	B7	A2/CAD24
	D10	A3/CAD23
	B12	A4/CAD22
	C8	A5/CAD21
	C9	A6/CAD20
	A12	A7/CAD18
	E11	A8/CC/BE1*
	F11	A9/CAD14
	G11	A10/CAD9
	G12	A11/CAD12
	D9	A12/CC/BE2*
	E12	A13/CPAR
	D12	A14/CPERR*
	C10	A15/CIRDY*
	B13	A16/CCLK
	F10	A17/CAD16
	E13	A18/RSVD
	A13	A19/CBLOCK*
	E10	A20/CSTOP*
	D11	A21/CDEVSEL*
	C12	A22/CTRDY*
	A10	A23/CFRAME*
	B10	A24/CAD17
	B9	A25/CAD19
	A4	D0/CAD27
	C4	D1/CAD29
	A3	D2/RSVD
	K11	D3/CAD0
	K12	D4/CAD1
	J13	D5/CAD3
	J10	D6/CAD5
	H12	D7/CAD7
	C5	D8/CAD28
	B4	D9/CAD30
	B3	D10/CAD31
	M12	D11/CAD2
	J11	D12/CAD4
	K13	D13/CAD6
	J12	D14/RSVD
	H11	D15/CAD8

INTEGRATED PULL-UP

R767 22 5% 1/16W MF 402

NO STUFF
R764 47 5% 1/16W MF 402 — 30 27 26 23 IO_RESET_L

R766 47 5% 1/16W MF 402 — 39 30 26 24 20 18 17 14 MAIN_RESET_L

RP39 10K 5% 1/32W 25V SM

6	CBUS_MFUNC1_PD 17
4	CBUS_MFUNC2_PD 17
7	CBUS_MFUNC3_PD 17
3	CBUS_MFUNC4_PD 17
9	CBUS_MFUNC5_PD 17
8	CBUS_MFUNC6_PD 17
5, 10	
2	
1	

GND: A2, A11, D1, F13, H4, K8, M13, N2

R750 47 5% 1/16W MF 402 — CBUS_ADDR<16> 17

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

C783 2.2UF 20% 10V CERM 805
C776 2.2UF 20% 10V CERM 805

PC CARD/CARDBUS CONNECTOR

CRITICAL
J9
QT500806-L111
M-ST-SM1

		84	81
		2	1 CBUS_DATA<3> 17
39 17	CBUS_DET_1_L	4	3 CBUS_DATA<4> 17
17	CBUS_DATA<11>	6	5 CBUS_DATA<5> 17
17	CBUS_DATA<12>	8	7 CBUS_DATA<6> 17
17	CBUS_DATA<13>	10	9
		12	11 CBUS_DATA<7> 17
17	CBUS_DATA<14>	14	13 CBUS_CE1_L 17
17	CBUS_DATA<15>	16	15 CBUS_ADDR<10> 17
17	CBUS_CE2_L	18	17 CBUS_OE_L 17
17	CBUS_VS1	20	19
		22	21 CBUS_ADDR<11> 17
17	CBUS_IORD_L	24	23 CBUS_ADDR<9> 17
17	CBUS_IOWR_L	26	25 CBUS_ADDR<8> 17
17	CBUS_ADDR<17>	28	27 CBUS_ADDR<13> 17
17	CBUS_ADDR<18>	30	29
		32	31 CBUS_ADDR<14> 17
17	CBUS_ADDR<19>	34	33 CBUS_WE_L 17
17	CBUS_ADDR<20>	36	35 CBUS_READY 17
17	CBUS_ADDR<21>	38	37 +VCC_CBUS_SW 17 38
38 17	+VCC_CBUS_SW	40	39
		42	41 +VPP_CBUS_SW 17 38
38 17	+VPP_CBUS_SW	44	43 CBUS_ADDR<16> 17
17	CBUS_ADDR<22>	46	45 CBUS_ADDR<15> 17
17	CBUS_ADDR<23>	48	47 CBUS_ADDR<12> 17
17	CBUS_ADDR<24>	50	49
		52	51 CBUS_ADDR<7> 17
17	CBUS_ADDR<25>	54	53 CBUS_ADDR<6> 17
17	CBUS_VS2	56	55 CBUS_ADDR<5> 17
17	CBUS_RESET_L	58	57 CBUS_ADDR<4> 17
17	CBUS_WAIT_L	60	59
		62	61 CBUS_ADDR<3> 17
17	CBUS_INPACK_L	64	63 CBUS_ADDR<2> 17
17	CBUS_REG_L	66	65 CBUS_ADDR<1> 17
17	CBUS_BVD2_L	68	67 CBUS_ADDR<0> 17
17	CBUS_BVD1_L	70	69
		72	71 CBUS_DATA<0> 17
17	CBUS_DATA<8>	74	73 CBUS_DATA<1> 17
17	CBUS_DATA<9>	76	75 CBUS_DATA<2> 17
17	CBUS_DATA<10>	78	77 CBUS_WP_L 17
39 17	CBUS_DET_2_L	80	79
		83	82

CARDBUS

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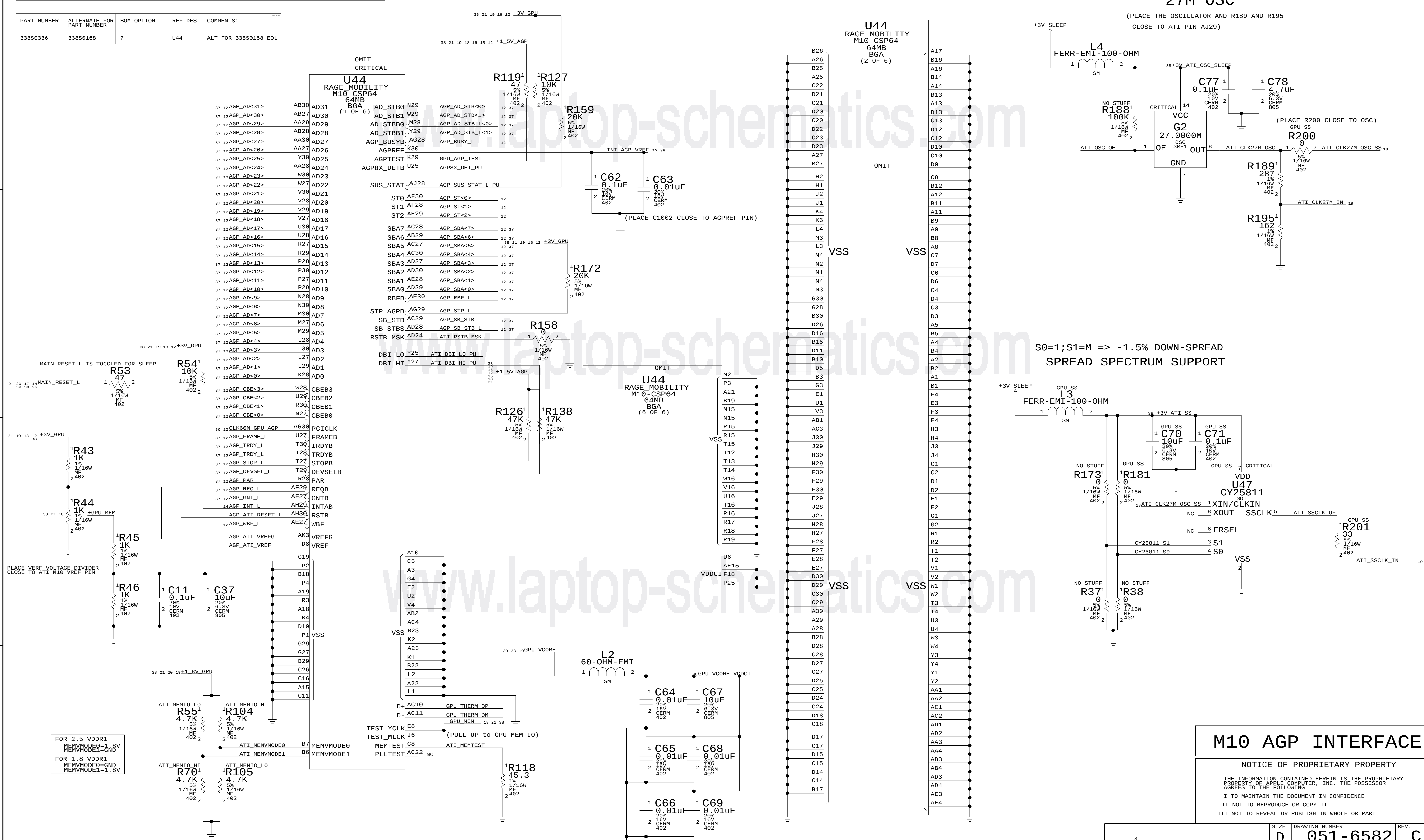
D	051-6582	C
SCALE: NONE	SHT 17 OF 44	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0168	1	IC,ATI,M10,NO HEATSPREADER	U44	CRITICAL	?

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0336	338S0168	?	U44	ALT FOR 338S0168 EOL



M10 AGP INTERFACE

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D	051-6582	C

SCALE NONE

TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

GPU VCORE - 1.2V

(PUT ALL CAPs BELOW ATI ASIC)

M10 Power Shut down Sequencing

GPU VCORE SUPPLY

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R332 / (R331//R333))

WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R332 / R333)

M10 CORE PWR/LVDS/TMDS

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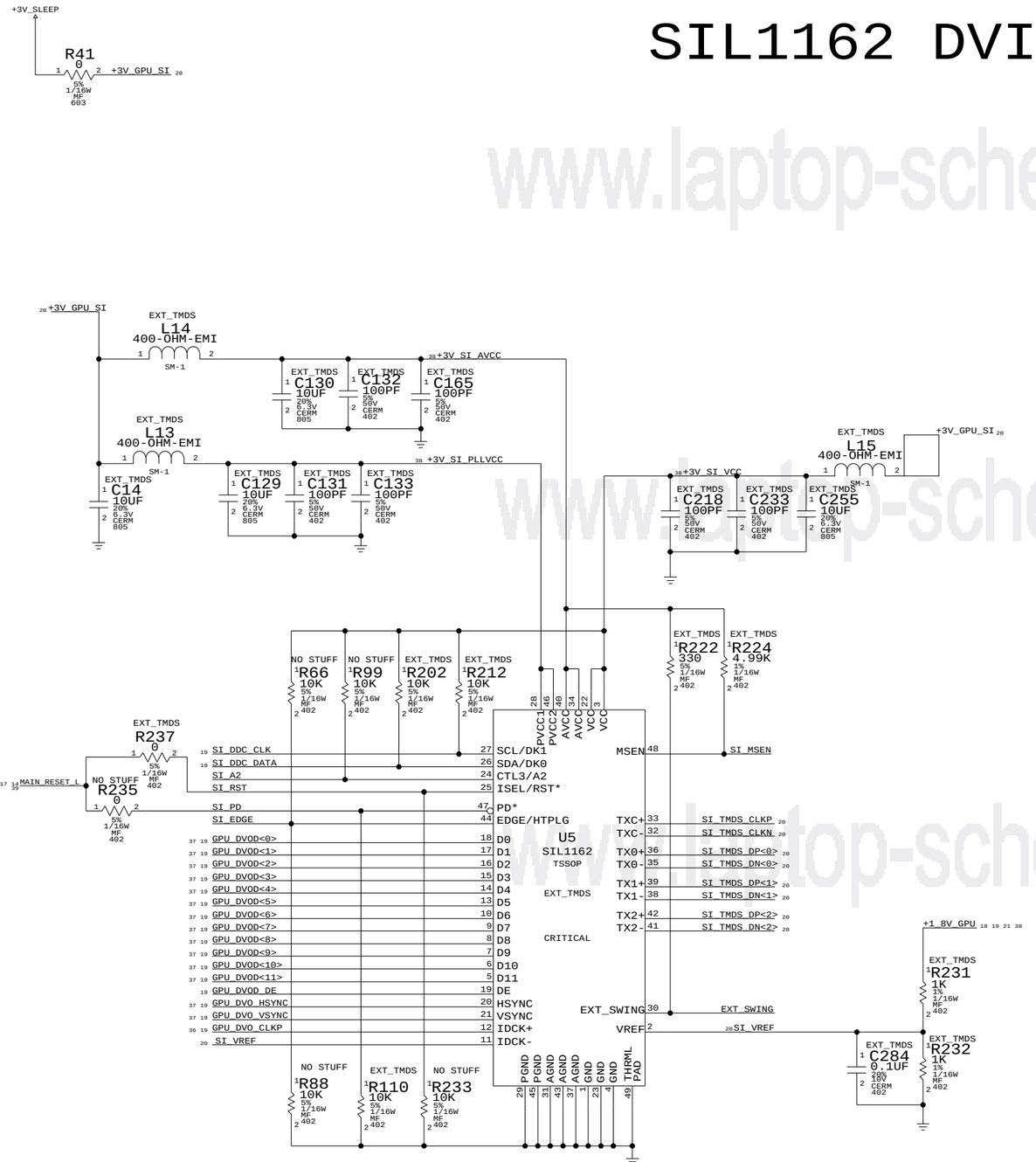
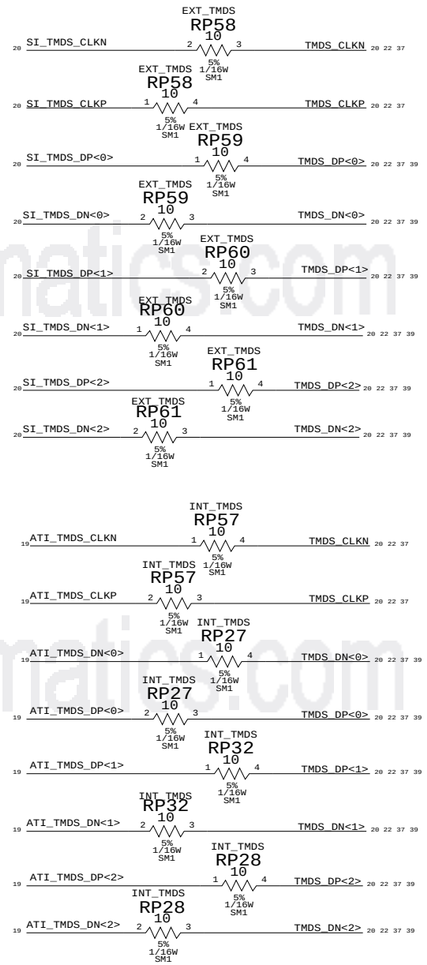
D	051-6582	C
SCALE: NONE	SHT 19 OF 44	

SIL1162 DVI TRANSMITTER





APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C

SCALE	SHT
NONE	20 OF 44

GPU PLL - 1.8V

U55 MM1571J (100mA MAX) SOT-25A CRITICAL
(Total PVDD = 66mA)
+2_5V_GPU → VIN; GPU_CORE_OK → CONT; +1_8V_ATI_PVDD ← VOUT; ATI_PVDD_BYP; GND
C889 1UF 10% 6.3V CERM 603
C379 0.01uF 20% 16V CERM 402
C380 10uF 20% 6.3V CERM 805

L65 FERR-220-OHM 0402: +1_8V_GPU_PLL
C438 10uF 20% 6.3V CERM 805
C865 0.1uF 20% 10V CERM 402
C716 0.01uF 20% 16V CERM 402 (21mA)

L58 FERR-220-OHM 0402: +2_5V_GPU → +2_5V_GPU_A2VDD (140mA)
C360 10uF 20% 6.3V CERM 805
C364 0.01uF 20% 16V CERM 402
C374 0.01uF 20% 16V CERM 402

L66 FERR-220-OHM 0402: +1_8V_GPU_AVDD (AVDD+VDDDI=75mA)
C415 10uF 20% 6.3V CERM 805
C437 0.01uF 20% 16V CERM 402
C870 0.01uF 20% 16V CERM 402

L55 FERR-220-OHM 0402: +1_8V_GPU → +1_8V_GPU_AVDDQ (2mA)
C339 10uF 20% 6.3V CERM 805
C363 0.01uF 20% 16V CERM 402

L56 FERR-220-OHM 0402: +1_8V_GPU → +1_8V_GPU_VDDDI (AVDD+VDDDI=75mA)
C358 10uF 20% 6.3V CERM 805
C361 0.01uF 20% 16V CERM 402
C372 0.01uF 20% 16V CERM 402

L57 FERR-220-OHM 0402: +GPU_MEM → +GPU_MCLK
C359 10uF 20% 6.3V CERM 805
C362 0.01uF 20% 16V CERM 402
C373 0.01uF 20% 16V CERM 402

+1_5V_SLEEP → R722 0 5% 1/10W FF 805 → +1_5V_AGP
1.5V

+1_8V_SLEEP → R284 0 5% 1/10W FF 805 → +1_8V_GPU
1.8V

+1_8V_SLEEP → R729 0 5% 1/4W FF 1210
+2_5V_SLEEP → R728 0 5% 1/4W FF 1210 → +GPU_MEM
ATI_MEMIO_LO / ATI_MEMIO_HI
1.8V 2.5V

AGP 4X I/O - 1.5V

L59 FERR-10-OHM-500MA SM: +1_5V_AGP_GPU (20mA)
C381 0.1uF 20% 10V CERM 402
C420 0.1uF 20% 10V CERM 402
C446 0.1uF 20% 10V CERM 402
C543 0.1uF 20% 10V CERM 402
C871 10uF 20% 6.3V CERM 805
C382 0.01uF 20% 16V CERM 402
C421 0.01uF 20% 16V CERM 402
C447 0.01uF 20% 16V CERM 402
C671 0.01uF 20% 16V CERM 402

MEMORY CORE - 2.5V

L63 FERR-220-OHM 0805: +GPU_MEM → +GPU_MEMCORE (1800mA)
C383 0.1uF 20% 10V CERM 402
C425 0.1uF 20% 10V CERM 402
C866 0.1uF 20% 10V CERM 402
C672 0.1uF 20% 10V CERM 402
C715 10uF 20% 6.3V CERM 805
C408 0.01uF 20% 16V CERM 402
C426 0.01uF 20% 16V CERM 402
C450 0.01uF 20% 16V CERM 402
C701 0.01uF 20% 16V CERM 402

LVDS PLL - 1.8V

L61 FERR-220-OHM 0402: +1_8V_ATI_PVDD → +1_8V_GPU_PNLPLL (40mA)
C409 10uF 20% 6.3V CERM 805
C428 0.01uF 20% 16V CERM 402
C867 0.01uF 20% 16V CERM 402
EXT_TMDS R279 0 5% 1/16W MF 603 → +1_8V_GPU_TP_PLL
C877 10uF 20% 6.3V CERM 805
C878 0.01uF 20% 16V CERM 402

MEMORY PLL - 1.8V

L62 FERR-220-OHM 0402: +1_8V_ATI_PVDD → +1_8V_GPU_MEMPLL
C411 10uF 20% 6.3V CERM 805
C429 0.01uF 20% 16V CERM 402

LVDS - 2.5V

L64 FERR-10-OHM-500MA SM: +2_5V_GPU → +2_5V_GPU_PNLTO (350mA)
C412 10uF 20% 6.3V CERM 805
C434 0.01uF 20% 16V CERM 402
C868 0.01uF 20% 16V CERM 402

+2_5V_SLEEP → R721 0 5% 1/10W FF 805 → +2_5V_GPU
2.5V

LVDS/TMDS - 1.8V

L60 FERR-220-OHM 0402: +1_8V_GPU → +1_8V_GPU_PNLTO (180mA)
C413 10uF 20% 6.3V CERM 805
C435 0.1uF 20% 10V CERM 402
C864 0.1uF 20% 10V CERM 402
C704 0.1uF 20% 10V CERM 402
C414 0.1uF 20% 10V CERM 402
C436 0.01uF 20% 16V CERM 402
C869 0.01uF 20% 16V CERM 402

+3V_SLEEP → R299 0 5% 1/10W FF 805 → +3V_GPU
3.3V

GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

U44 RAGE MOBILITY M10-CSP64 64MB BGA (4 OF 6) OMIT

AK29	PVDD
AF23	AVDD0
AF24	AVDD1
AE21	A2VDD0
AF21	A2VDD1
AJ23	A2VDDQ
AH23	VDD1DI
AF20	VDD2DI
F19	VDDRH0
N6	VDDRH1
K25	VDDP
L25	
T25	
Y28	
K27	
AA25	
K26	
L26	
M26	
N26	
P26	
R26	
T26	
U26	
V26	
Y26	
AA26	
AB26	
AC26	
E6	VDDM
E12	
E13	
E18	
E19	
E20	
E26	
F26	
E7	VDDR1
H26	
E9	
E10	
E11	
E14	
E15	
E16	
E17	
E21	
E22	
E23	
E24	
E25	
AK21	LPVDD
AK11	TPVDD
A7	MPVDD
AE16	LVDDR_18
AF16	LVDDR_18
AG16	LVDDR_25
AF17	LVDDR_25
AG12	TXVDDR0
AG13	TXVDDR1
AG14	TXVDDR2
AG15	TXVDDR3
AK30	PVSS
AF22	AVSSQ
AJ22	A2VSSQ
AE22	AVSSN0
AE23	AVSSN1
AE19	A2VSSN0
AE20	A2VSSN1
AG23	VSS1DI
AF19	VSS2DI
F20	VSSRH0
M6	VSSRH1
AJ21	LPVSS
AJ11	TPVSS
A6	MPVSS
AH16	LVSSR0
AG17	LVSSR1
AH17	LVSSR2
AF18	LVSSR3
AH12	DVOVMODE
AH13	TXVSSR1
AH14	TXVSSR2
AH15	TXVSSR3
F5	VDDR1
G5	
H5	
J5	
K5	
L5	
M5	
N5	
P5	
R5	
T5	
U5	
V5	
W5	
Y5	
AA5	
AB5	
AC5	
AD5	
G26	
K6	
R6	
Y6	
AA6	
F8	
F9	
F15	
F16	
F21	
F22	
H25	
J25	
J26	
AF6	VDDR4
AE7	
AF7	
AE8	
AF8	
AE9	VDDR3
AF9	
AF10	
AD25	
AE25	
AE26	
AF26	

MEMORY I/O

U54 INT_TMDS CRITICAL MM1571J SOT-25A
+2_5V_GPU → VIN; INT_TMDS GPU_CORE_OK → CONT; +1_8V_ATI_TPVDD ← VOUT; ATI_TPVDD_BYP; GND
C879 1UF 10% 6.3V CERM 603
C880 0.01uF 10% 16V CERM 402

L69 INT_TMDS FERR-220-OHM 0402: +1_8V_GPU_TP_PLL
C881 10UF 20% 6.3V CERM 805 INT_TMDS

L67 FERR-220-OHM 0805: +GPU_MEM
(1200mA) +GPU_MEM_IO_FLT
C872 10uF 20% 6.3V CERM 805
C875 0.1uF 20% 10V CERM 402
C850 0.1uF 20% 10V CERM 402
C855 0.1uF 20% 10V CERM 402
C860 0.1uF 20% 10V CERM 402
C873 0.1uF 20% 10V CERM 402
C876 0.1uF 20% 10V CERM 402
C851 0.1uF 20% 10V CERM 402
C856 0.1uF 20% 10V CERM 402
C861 0.1uF 20% 10V CERM 402
C874 0.1uF 20% 10V CERM 402
C847 0.1uF 20% 10V CERM 402
C852 0.1uF 20% 10V CERM 402
C857 0.1uF 20% 10V CERM 402
C862 0.01uF 20% 16V CERM 402

L16 EXT_TMDS FERR-10-OHM-500MA SM: +1_8V_GPU → +1_8V_DVO_F
C304 10uF 20% 6.3V CERM 805
C327 0.1uF 20% 10V CERM 402
C647 0.1uF 20% 10V CERM 402
INT_TMDS R268 0 5% 1/16W MF 603

L68 FERR-10-OHM-500MA SM: +3V_GPU → +3V_GPU_FLT
C722 10uF 20% 6.3V CERM 805
C848 0.1uF 20% 10V CERM 402
C853 0.1uF 20% 10V CERM 402
C858 0.1uF 20% 10V CERM 402
C863 0.1uF 20% 10V CERM 402
C725 0.1uF 20% 10V CERM 402
C849 0.1uF 20% 10V CERM 402
C854 0.1uF 20% 10V CERM 402
C859 0.1uF 20% 10V CERM 402

EXT_TMDS R255 0 5% 1/16W MF 402 → +1_8V_GPU
ATI_DVODMODE → INT_TMDS R251 0 5% 1/16W MF 402

3.3V IO SUPPLY

(Max Current varies, depends on usage)

M10 SHUT DOWN POWER SEQUENCING

+2_5V_SLEEP → OMIT XW27 SM → +2_5V_SLEEP_NECK2 → DP7 BAS16TW SOT-363 → +3V_SLEEP_NECK → OMIT XW30 SM → +3V_SLEEP
+1_8V_SLEEP → OMIT XW28 SM → +1_8V_SLEEP_NECK → DP7 BAS16TW SOT-363
+1_5V_SLEEP → OMIT XW29 SM → +1_5V_SLEEP_NECK → DP7 BAS16TW SOT-363

M10 POWER

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SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 21 OF 44	

EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

Isolation required for DVI power switch

3V LEVEL SHIFTERS

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, +5V_will be driven into DDC CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC clk. Isolation will be disabled as well.

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.

VGA VSYNC BUFFERS

TMDS FILTERING PLACE CLOSE TO CONNECTOR

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

PLACE NEAR 3, 11 & 19

PLACE NEAR C5A & C5B

LCD INTERFACE

LVDS INTERFACE

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

INVERTER INTERFACE

INVERTER EXPECTS ACTIVE HIGH SIGNAL

NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY

SHARES LOGIC WITH KB RESET SIGNALS (PG 28)

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

Place GND shorts at graphics controller

LCD POWER SWITCHES

VIDEO CONNECTORS

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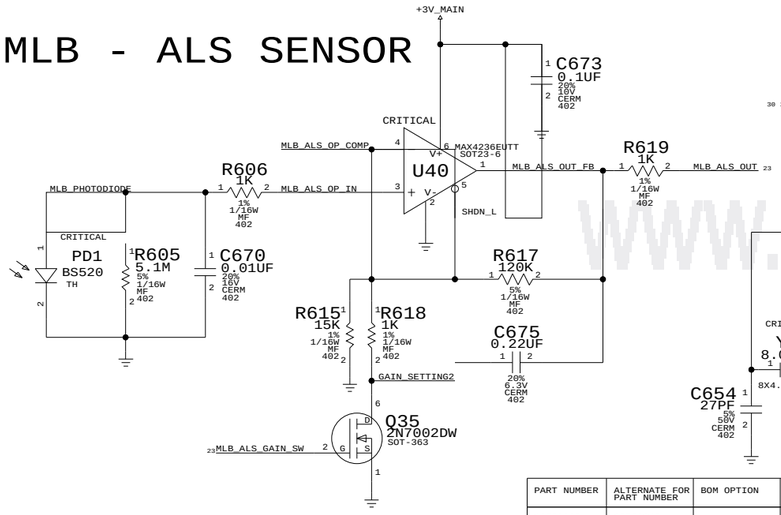
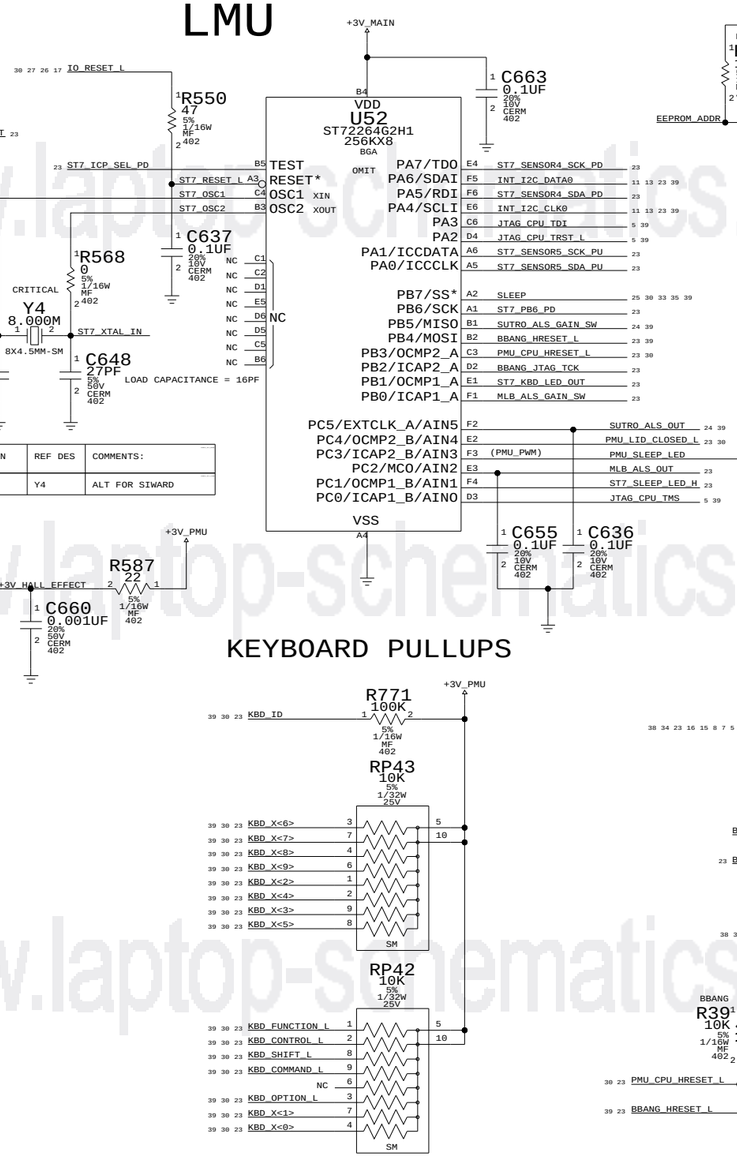
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?

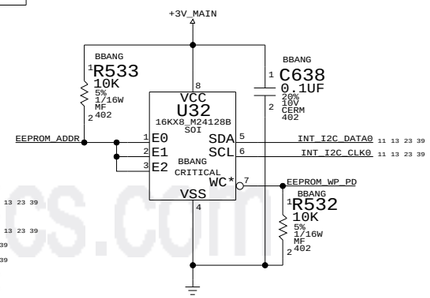
MLB - ALS SENSOR



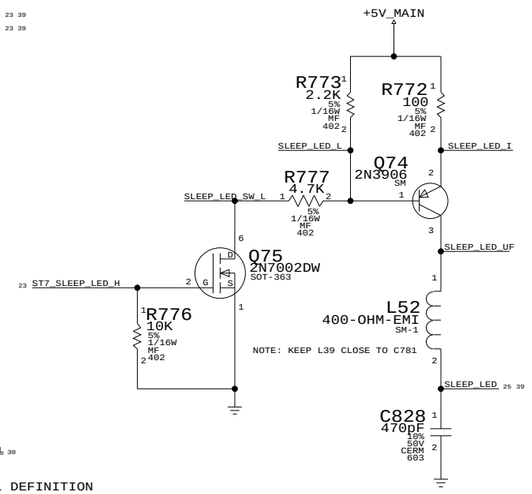
LMU



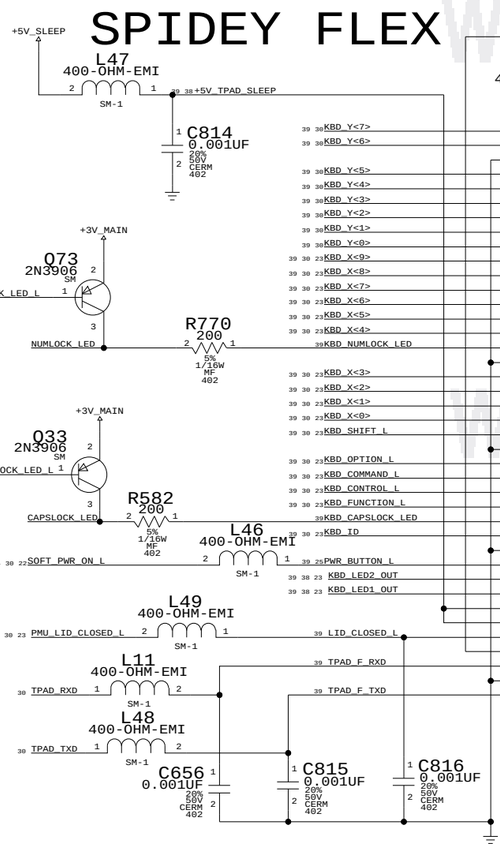
BOOT BANGER E2PROM



SLEEP LED



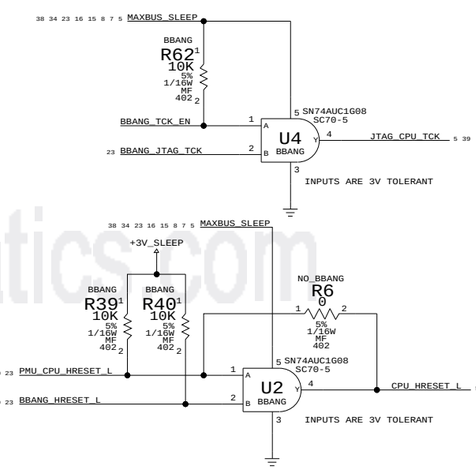
SPIDEY FLEX



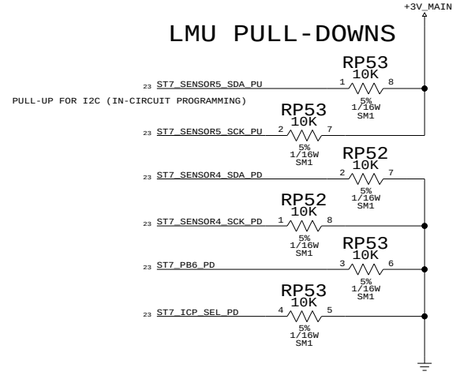
KEYBOARD PULLUPS

BOOT BANGING SIGNAL DEFINITION

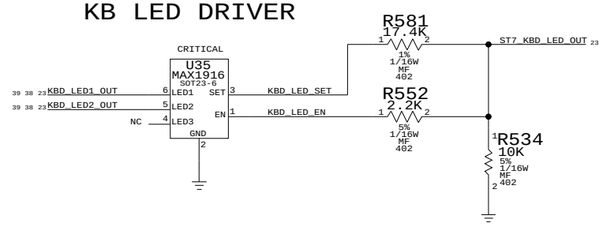
1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)



LMU PULL-DOWNS



KB LED DRIVER



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0008	197S0040		Y4	ALT FOR SIWARD

LMU/BOOTBANGER/SPIDEY

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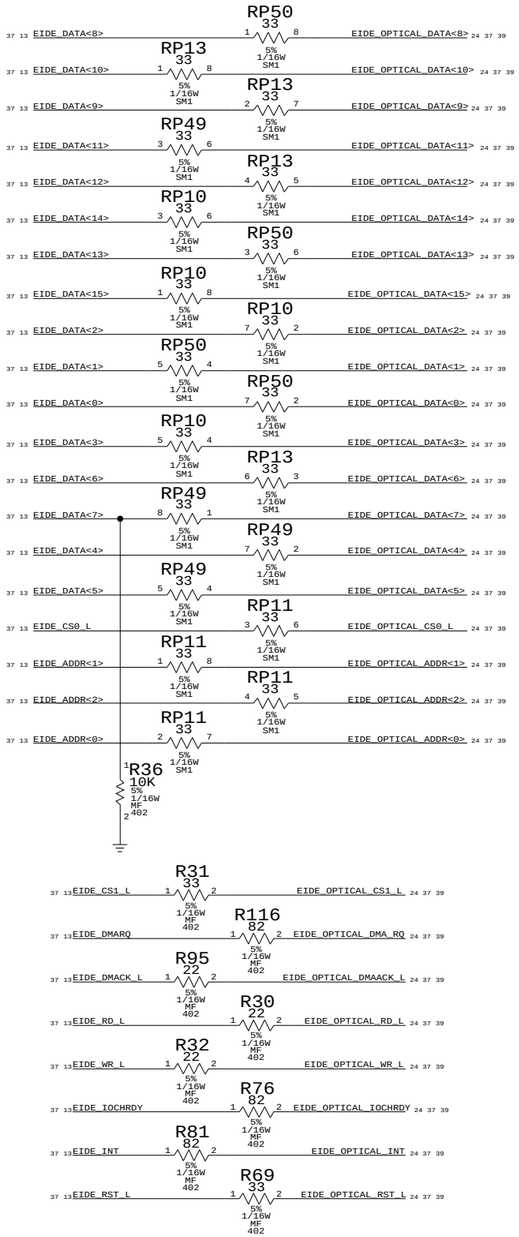
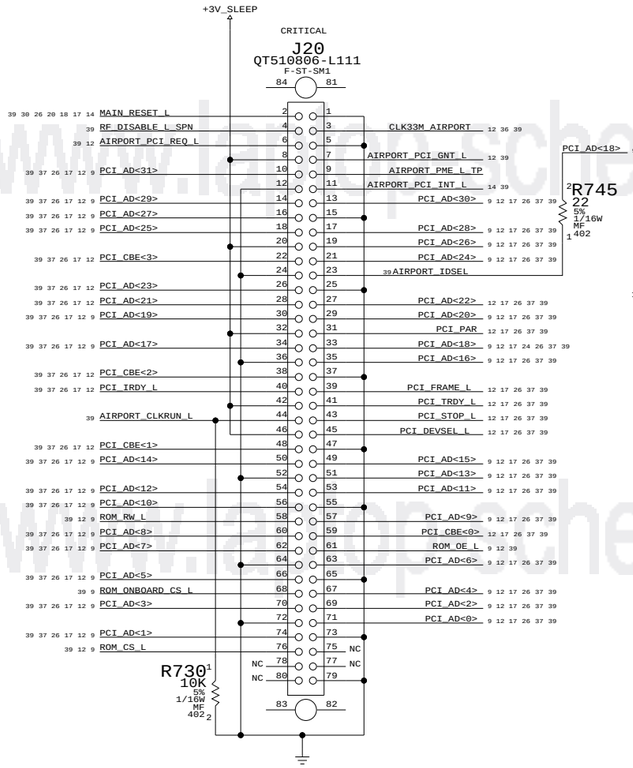
HARD DRIVE INTERFACE (UATA100)

EIDE SERIES TERMINATION

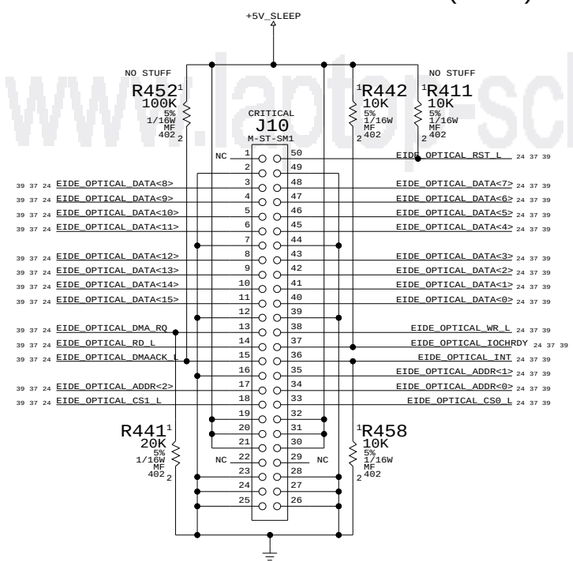
PLACE TERMINATORS NEAR INTREPID



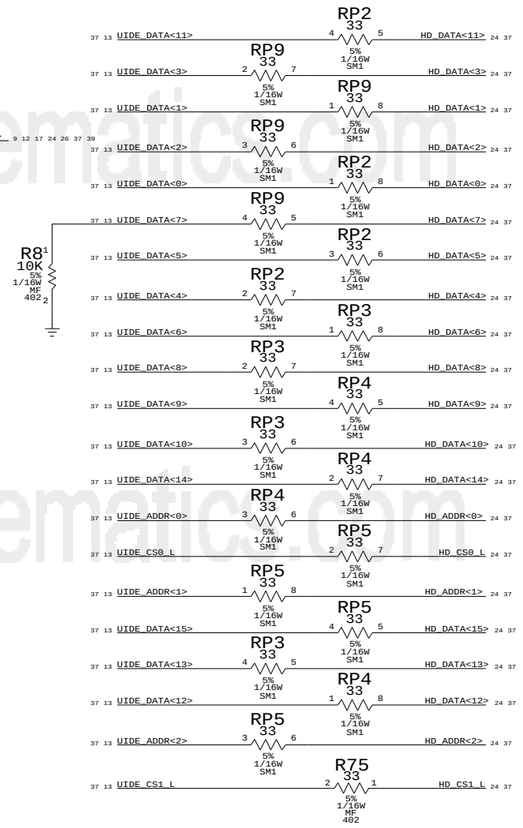
WIRELESS INTERFACE



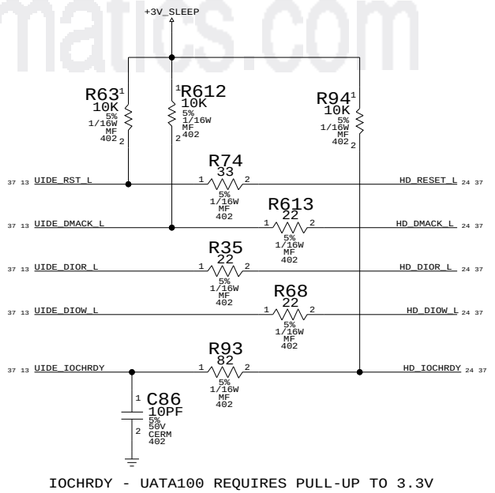
OPTICAL DRIVE INTERFACE (EIDE)



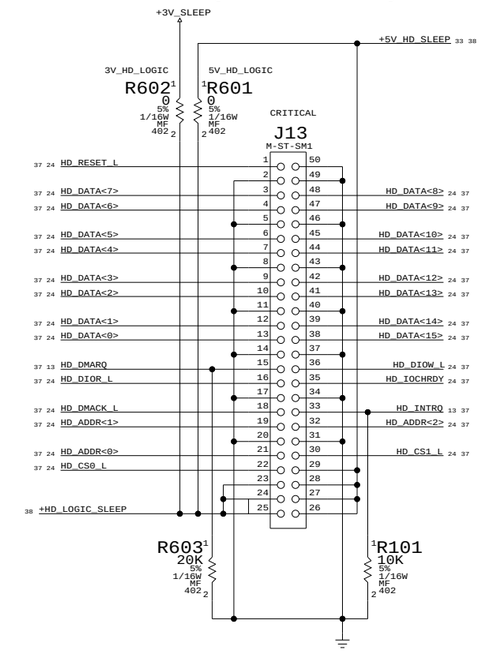
PLACE SERIES R CLOSE TO INTREPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID

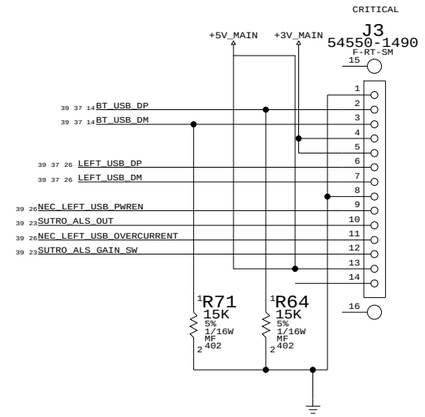


IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB



INTERNAL I/O CONNECTORS

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SOUND BOARD (SOUSAPHONE)

AUDIO - SNAPPER
SND - INTREPID

L77 FERR-220-OHM 0402 — SND_SYNC → SND_SYNC_F
C895 0.01UF 20% 16V CERM 402 NO STUFF
L80 FERR-220-OHM 0402 — SND_CLKOUT → SND_CLKOUT_F
C899 0.01UF 20% 16V CERM 402 NO STUFF
L81 FERR-220-OHM 0402 — INT_AUDIO_TO_SND → INT_AUDIO_TO_SND_F
C896 0.01UF 20% 16V CERM 402 NO STUFF
L82 FERR-220-OHM 0402 — SND_TO_AUDIO → SND_TO_AUDIO_F
C897 0.01UF 20% 16V CERM 402 NO STUFF
L76 FERR-220-OHM 0402 — SND_AMP_MUTE → SND_AMP_MUTE_F
C898 0.01UF 20% 16V CERM 402 NO STUFF
L78 FERR-220-OHM 0402 — SND_HW_RESET_L → SND_HW_RESET_L_F
C900 0.01UF 20% 16V CERM 402 NO STUFF
L79 FERR-220-OHM 0402 — SND_SCLK → SND_SCLK_F
C901 0.01UF 20% 16V CERM 402 NO STUFF

CRITICAL
J12 QT510306-L111 F-ST-SM1
INT_AUDIO_TO_SND_F → SND_TO_AUDIO_F
SND_HP_SENSE_L
INT_I2C_CLK2, SND_LIN_SENSE_L
SND_SCLK_F
SND_AMP_MUTE_F
SND_CLKOUT_F, SLEEP
SND_SYNC_F
INT_I2C_DATA2, SND_HW_RESET_L_F
SLEEP_LED
SND_HP_MUTE_INV
XW9 SM — SND_AGND

+5V_MAIN
RP44 100K 5% 1/16W SM1 — SND_AMP_MUTE
Q26 2N7002DW SOT-363 — SND_AMP_MUTE_L
AMP_CONTROL
RP44 100K 5% 1/16W SM1 — INT_PU_RESET_L
Q26 2N7002DW SOT-363

+3V_MAIN
RP44 100K 5% 1/16W SM1 — SND_HP_MUTE_INV
R689 100K 5% 1/16W MF 402
Q31 2N7002DW SOT-363 — SND_HP_MUTE
Q31 2N7002DW SOT-363 — SND_HP_MUTE_L
RP44 100K 5% 1/16W SM1 — AMP_CONTROL

PLACE XW9 CLOSE TO 5V SWITCHER (U27)
PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

CAPS FOR EMI EXPERIMENTATION ONLY

MAIN1
SUPPLY_M_DP → C681 0.001UF 20% 50V CERM 402 → Q66 2N3904 SM → SUPPLY_M_DM

PLACE CLOSE TO CPU
MAIN2
CPU_M_DP → C668 0.001UF 20% 50V CERM 402 → Q39 2N3904 SM → CPU_M_DM

PLACE UNDERNEATH UPPER RAM
ALTERNATE1
THERM1_A_DP → C678 0.001UF 20% 50V CERM 402 NO STUFF → Q47 2N3904 SM NO STUFF → THERM1_A_DM

PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2
THERM2_A_DP → C651 0.001UF 20% 50V CERM 402 NO STUFF → Q62 2N3904 SM NO STUFF → THERM2_A_DM

FAN INTERFACE

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

CPU_M_DP → R719 0 5% 1/16W MF 402 → THERM1_DP
CPU_M_DM → R725 0 5% 1/16W MF 402 → THERM1_DM
SUPPLY_M_DP → R713 0 5% 1/16W MF 402 → THERM2_DP
SUPPLY_M_DM → R716 0 5% 1/16W MF 402 → THERM2_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

THERM1_A_DP → R723 0 5% 1/16W MF 402 NO STUFF → THERM1_DP
THERM1_A_DM → R726 0 5% 1/16W MF 402 NO STUFF → THERM1_DM
THERM2_A_DP → R710 0 5% 1/16W MF 402 NO STUFF → THERM2_DP
THERM2_A_DM → R717 0 5% 1/16W MF 402 NO STUFF → THERM2_DM

FAN CONTROLLER

+3V_MAIN
R814 10 5% 1/16W MF 402
ADT7460_VCC
C904 1UF 20% 10V CERM 603
C711 0.1UF 20% 10V CERM 402

U3 ADT7460 QSOP
VCC
+2.5V/SMBALERT# — ADT7460_VCORE_MON
SDA — INT_I2C_DATA1
SCL — INT_I2C_CLK1
D1+ — THERM1_DP
D1- — THERM1_DM
D2+ — THERM2_DP
D2- — THERM2_DM
GND
PWM1/XTO — ADT7460_FAN1_PWM
TACH1 — FANL_TACH
PWM2/SMBALERT# — ADT7460_FAN2_PWM
TACH2 — FANR_TACH
PWM3/ADR ENABLE# — ADT7460_ADR_EN_L
TACH3 — NC
TACH4/ADR SELECT/THERM# — ADT7460_THERM

R42 10K 5% 1/16W MF 402
R692 10K 5% 1/16W MF 402
R695 10K 5% 1/16W MF 402
+5V_SLEEP
Q78 2N7002DW SOT-363 — FANR_PWM
Q78 2N7002DW SOT-363

C688 0.001UF 20% 50V CERM 402 NO STUFF
C690 0.001UF 20% 50V CERM 402 NO STUFF
C846 0.001UF 20% 50V CERM 402 NO STUFF
C905 0.001UF 20% 50V CERM 402 NO STUFF

THERM ISOLATION

+3V_MAIN
R811 100K 5% 1/16W MF 402
R813 100K 5% 1/16W MF 402
ADT7460_THERM
Q87 2N7002DW SOT-363
THERM_INV
C903 0.1UF 20% 10V CERM 402
+3V_PMU_AVCC
R812 100K 5% 1/16W MF 402
THERM_L_OC
Q87 2N7002DW SOT-363

LEFT FAN (CPU)

+5V_SLEEP
R679 10K 5% 1/16W MF 402
FANL_TACH
FANL_GND
Q37 SI3446DV TSOP
CRITICAL
J4 SM-2MT
PLACE CLOSE TO CONNECTOR
C134 4.7UF 20% 10V CERM 1206
FANL_PWM

MODEM

SUPPORTS BOTH THE LAST DASH AND Q52 SOFT MODEM

+5V_MAIN
C767 10UF 20% 6.3V CERM 805
C513 0.1UF 20% 10V CERM 402 NO STUFF
+3V_MAIN
R405 10K 5% 1/16W MF 402
C478 0.1UF 20% 10V CERM 402 NO STUFF
C469 10UF 20% 6.3V CERM 805

CRITICAL
J8 QT510166-L010 F-ST-SM1
MOD_DTO → MOD_SYNC
MOD_CLKOUT → INT_MOD_DTI
MOD_BITCLK
COMM_RESET_L
COMM_SHUTDOWN → MODEM_USB_DM
INT_I2C_CLK2 → MODEM_USB_DP
INT_I2C_DATA2 → COMM_RING_DET_L

SERIAL DEBUG INTERFACE

+5V_MAIN
CRITICAL
J16 M-ST-5087 SM
COMM_TXD_L
COMM_TRXC
COMM_GPIO_L
COMM_DTR_L
COMM_RTS_L
COMM_RXD

DEBUG POWER BUTTON

NO STUFF
R527 0 5% 1/16W MF 603
PWR_BUTTON_L

DEBUG JUMPERS

+5V_SLEEP
R293 10K 5% 1/16W MF 402
R295 10K 5% 1/16W MF 402
FANL_PWM
FANR_PWM

NO STUFF
R537 0 5% 1/16W MF 603
PMU_NMI_BUTTON_L

NO STUFF
R553 0 5% 1/16W MF 603
PMU_RESET_BUTTON_L

RIGHT FAN (GPU)

+5V_SLEEP
R623 10K 5% 1/16W MF 402
CRITICAL
J2 SM-2MT
FANR_GND
FANR_TACH
Q36 SI3446DV TSOP
PLACE CLOSE TO CONNECTOR
C135 4.7UF 20% 10V CERM 1206
FANR_PWM

FAN/MODEM/SOUND/SLEEP LED/DEBUG

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D	051-6582	C
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038	NEC_USB	Y5	ALT FOR SIWARD

Y7 LOAD CAPACITANCE IS 16PF

SERR_L AND PERR_L
HAS DEDICATED PULL-UP
FOR BOTH CBUS AND USB2

Series Rpaks required to
facilitate NAND-tree testing

Low/Full/High Speed (External)

Low/Full/High Speed (External)

Tie to GND at ball N11

NEED PULL-UP RESISTORS IN CASE USB 1.0 IS USED FOR PORT POWER

INTREPID USB CONSTRAINTS

PLACE NEAR J3

SUTRO CONNECTOR

PLACE NEAR J12

BUBBA CONNECTOR

USB 2.0

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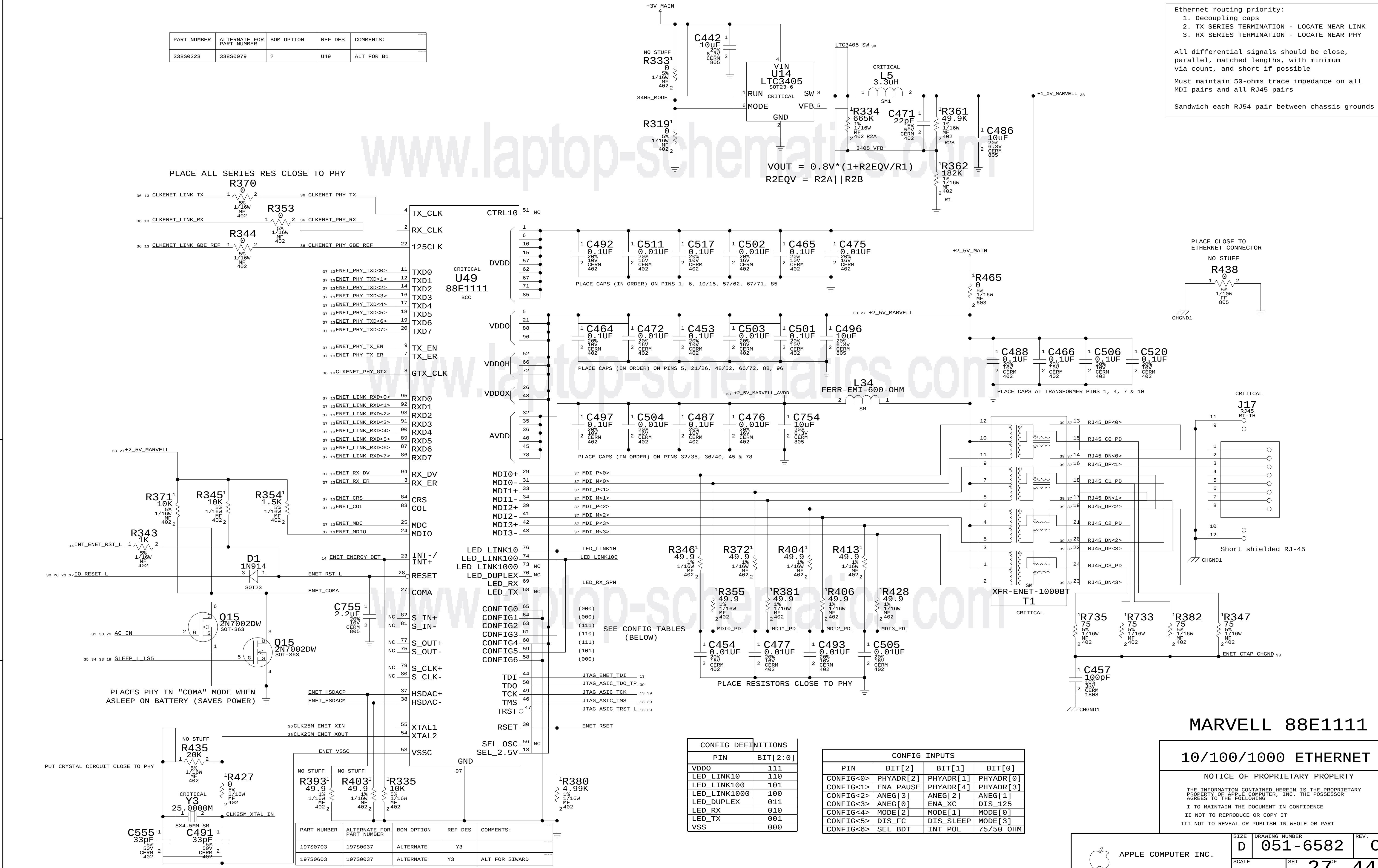
Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0223	338S0079	?	U49	ALT FOR B1



+3V_MAIN
C442 10uF
NO STUFF R333 0
U14 LTC3405 SOT23-6
VIN RUN MODE SW VFB GND
CRITICAL L5 3.3uH
R334 665K
C471 22pF
R361 49.9K
C486 10uF
R362 182K
R319 0
+1_0V_MARVELL
VOUT = 0.8V*(1+R2EQV/R1)
R2EQV = R2A||R2B
PLACE ALL SERIES RES CLOSE TO PHY
R370 0
R353 0
R344 0
CLKENET_LINK_TX
CLKENET_LINK_RX
CLKENET_LINK_GBE_REF
CLKENET_PHY_TX
CLKENET_PHY_RX
CLKENET_PHY_GBE_REF
CRITICAL U49 88E1111 BCC
TX_CLK RX_CLK 125CLK TXD0 TXD1 TXD2 TXD3 TXD4 TXD5 TXD6 TXD7 TX_EN TX_ER GTX_CLK
RXD0 RXD1 RXD2 RXD3 RXD4 RXD5 RXD6 RXD7 RX_DV RX_ER CRS COL MDC MDIO INT-/ INT+ RESET COMA
S_IN+ S_IN- S_OUT+ S_OUT- S_CLK+ S_CLK- HSDAC+ HSDAC- XTAL1 XTAL2 VSSC GND
CTRL10 DVDD VDDO VDDOH VDDOX AVDD
MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3-
LED_LINK10 LED_LINK100 LED_LINK1000 LED_DUPLEX LED_RX LED_TX
CONFIG0 CONFIG1 CONFIG2 CONFIG3 CONFIG4 CONFIG5 CONFIG6
TDI TDO TCK TMS TRST RSET SEL_OSC SEL_2.5V
SEE CONFIG TABLES (BELOW)
PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85
PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96
PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78
PLACE CAPS AT TRANSFORMER PINS 1, 4, 7 & 10
L34 FERR-EMI-600-OHM
+2_5V_MAIN
R465 0
+2_5V_MARVELL
+2_5V_MARVELL_AVDD
PLACE CLOSE TO ETHERNET CONNECTOR
NO STUFF R438 0
CRITICAL J17 RJ45 RT-TH
Short shielded RJ-45
XFR-ENET-1000BT T1 CRITICAL
RJ45_DP<0> RJ45_C0_PD RJ45_DN<0> RJ45_DP<1> RJ45_C1_PD RJ45_DN<1> RJ45_DP<2> RJ45_C2_PD RJ45_DN<2> RJ45_DP<3> RJ45_C3_PD RJ45_DN<3>
R735 75
R733 75
R382 75
R347 75
ENET_CTAP_CHGND
C457 100pF
CHGND1
R346 49.9
R372 49.9
R404 49.9
R413 49.9
R355 49.9
R381 49.9
R406 49.9
R428 49.9
C454 0.01UF
C477 0.01UF
C493 0.01UF
C505 0.01UF
PLACE RESISTORS CLOSE TO PHY
R371 10K
R345 10K
R354 1.5K
R343 1K
INT_ENET_RST_L
D1 1N914 SOT23
IO_RESET_L
ENET_RST_L
ENET_COMA
Q15 2N7002DW SOT-363
AC_IN
SLEEP_L_LS5
PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)
C755 2.2uF
ENET_HSDACP
ENET_HSDACM
CLK25M_ENET_XIN
CLK25M_ENET_XOUT
ENET_VSSC
NO STUFF R435 20K
PUT CRYSTAL CIRCUIT CLOSE TO PHY
R427 0
CRITICAL Y3 25.0000M 8X4.5MM-SM
CLK25M_XTAL_IN
C555 33pF
C491 33pF
Y3'S LOAD CAPACITANCE IS 20PF
NO STUFF R393 49.9
NO STUFF R403 49.9
R335 10K
R380 4.99K
JTAG_ENET_TDI
JTAG_ASIC_TDO_TP
JTAG_ASIC_TCK
JTAG_ASIC_TMS
JTAG_ASIC_TRST_L
ENET_RSET

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0703	197S0037	ALTERNATE	Y3	
197S0603	197S0037	ALTERNATE	Y3	ALT FOR SIWARD

CONFIG DEFINITIONS

PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS

PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

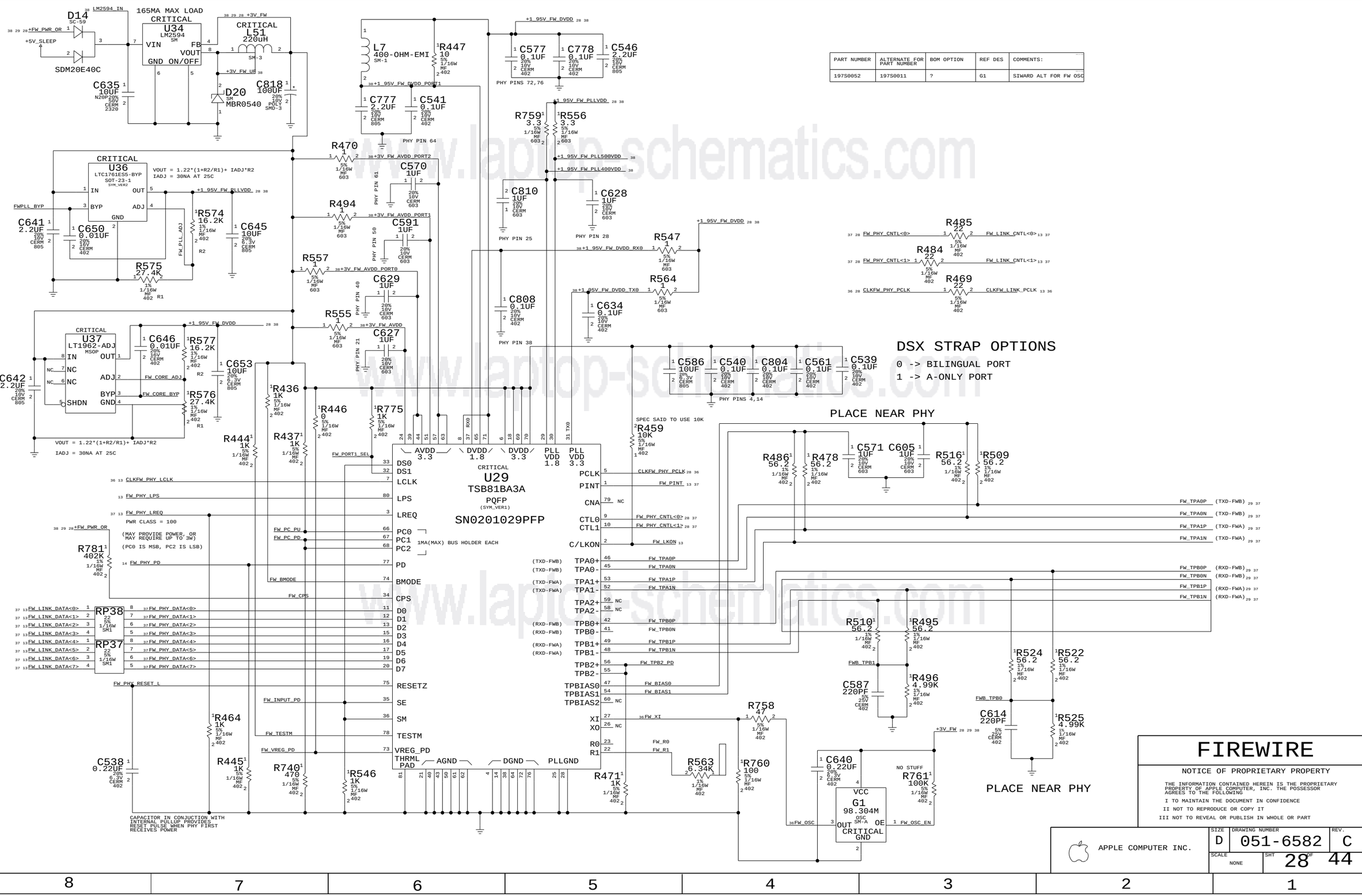
MARVELL 88E1111

10/100/1000 ETHERNET

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6582 | REV. C

SCALE NONE | SHT 27 OF 44


D14
SC-59
SDM20E40C
+FW_PWR_OR
+5V_SLEEP
LM2594_IN
165MA MAX LOAD
CRITICAL
U34
LM2594
SM
VIN
FB
VOUT
GND
ON/OFF
+3V_FW
CRITICAL
L51
220uH
SM-3
+3V_FW_UP
C635
10UF
N20P
CERM
2320
D20
SM
MBR0540
C818
100UF
POLY
SMD-3
L7
400-OHM-EMI
SM-1
R447
10
+1_95V_FW_DVDD_PORT1
PHY PINS 72,76
C577
0.1UF
C778
0.1UF
C546
2.2UF
C777
2.2UF
C541
0.1UF
PHY PIN 64
+1_95V_FW_PLLVDD
R759
3.3
R556
3.3
+1_95V_FW_PLL500VDD
+1_95V_FW_PLL400VDD
C810
1UF
C628
1UF
PHY PIN 25
PHY PIN 28
R470
1
+3V_FW_AVDD_PORT2
C570
1UF
PHY PIN 61
R494
1
+3V_FW_AVDD_PORT1
C591
1UF
PHY PIN 50
CRITICAL
U36
LTC1761ES5-BYP
SOT-23-1
SYM_VER2
VOUT = 1.22*(1+R2/R1)+ IADJ*R2
IADJ = 30NA AT 25C
IN
OUT
BYP
ADJ
GND
FWPLL_BYP
+1_95V_FW_PLLVDD
C641
2.2UF
C650
0.01UF
R574
16.2K
C645
10UF
FW_PLL_ADJ
R2
R575
27.4K
R1
R557
1
+3V_FW_AVDD_PORT0
C629
1UF
PHY PIN 40
R555
1
+3V_FW_AVDD
C627
1UF
PHY PIN 21
+1_95V_FW_DVDD
R547
1
+1_95V_FW_DVDD_RX0
R564
1
+1_95V_FW_DVDD_TX0
C808
0.1UF
C634
0.1UF
PHY PIN 38
R485
22
FW_PHY_CNTL<0>
FW_LINK_CNTL<0>
R484
22
FW_PHY_CNTL<1>
FW_LINK_CNTL<1>
R469
22
CLKFW_PHY_PCLK
CLKFW_LINK_PCLK
CRITICAL
U37
LT1962-ADJ
MSOP
IN
NC
NC
SHDN
OUT
ADJ
BYP
GND
C642
2.2UF
C646
0.01UF
R577
16.2K
C653
10UF
FW_CORE_ADJ
FW_CORE_BYP
R576
27.4K
R2
R1
VOUT = 1.22*(1+R2/R1)+ IADJ*R2
IADJ = 30NA AT 25C
C586
10UF
C540
0.1UF
C804
0.1UF
C561
0.1UF
C539
0.1UF
PHY PINS 4,14
DSX STRAP OPTIONS
0 -> BILINGUAL PORT
1 -> A-ONLY PORT
SPEC SAID TO USE 10K
R459
10K
PLACE NEAR PHY
R436
1K
R446
0
R775
1K
R444
1K
R437
1K
FW_PORT1_SEL
AVDD 3.3
DVDD 1.8
DVDD 3.3
PLL VDD 1.8
PLL VDD 3.3
CRITICAL
U29
TSB81BA3A
PQFP
(SYM_VER1)
SN0201029PFP
1MA(MAX) BUS HOLDER EACH
DS0
DS1
LCLK
LPS
LREQ
PC0
PC1
PC2
PD
BMODE
CPS
D0
D1
D2
D3
D4
D5
D6
D7
RESETZ
SE
SM
TESTM
VREG_PD
THRML PAD
AGND
DGND
PLLGND
PCLK
PINT
CNA
CTL0
CTL1
C/LKON
TPA0+
TPA0-
TPA1+
TPA1-
TPA2+
TPA2-
TPB0+
TPB0-
TPB1+
TPB1-
TPB2+
TPB2-
TPBIAS0
TPBIAS1
TPBIAS2
XI
XO
R0
R1
CLKFW_PHY_PCLK
FW_PINT
FW_PHY_CNTL<0>
FW_PHY_CNTL<1>
FW_LKON
FW_TPA0P
FW_TPA0N
FW_TPA1P
FW_TPA1N
FW_TPB0P
FW_TPB0N
FW_TPB1P
FW_TPB1N
FW_TPB2_PD
FW_BIAS0
FW_BIAS1
FW_XI
FW_R0
FW_R1
R486
56.2
R478
56.2
C571
1UF
C605
1UF
R516
56.2
R509
56.2
FW_TPA0P (TXD-FWB)
FW_TPA0N (TXD-FWB)
FW_TPA1P (TXD-FWA)
FW_TPA1N (TXD-FWA)
FW_TPB0P (RXD-FWB)
FW_TPB0N (RXD-FWB)
FW_TPB1P (RXD-FWA)
FW_TPB1N (RXD-FWA)
R510
56.2
R495
56.2
FWB_TPB1
C587
220PF
R496
4.99K
R524
56.2
R522
56.2
FWB_TPB0
C614
220PF
R525
4.99K
PLACE NEAR PHY
R758
47
R760
100
R563
6.34K
C640
0.22UF
VCC
G1
98.304M
OSC
SM-A
OUT
OE
CRITICAL
GND
FW_OSC
FW_OSC_EN
NO STUFF
R761
100K
+3V_FW
R471
1K
R740
470
R546
1K
R445
1K
R464
1K
C538
0.22UF
FW_PHY_RESET_L
FW_INPUT_PD
FW_TESTM
FW_VREG_PD
FW_BMODE
FW_CPS
FW_PC_PU
FW_PC_PD
FW_PHY_PD
FW_PHY_LREQ
FW_PHY_LPS
CLKFW_PHY_LCLK
PWR CLASS = 100
(MAY PROVIDE POWER, OR
MAY REQUIRE UP TO 3W)
(PC0 IS MSB, PC2 IS LSB)
R781
402K
RP38
22
5%
1/16W
SM1
RP37
22
5%
1/16W
SM1
FW_LINK_DATA<0>
FW_LINK_DATA<1>
FW_LINK_DATA<2>
FW_LINK_DATA<3>
FW_LINK_DATA<4>
FW_LINK_DATA<5>
FW_LINK_DATA<6>
FW_LINK_DATA<7>
FW_PHY_DATA<0>
FW_PHY_DATA<1>
FW_PHY_DATA<2>
FW_PHY_DATA<3>
FW_PHY_DATA<4>
FW_PHY_DATA<5>
FW_PHY_DATA<6>
FW_PHY_DATA<7>
CAPACITOR IN CONJUCTION WITH
INTERNAL PULLUP PROVIDES
RESET PULSE WHEN PHY FIRST
RECEIVES POWER
PART NUMBER
ALTERNATE FOR PART NUMBER
BOM OPTION
REF DES
COMMENTS:
197S0052
197S0011
?
G1
SIWARD ALT FOR FW OSC
FIREWIRE
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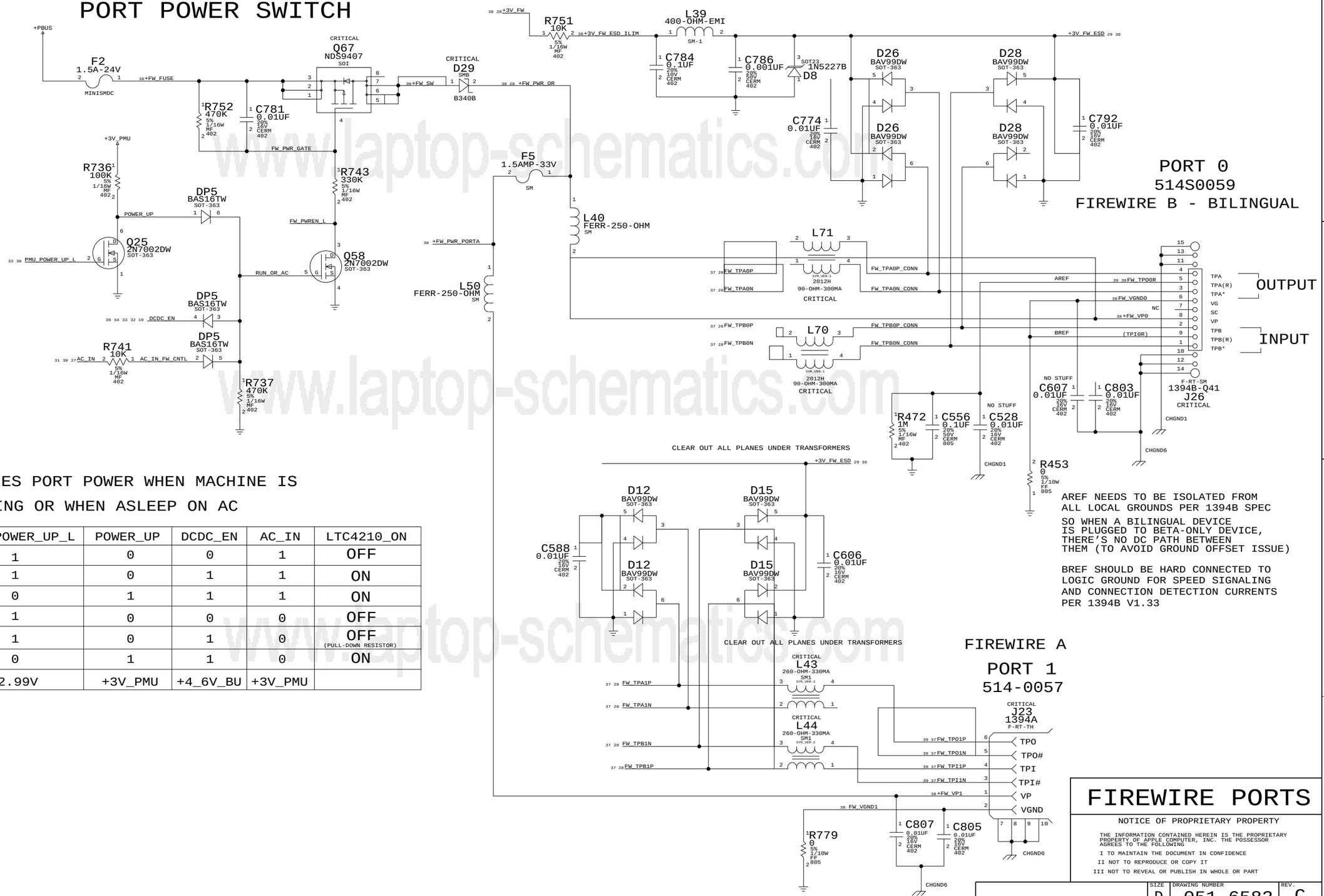
PORT POWER SWITCH



PORT 0
514S0059
FIREWIRE B - BILINGUAL

AREF NEEDS TO BE ISOLATED FROM
ALL LOCAL GROUNDS PER 1394B SPEC

SO WHEN A BILINGUAL DEVICE
IS PLUGGED TO BETA-ONLY DEVICE,
THERE'S NO DC PATH BETWEEN
THEM (TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO
LOGIC GROUND FOR SPEED SIGNALING
AND CONNECTION DETECTION CURRENTS
PER 1394B V1.33

ENABLES PORT POWER WHEN MACHINE IS
RUNNING OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	LTC4210_ON
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	

FIREWIRE PORTS

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U33	

CPU_VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. MLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.

UNDERVOLTAGE RESET CIRCUIT

PMU KEYBOARD RESET CIRCUIT

Keep crystal subcircuit close to PMU.
Y6'S LOAD CAPACITANCE IS 12PF

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0041		Y6	ALT CRYSTAL SIZE
197S0604	197S0041		Y6	ALT FOR SIWARD

Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V- 2.066V	1.65V- 2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V- 2.661V	2.31V- 2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V- 0.663V	0.33V- 0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V- 3.28V	2.97V- 3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

Keep crystal subcircuit close to PMU.
Y7'S LOAD CAPACITANCE IS 12.5PF

A29 DETECT CIRCUIT

PMU

APPLE COMPUTER INC.

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DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL

J18
87438-0833
M-RT-SM

CHARGE_LED_L
+ADAPTER
ADAPTER_DET

NO STUFF
C757 0.1UF 20% 50V CERM 805

PLACE CLOSE TO DC INPUT

R396 20K 1% 1/16W MF 402

R395 102K 1% 1/16W MF 402
R364 102K 1% 1/16W MF 402
R375 10K 1% 1/16W MF 402
R365 57.6K 1% 1/16W MF 402

C468 0.01UF 20% 16V CERM 402
R363 10K 5% 1/16W MF 402

U15 LMC7211 SM
CRITICAL

1V20_REF
AC_IN
AC_DIV
R394 1M 5% 1/16W MF 402
AC_IN_L
Q010 2N7002DW SOT-363
R383 470K 5% 1/16W MF 402

GREATER THAN 13.5V DETECT

DC INRUSH LIMITER

Q013 SI4435DY SOI
Q016 SI4435DY SOI

+ADAPTER_SW
+ADAPTER_SENSE
R414 330K 5% 1/16W MF 402
C458 0.1UF 20% 50V CERM 805
AC_ENABLE_GATE
R374 470K 5% 1/16W MF 402
AC_ENABLE_L
Q010 2N7002DW SOT-363

BCKFD_PROT_GATE
C592 0.1UF 20% 50V CERM 805
R474 47K 5% 1/16W MF 402
R499 68K 5% 1/16W MF 402
BCKFD_PROT_EN_L
Q021 2N7002DW SOT-363
AC_IN

R754 100K 1% 1/16W MF 402
D9 1N914 SOT23
C600 1UF 20% 50V CERM1 1210
R755 12.7K 1% 1/16W MF 402

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

PLACE U23 NEXT TO R460

U23 SENSE VOLTAGE DROP ACROSS R460

C572 0.01UF 20% 50V CERM 603

U23 MAX4172 TSSOP
RS+ RS- PG NC1 NC2 OUT GND
CRITICAL
MAX4172_OUT

R454 2.21K 0.1% 1/10W MF 603
C883 0.1UF 10% 50V X7R 603-1

R460 0.025 1% 1W MF 2512
R488 4.7 5% 1/16W MF 402
R498 4.7 5% 1/16W MF 402
1772_CSSP
1772_CSSN

IF A29 ADAPTER USED, ADJUST CURRENT SETTING

C578 0.47UF 10% 16V CERM 1206
C579 0.47UF 10% 16V CERM 1206

1MSEC INTEGRATION TIME

R742 1K 1% 1/16W MF 402
IAC_RC_COMP
C771 0.1UF 20% 10V CERM 402

+3V_PMU
R747 42.2K 0.1% 1/16W FF 603
C772 0.1UF 20% 10V CERM 402

U50 LMC7111 SOT23-5
CRITICAL
IAC_FB
ADAPTER_I_REG

DP4 BAS16TW SOT-363
LTC1625_ITH
R358 150 1% 1/16W MF 402
1_1625_COMP

PLACE R358 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY

R466 10K 1% 1/16W MF 402
CURRENT_THRESHOLD
R738 42.2K 0.1% 1/16W FF 603
R734 82.5K 0.1% 1/16W FF 603
A29_CURRENT_ADJ
Q020 2N7002DW SOT-363
A29_DETECT

R739 51.1K 0.1% 1/16W FF 603
IF ADAPTER IS OVER 18V, ADJUST CURRENT SETTING
R748 100K 5% 1/16W MF 402
OVER_18V_ADJ
Q020 2N7002DW SOT-363
AC_GTR_18V
C775 1UF 20% 10V CERM 603
Q065 2N7002DW SOT-363
1772_ACOK_L

BATTERY SWITCH-OVER CIRCUIT

+BATT
F4 5AMP-125V SM-2
F3 5AMP-125V SM-2
+24V_PBUS
+PBUS
+BATT_24V_FUSE
+BATT_14V_FUSE
CRITICAL
Q024 SI4435DY SOI
Q076 SUD45P03 TO-252
R490 47K 5% 1/16W MF 402
R746 47K 5% 1/16W MF 402
BATT_14V_GATE
BATT_24V_GATE
R512 10K 5% 1/16W MF 402
R744 10K 5% 1/16W MF 402
DP4 BAS16TW SOT-363
BATT_24PBUS_EN
BATT_14PBUS_EN
AC_IN_L
R489 158K 1% 1/16W MF 402
DP4 BAS16TW SOT-363
AC_IN_L_RC
C593 10UF 20% 6.3V CERM 805
Q021 2N7002DW SOT-363

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

+3V_PMU
R567 27.4K 1% 1/16W MF 402
R558 10K 1% 1/16W MF 402
R548 10K 1% 1/16W MF 402
R560 4.12K 1% 1/16W MF 402
R565 48.7K 1% 1/16W MF 402
R561 100K 5% 1/16W MF 402
BATTV_HIGH
BATTV_LOW
Q027 2N7002DW SOT-363
R580 5.23K 1% 1/16W MF 402
Q027 2N7002DW SOT-363
PMU_CHARGE_V

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

R566 1K 1% 1/16W MF 402
BATT_LOW_L
Q029 2N7002DW SOT-363
Q029 2N7002DW SOT-363
R542 1K 1% 1/16W MF 402

U31 MAX1772 QSOP
CRITICAL
REF = 4.096V
REF CLS

1772_DCIN
1772_ACIN
1772_ACOK_L
(+3V_PMU)
1772_VCTL
1772_ICTL
1772_ICHG
1772_IINP
1772_CCV
1772_CCI
1772_CCS
1772_REF
1772_GND
1772_LDO
1772_DLOV
1772_BST
1772_DHI
1772_LX
1772_DLO
(GND)
1772_CSIP
1772_CSIN
1772_CELLS

R526 1K 1% 1/16W MF 402
C622 0.01UF 20% 16V CERM 402
C616 0.01UF 20% 16V CERM 402
1772_CCV_RC
R497 1K 1% 1/16W MF 402
C621 0.1UF 20% 10V CERM 402
C630 1UF 20% 10V CERM 603
R487 10K 1% 1/16W MF 402
R473 4.12K 1% 1/16W MF 402
1772_CLS

R571 33 5% 1/8W FF 1206
D10 1N914 SOT23
1772_BST_ESR
R549 100K 5% 1/16W MF 402
C624 0.1UF 20% 25V CERM 603
R774 4.7 5% 1/16W MF 603
C608 0.1UF 20% 50V CERM 805

C652 1UF 20% 10V CERM 603
C817 0.1UF 20% 50V CERM 603
C802 0.1UF 20% 50V CERM 603
R559 100K 5% 1/16W MF 402
NO STUFF
C906 0.0022UF 10% 50V CERM 402
XW19

Q063 IRF7805 SM
Q064 IRF7811W SO-8
CRITICAL

C547 2.2UF 10% 16V CERM 1812
C562 2.2UF 10% 16V CERM 1812
C563 2.2UF 10% 16V CERM 1812
C557 2.2UF 10% 16V CERM 1812
C564 2.2UF 10% 16V CERM 1812

L42 10UH SM1
D30 MBRS140T3
R763 0.05 1% 1W MF 2512
+BATT_RSNS
+BATT_24V_FUSE
R543 1 5% 1/16W MF 603
R511 1 5% 1/16W MF 603
C619 4.7UF 20% 25V CERM 1206
C632 4.7UF 20% 25V CERM 1206
C631 4.7UF 20% 25V CERM 1206
C633 4.7UF 20% 25V CERM 1206
C617 4.7UF 20% 25V CERM 1206
C618 4.7UF 20% 25V CERM 1206
C824 33UF 20% 25V ELEC SM1

R578 100K 5% 1/16W MF 402
CHARGE_DISABLE
Q030 2N7002DW SOT-363
Q030 2N7002DW SOT-363
PMU_CHRG_BATT_0

C615 0.1UF 20% 10V CERM 402
U38 LMC7211 SM
CRITICAL
BATT_LOW
R588 100K 1% 1/16W MF 402
R579 499K 1% 1/16W MF 402
BATT_DIV
1V65_REF
R599 100K 1% 1/16W MF 402
R570 100K 1% 1/16W MF 402
C658 0.047UF 10% 16V CERM 402

R749 6.34K 1% 1/16W MF 402
A29_CLS_ADJ
Q065 2N7002DW SOT-363
A29_DETECT

BATTERY CONNECTOR

CRITICAL
J25
87438-0833
M-RT-SM

+BATT_VSNS
+BATT_POS
(BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
BATT_NEG

L9 FERR-EMI-100-OHM SM
L53 FERR-50-OHM SM
L10 FERR-EMI-100-OHM SM
PMU_SMB_CLK
L8 FERR-EMI-100-OHM SM
PMU_SMB_DATA
L12 FERR-50-OHM SM

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

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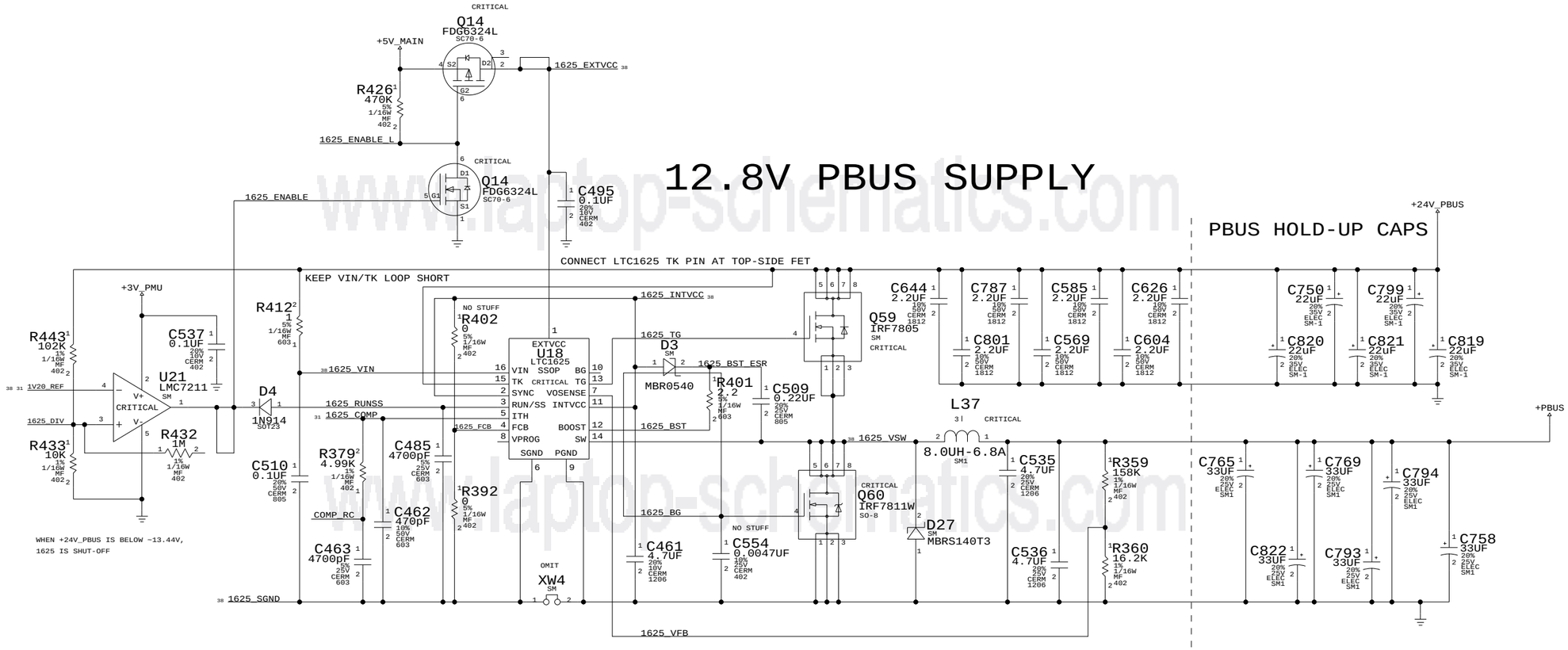
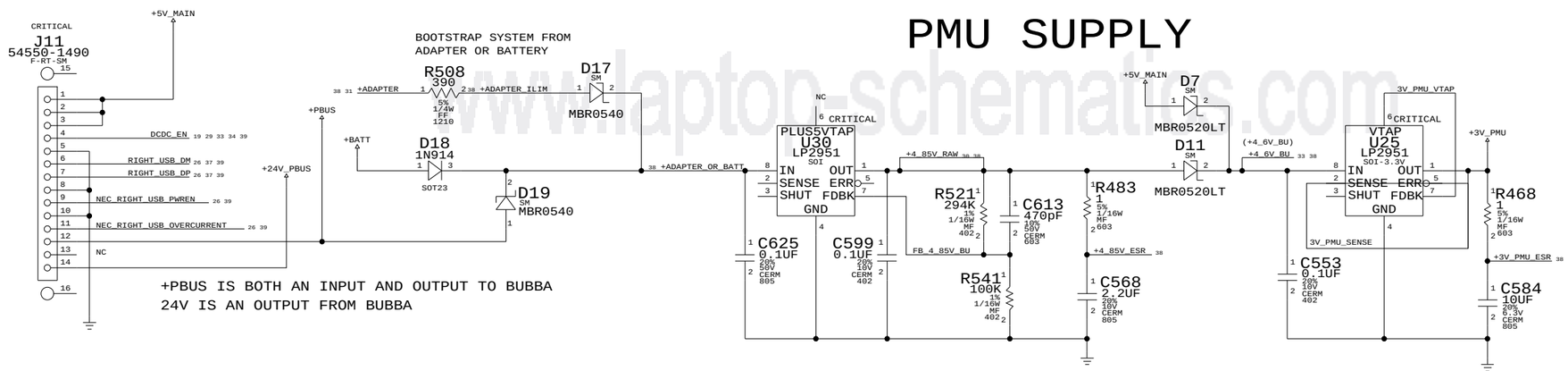
12.8V PBUS SUPPLY



PMU SUPPLY



BACKUP BATTERY / USB CONNECTOR

12.8V REGULATOR

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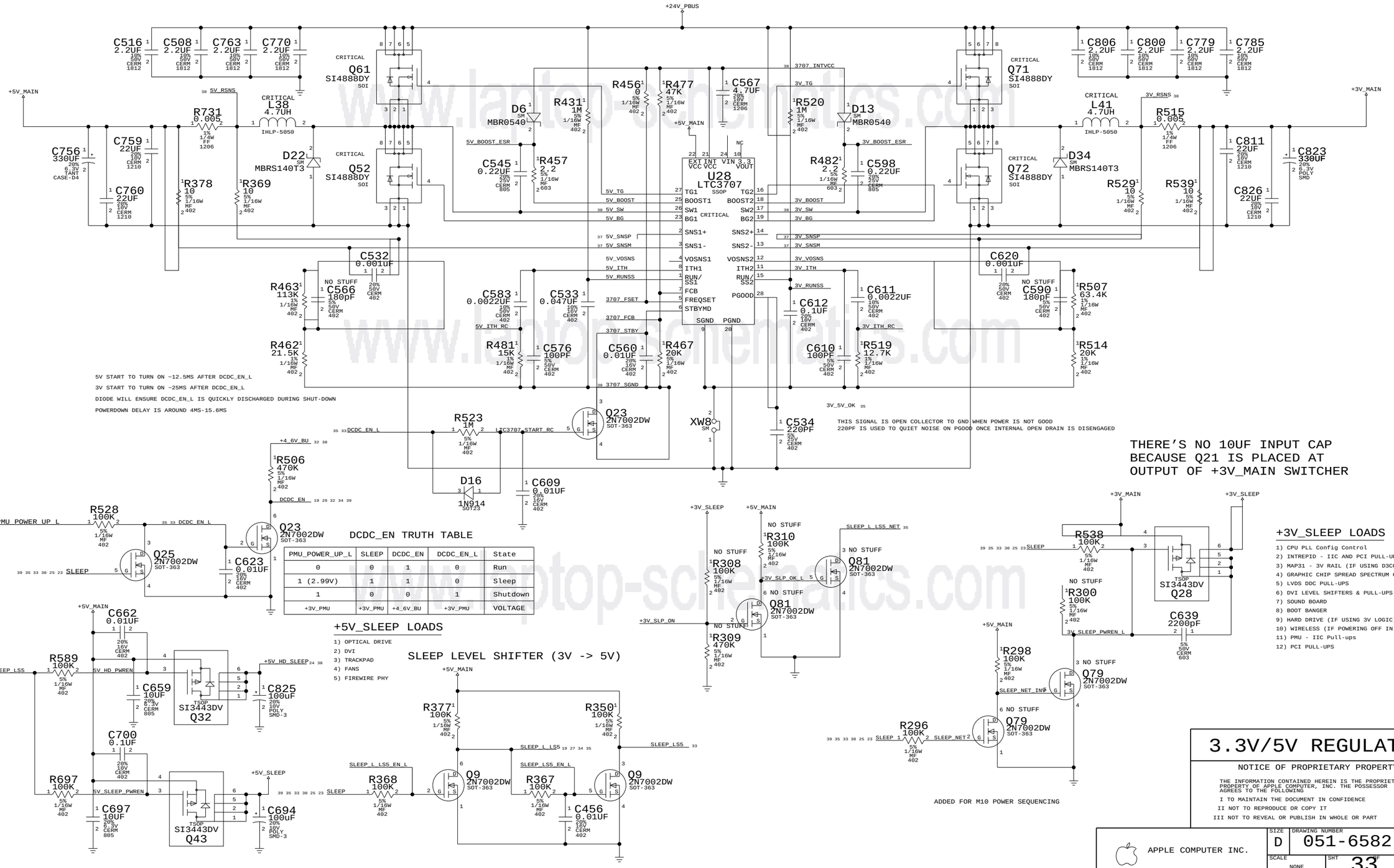
3.3V/5V MAIN SUPPLY



DCDC_EN TRUTH TABLE

PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

+5V_SLEEP LOADS

1) OPTICAL DRIVE
2) DVI
3) TRACKPAD
4) FANS
5) FIREWIRE PHY

SLEEP LEVEL SHIFTER (3V -> 5V)

+3V_SLEEP LOADS

1) CPU PLL Config Control
2) INTREPID - IIC AND PCI PULL-UPS
3) MAP31 - 3V RAIL (IF USING D3COLD)
4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
5) LVDS DDC PULL-UPS
6) DVI LEVEL SHIFTERS & PULL-UPS & HPD
7) SOUND BOARD
8) BOOT BANGER
9) HARD DRIVE (IF USING 3V LOGIC)
10) WIRELESS (IF POWERING OFF IN SLEEP)
11) PMU - IIC Pull-ups
12) PCI PULL-UPS

ADDED FOR M10 POWER SEQUENCING

3.3V/5V REGULATOR

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SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 33 OF 44	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.175V -> 1.025V 1.30V -> 1.10V

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

Connect MAX1717 GND pin 13 to GND at bottom-side FET

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

Keep trace fat and short!!

PLACE THIS SHORT AT PIN OF 1000uF CAP CLOSEST TO CPU

Keep trace fat and short!!

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, $V_A = V_B$.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S4023	1	RESISTOR	R321	?	1_30_VCORE
114S6343	1	RESISTOR	R321	?	1_32_VCORE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0022	128S0034	?	C728,C729,C730,C731,C732,C733,C734,C884,C885	

FMAX CONNECTOR

CRITICAL
NO STUFF
J5
M-ST-SM-52465-1217

VCORE_GNDDIV_TEST
VCORE_GNDSNS_TEST
+3V_PMU_RESET
SOFT_PWR_ON_L
NC (RFU)

VCORE SUPPLY

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1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE
2) AGP I/O IF USING D3HOT

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES
5) CLOCK SLEWING I/O
6) PCI1510 CORE

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD
2) INTREPID MEMORY I/O

DIODE PROVIDE PROVIDE QUICK SHUT-DOWN
POWER DOWN DELAY 1.5MS TO 3.5MS

THERE'S 100K PULL-UP ON PG 31 ALREADY

CHANGE R424 BACK TO 10K, 1%, AND STUFF 5.11K FOR 1.5V OPERATION
CONNECTING 1_5V_FB TO GND, FORCES 1.8V OUTPUT

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7450 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) OPTIONAL VIDEO MEMORY (M10 PRO ONLY)

CONTINUOUS MODE
BURST MODE

1.5V/1.8V/2.5V SUPPLIES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 35 OF 44	

DIGITAL SIGNALS

GROUP	SIG_NAME		MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
MAXBUS	CPU_AACK_L				250.0000	10 MIL SPACING		
	CPU_ADDR<0..31>		5		250			83 MHZ
	CPU_ARTRY_L				250.0000	10 MIL SPACING		
	CPU_BG_L				250.0000	10 MIL SPACING		
	CPU_BR_L				250.0000	10 MIL SPACING		
	CPU_CI_L		5		250.0000			
	CPU_DATA<0..31>		5		250			83 MHZ
	CPU_DATA<32..63>		5		250			83 MHZ
	CPU_DBG_L		5		250.0000	10 MIL SPACING		
	CPU_DTI<0..2>		5		250			
	CPU_DRDY_L_UF					10 MIL SPACING		
	CPU_DRDY_L				250.0000	10 MIL SPACING		
	CPU_GBL_L		5		250.0000			
	CPU_HIT_L				250.0000	10 MIL SPACING		
	CPU_QACK_L		5		250.0000	10 MIL SPACING		
	CPU_QREQ_L				250.0000	10 MIL SPACING		
	CPU_TA_L				250.0000	10 MIL SPACING		
	CPU_TBST_L		5		250.0000	10 MIL SPACING		
	CPU_TEA_L				250.0000			
	CPU_TS_L				250.0000	10 MIL SPACING		
	CPU_TSIZ<0..2>		5		250			
	CPU_TT<0..4>		5		250			
	CPU_WT_L		5		250.0000			
GROUP 0	MEM_DATA<7..0>		4		200			167 MHZ
	RAM_DATA_A<7..0>		4		200			167 MHZ
	RAM_DATA_B<7..0>		4		200			167 MHZ
	MEM_DQS<0>	TOTAL LENGTH CONTROLLED BY SPREADSHEET			200			
	RAM_DQS_A<0>		4		200			
	RAM_DQS_B<0>		4		200			
	MEM_DQM<0>		4		200			
	RAM_DQM_A<0>		4		200			
	RAM_DQM_B<0>		4		200			
GROUP 1	MEM_DATA<15..8>		4		200			167 MHZ
	RAM_DATA_A<15..8>		4		200			167 MHZ
	RAM_DATA_B<15..8>		4		200			167 MHZ
	MEM_DQS<1>	TOTAL LENGTH CONTROLLED BY SPREADSHEET			200			
	RAM_DQS_A<1>		4		200			
	RAM_DQS_B<1>		4		200			
	MEM_DQM<1>				200			
	RAM_DQM_A<1>		4		200			
	RAM_DQM_B<1>		4		200			
GROUP 2/3	MEM_DATA<31..16>		4		200			167 MHZ
	RAM_DATA_A<31..16>		4		200			167 MHZ
	RAM_DATA_B<31..16>		4		200			167 MHZ
	MEM_DQS<3..2>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167 MHZ
DDR RAM	RAM_DQS_A<3..2>		4		200			167 MHZ
	RAM_DQS_B<3..2>		4		200			167 MHZ
	MEM_DQM<3..2>		4		200			167 MHZ
	RAM_DQM_A<3..2>		4		200			167 MHZ
	RAM_DQM_B<3..2>		4		200			167 MHZ
GROUP 4/5	MEM_DATA<47..32>		4		200			167 MHZ
	RAM_DATA_A<47..32>		4		200			167 MHZ
	RAM_DATA_B<47..32>		4		200			167 MHZ
	MEM_DQS<5..4>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167 MHZ
	RAM_DQS_A<5..4>		4		200			167 MHZ
	RAM_DQS_B<5..4>		4		200			167 MHZ
	MEM_DQM<5..4>		4		200			167 MHZ
	RAM_DQM_A<5..4>		4		200			167 MHZ
	RAM_DQM_B<5..4>		4		200			167 MHZ
GROUP 6	MEM_DATA<55..48>		4		200			167 MHZ
	RAM_DATA_A<55..48>		4		200			167 MHZ
	RAM_DATA_B<55..48>		4		200			167 MHZ
	MEM_DQS<6>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			
	RAM_DQS_A<6>				200			
	RAM_DQS_B<6>		4		200			
	MEM_DQM<6>				200			
	RAM_DQM_A<6>		4		200			
	RAM_DQM_B<6>		4		200			
GROUP 7	MEM_DATA<63..56>		4		200			167 MHZ
	RAM_DATA_A<63..56>		4		200			167 MHZ
	RAM_DATA_B<63..56>		4		200			167 MHZ
	MEM_DQS<7>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			
	RAM_DQS_A<7>				200			
	RAM_DQS_B<7>				200			
	MEM_DQM<7>		4		200			
	RAM_DQM_A<7>		4		200			
	RAM_DQM_B<7>		4		200			
ADDR	MEM_ADDR<12..0>		4					83 MHZ
	RAM_ADDR<12..0>		6		200			
CONTROL	MEM_BA<1..0>		4					
	RAM_BA<1..0>		6		200			
	MEM_CS_L<3..0>		4					
	RAM_CS_L<3..0>		6		200			
	MEM_CKE<3..0>		4					
	RAM_CKE<3..0>		6		200			
	MEM_RAS_L		4					
	RAM_RAS_L				200.0000			
	MEM_CAS_L		4					
	RAM_CAS_L				200.0000			
	MEM_WE_L		4					
	RAM_WE_L				200.0000			
	MEM_MUXSEL_H<1..0>		3					
	MEM_MUXSEL_L<1..0>		3					
	RAM_MUXSEL_H		5					
	RAM_MUXSEL_L		5					

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME			MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM
INTREPID CLOCKS	SYSCLK_CPU_UF						10 MIL SPACING	
	SYSCLK_CPU			4		200.0000	10 MIL SPACING	
	INT_CPUFB_OUT			3			10 MIL SPACING	
	INT_CPUFB_OUT_SHORT			3			10 MIL SPACING	
	INT_CPUFB_OUT_NORM			3			10 MIL SPACING	
	INT_CPUFB_IN_NORM			3			10 MIL SPACING	
	INT_CPUFB_LONG			3			10 MIL SPACING	
	INT_CPUFB_IN					200.0000	10 MIL SPACING	
	SYSCLK_DDRCLK_A0_UF			3		200.0000	10 MIL SPACING	
	SYSCLK_DDRCLK_A0_L_UF			3		200.0000	10 MIL SPACING	
	SYSCLK_DDRCLK_A1_UF			3		200.0000	10 MIL SPACING	
	SYSCLK_DDRCLK_A1_L_UF			3		200.0000	10 MIL SPACING	
	SYSCLK_DDRCLK_B0_UF			3		200.0000	10 MIL SPACING	
	SYSCLK_DDRCLK_B0_L_UF			3		200.0000	10 MIL SPACING	
	SYSCLK_DDRCLK_B1_UF			3		200.0000	10 MIL SPACING	
	SYSCLK_DDRCLK_B1_L_UF			3		200.0000	10 MIL SPACING	
	SYSCLK_DDRCLK_A0	DDRCLK_A0		3		200.0000	10 MIL SPACING	
	SYSCLK_DDRCLK_A0_L	DDRCLK_A0				200.0000	10 MIL SPACING	
	SYSCLK_DDRCLK_A1	DDRCLK_A1		3		200.0000	10 MIL SPACING	
	SYSCLK_DDRCLK_A1_L	DDRCLK_A1				200.0000	10 MIL SPACING	
	SYSCLK_DDRCLK_B0	DDRCLK_B0		3		200.0000	10 MIL SPACING	
	SYSCLK_DDRCLK_B0_L	DDRCLK_B0		3		200.0000	10 MIL SPACING	
	SYSCLK_DDRCLK_B1	DDRCLK_B1		3		200.0000	10 MIL SPACING	
	SYSCLK_DDRCLK_B1_L	DDRCLK_B1		3		200.0000	10 MIL SPACING	
	INT_REF_CLK_OUT			3		200.0000	10 MIL SPACING	
	INT_REF_CLK_IN					200.0000	10 MIL SPACING	
	CLK66M_GPU_AGP_UF					200.0000	10 MIL SPACING	
	CLK66M_GPU_AGP			4		200.0000	10 MIL SPACING	
	INT_AGP_FB_OUT					200.0000	10 MIL SPACING	
	INT_AGP_FB_IN			4		200.0000	10 MIL SPACING	
	CLK33M_CBUS_UF					200.0000	10 MIL SPACING	
	CLK33M_CBUS	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10 MIL SPACING	
	CLK33M_AIRPORT_UF					200.0000	10 MIL SPACING	
	CLK33M_AIRPORT	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10 MIL SPACING	
	CLK33M_USB2_UF					200.0000	10 MIL SPACING	
	CLK33M_USB2	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10 MIL SPACING	
	INT_PCI_FB_OUT					200.0000	10 MIL SPACING	
	INT_PCI_FB_IN			3		200.0000	10 MIL SPACING	
MAP31	GPU_CLK27M_OUT						10 MIL SPACING	
	GPU_CLK27M_UF						10 MIL SPACING	
	GPU_SSCLK_UF						10 MIL SPACING	
	GPU_SSCLK_IN						10 MIL SPACING	
	GPU_FBCLK0						10 MIL SPACING	
	GPU_FBCLK0_L						10 MIL SPACING	
	GPU_FBCLK1						10 MIL SPACING	
	GPU_FBCLK1_L						10 MIL SPACING	
	GPU_DVO_CLKP						10 MIL SPACING	
CRYSTALS	CLK27M_GPU_XOUT						10 MIL SPACING	
	CLK27M_XTAL_IN						10 MIL SPACING	
	CLK27M_GPU_XIN						10 MIL SPACING	
	CLK18M_INT_XIN						10 MIL SPACING	
	CLK18M_INT_XOUT						10 MIL SPACING	
	CLK18M_XTAL_IN						10 MIL SPACING	
	CLK18M_INT_EXT						10 MIL SPACING	
	CLK25M_ENET_XIN						10 MIL SPACING	
	CLK25M_ENET_XOUT						10 MIL SPACING	
	NEC_XT1						10 MIL SPACING	
	NEC_XT2	THERE'S ANOTHER 280MIL LEG					10 MIL SPACING	
SOUND	SND_SCLK			7		200.0000	10 MIL SPACING	
	SND_CLKOUT					200.0000	10 MIL SPACING	
ETHERNET MARVELL	CLKENET_PHY_RX					200.0000		
	CLKENET_LINK_RX			3		200.0000	10 MIL SPACING	
	CLKENET_PHY_GBE_REF					200.0000		
	CLKENET_LINK_GBE_REF			3		200.0000	10 MIL SPACING	
	CLKENET_PHY_TX					200.0000		
	CLKENET_LINK_TX			5		200.0000	10 MIL SPACING	
	CLKENET_LINK_GTX					200.0000		
	CLKENET_PHY_GTX			3		200.0000	10 MIL SPACING	
FIREWIRE	CLKFW_PHY_PCLK					200.0000		
	CLKFW_LINK_PCLK			3		200.0000	10 MIL SPACING	
	CLKFW_PHY_LCLK			3		200.0000	10 MIL SPACING	
	CLKFW_LINK_LCLK					200.0000		
	FW_XI					200.0000	10 MIL SPACING	
	FW_OSC					200.0000	10 MIL SPACING	

SIGNAL CONSTRAINTS - PAGE 1

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Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>		5	100				66 MHz	12 18
AGP BYTES 0-1	AGP_CBE<1..0>		5	100				66 MHz	12 18
	AGP_AD_STB<0>		4	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<0>		4	100		8 MIL SPACING			12 18
AGP BYTES 2-3	AGP_AD<31..16>		5	100				66 MHz	12 18
	AGP_CBE<3..2>		5	100				66 MHz	12 18
	AGP_AD_STB<1>		4	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<1>			100		8 MIL SPACING			12 18
AGP SIDEBAND	AGP_SBA<7..0>		5	100				66 MHz	12 18
	AGP_SB_STB			100.0000		8 MIL SPACING			12 18
	AGP_SB_STB_L		4	100.0000		8 MIL SPACING			12 18
AGP CONTROL	AGP_FRAME_L			250.0000					12 18
	AGP_IRDY_L			250.0000					12 18
	AGP_TRDY_L		6	250.0000					12 18
	AGP_DEVSEL_L			250.0000					12 18
	AGP_STOP_L		6	250.0000					12 18
	AGP_PAR		6	250.0000					12 18
	AGP_REQ_L			285.0000					12 18
	AGP_GNT_L			250.0000					12 18
	AGP_RBF_L			250.0000					12 18
DVO	GPU_DVOD<0..11>		5	250					19 20
	GPU_DVO_HSYNC								19 20
	GPU_DVO_VSYNC								19 20
PCI	PCI_AD<31..0>					MIN_DAISY_CHAIN		33 MHz	9 12 17 24 26 39
	PCI_CBE<3..0>					MIN_DAISY_CHAIN		33 MHz	12 17 24 26 39
	PCI_FRAME_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_IRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_TRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_DEVSEL_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_STOP_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_PAR					MIN_DAISY_CHAIN			12 17 24 26 39
ULTRA ATA-100	UIDE_DATA<15..8>			NEED TO MATCH DELAY TO 250	200			100 MHz	13 24
	UIDE_DATA<7>				200				13 24
	UIDE_DATA<6..0>				200			100 MHz	13 24
	UIDE_ADDR<2..0>				200			100 MHz	13 24
	UIDE_RST_L				200.0000				13 24
	UIDE_DIOW_L				200.0000				13 24
	UIDE_DIOR_L			10 MIL SPACING	200.0000				13 24
	UIDE_DMACK_L				200.0000				13 24
	UIDE_CS0_L				200.0000				13 24
	UIDE_CS1_L				200.0000				13 24
	UIDE_DMARQ				200.0000				13
	UIDE_IOCHRDY			10 MIL SPACING	200.0000				13 24
	UIDE_INTRQ				200.0000				13
	HD_DATA<15..0>		5	TOTAL UIDE+HD SKEW <500MIL	200			100 MHz	24
	HD_ADDR<2..0>		5		200			100 MHz	24
	HD_RESET_L		5		200.0000				24
	HD_DIOW_L		5		200.0000				24
	HD_DIOR_L		5	10 MIL SPACING	200.0000				24
	HD_DMACK_L		5		200.0000				24
	HD_CS0_L		5		200.0000				24
	HD_CS1_L		5		200.0000				24
	HD_DMARQ				200.0000				13 24
	HD_IOCHRDY		5	10 MIL SPACING	200.0000				24
	HD_INTRQ		5						13 24
EIDE INTREPID	EIDE_DATA<15..0>							33 MHZ	13 24
	EIDE_ADDR<2..0>							33 MHZ	13 24
	EIDE_CS0_L								13 24
	EIDE_CS1_L								13 24
	EIDE_RD_L								13 24
	EIDE_WR_L								13 24
	EIDE_IOCHRDY								13 24
	EIDE_INT								13 24
	EIDE_RST_L								13 24
	EIDE_DMACK_L								13 24
	EIDE_DMARQ								13 24
OPTICAL	EIDE_OPTICAL_DATA<15..0>							33 MHZ	24 39
	EIDE_OPTICAL_ADDR<2..0>							33 MHZ	24 39
	EIDE_OPTICAL_CS0_L								24 39
	EIDE_OPTICAL_CS1_L								24 39
	EIDE_OPTICAL_RD_L								24 39
	EIDE_OPTICAL_WR_L								24 39
	EIDE_OPTICAL_IOCHRDY								24 39
	EIDE_OPTICAL_INT								24 39
	EIDE_OPTICAL_RST_L								24 39
	EIDE_OPTICAL_DMAACK_L								24 39
	EIDE_OPTICAL_DMA_RQ								24 39
ETHERNET MII	ENET_LINK_RXD<7..0>		5						13 27
	ENET_RX_DV								13 27
	ENET_RX_ER								13 27
	ENET_PHY_TXD<7..0>		5						13 27
	ENET_LINK_TXD<7..0>								13
	ENET_PHY_TX_ER		5						13 27
	ENET_LINK_TX_ER								13
	ENET_PHY_TX_EN		5						13 27
	ENET_LINK_TX_EN								13
	ENET_MDIO								13 27
	ENET_MDC								13 27
	ENET_COL								13 27
	ENET_CRS								13 27
FIREWIRE MII	FW_LINK_DATA<7..0>		5						13 28
	FW_PHY_DATA<7..0>		5						28
	FW_LINK_CNTL<1..0>								13 28
	FW_PHY_CNTL<1..0>								28
	FW_LINK_LREQ								13
	FW_PHY_LREQ								13 28
	FW_PINT								13 28

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR		MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0		SPACING DELETED BECAUSE OF PHYSICAL CONSTRAINTS AROUND MARVELL PHY			27
	MDI_P<0>	ENET_MDI0					27
	MDI_M<1>	ENET_MDI1					27
	MDI_P<1>	ENET_MDI1					27
	MDI_M<2>	ENET_MDI2					27
	MDI_P<2>	ENET_MDI2					27
	MDI_M<3>	ENET_MDI3					27
	MDI_P<3>	ENET_MDI3					27
	RJ45_DN<0>	RJ45_DP0			10 MIL SPACING		27 39
	RJ45_DP<0>	RJ45_DP0			10 MIL SPACING		27 39
	RJ45_DN<1>	RJ45_DP1			10 MIL SPACING		27 39
	RJ45_DP<1>	RJ45_DP1			10 MIL SPACING		27 39
	RJ45_DN<2>	RJ45_DP2			10 MIL SPACING		27 39
	RJ45_DP<2>	RJ45_DP2			10 MIL SPACING		27 39
	RJ45_DN<3>	RJ45_DP3			10 MIL SPACING		27 39
	RJ45_DP<3>	RJ45_DP3			10 MIL SPACING		27 39
FIREWIRE	FW_TPA0N	FW_TPA0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA0P	FW_TPA0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0N	FW_TPB0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0P	FW_TPB0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI0N	FW_TPI0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPI0P	FW_TPI0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0N	FW_TPO0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0P	FW_TPO0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPA1N	FW_TPA1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA1P	FW_TPA1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1N	FW_TPB1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1P	FW_TPB1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI1N	FW_TPI1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPI1P	FW_TPI1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1N	FW_TPO1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1P	FW_TPO1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L			10 MIL SPACING	4	19 22 39
	CLKLVDS_LP	CLKLVDS_L			10 MIL SPACING	4	19 22 39
	LVDS_L0N	LVDS_L0			10 MIL SPACING		19 22 39
	LVDS_L0P	LVDS_L0			10 MIL SPACING		19 22 39
	LVDS_L1N	LVDS_L1			10 MIL SPACING		19 22 39
	LVDS_L1P	LVDS_L1			10 MIL SPACING		19 22 39
	LVDS_L2N	LVDS_L2			10 MIL SPACING		19 22 39
	LVDS_L2P	LVDS_L2			10 MIL SPACING		19 22 39
UPPER	CLKLVDS_UN	CLKLVDS_U			10 MIL SPACING	4	19 22 39
	CLKLVDS_UP	CLKLVDS_U			10 MIL SPACING	4	19 22 39
	LVDS_U0N	LVDS_U0			10 MIL SPACING		19 22 39
	LVDS_U0P	LVDS_U0			10 MIL SPACING		19 22 39
	LVDS_U1N	LVDS_U1			10 MIL SPACING		19 22 39
	LVDS_U1P	LVDS_U1			10 MIL SPACING		19 22 39
	LVDS_U2N	LVDS_U2			10 MIL SPACING		19 22 39
	LVDS_U2P	LVDS_U2			10 MIL SPACING		19 22 39
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS			10 MIL SPACING	4	22 39
	TMDS_CONN_CLKP	CLKCONN_TMDS			10 MIL SPACING	4	22 39
	TMDS_CLKN	CLKTMDS			10 MIL SPACING	4	20 22
	TMDS_CLKP	CLKTMDS			10 MIL SPACING	4	20 22
	TMDS_DN<0>	TMDS_D0			10 MIL SPACING		20 22 39
	TMDS_DP<0>	TMDS_D0			10 MIL SPACING		20 22 39
	TMDS_DN<1>	TMDS_D1			10 MIL SPACING		20 22 39
	TMDS_DP<1>	TMDS_D1			10 MIL SPACING		20 22 39
	TMDS_DN<2>	TMDS_D2			10 MIL SPACING		20 22 39
	TMDS_DP<2>	TMDS_D2			10 MIL SPACING		20 22 39
USB	NEC_USB_DAM	NEC_USB_DA		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DAP	NEC_USB_DA		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DEM	USB_DE			5 MIL SPACING		14
	USB_DEP	USB_DE			5 MIL SPACING		14
	NEC_USB_DBM	NEC_USB_DB		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DBP	NEC_USB_DB		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DFM	USB_DF			5 MIL SPACING		14
	USB_DFP	USB_DF			5 MIL SPACING		14
	BT_USB_DM	BT_USB_D			5 MIL SPACING		14 24 39
	BT_USB_DP	BT_USB_D			5 MIL SPACING		14 24 39
	NEC_USB_RSDM1	NEC_USB_RSD1		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP1	NEC_USB_RSD1		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDM2	NEC_USB_RSD2		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP2	NEC_USB_RSD2		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	MODEM_USB_DM	MODEM_USB_D			5 MIL SPACING		14 25 39
	MODEM_USB_DP	MODEM_USB_D			5 MIL SPACING		14 25 39
	LEFT_USB_DM	LEFT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	LEFT_USB_DP	LEFT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	RIGHT_USB_DM	RIGHT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
	RIGHT_USB_DP	RIGHT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
POWER SUPPLIES	1772_CSSN	1772_CSS					31
	1772_CSSP	1772_CSS					31
	1772_CSIN	1772_CSI					31
	1772_CSIP	1772_CSI					31
	3V_SNSM	3V_SNS					33
	3V_SNSP	3V_SNS					33
	5V_SNSM	5V_SNS					33
	5V_SNSP	5V_SNS					33
THERMOSTAT	THERM1_DM	THERM1					25
	THERM1_DP	THERM1					25
	THERM2_DM	THERM2					25
	THERM2_DP	THERM2					25
	THERM1_M_DM	THERM1_MAIN					
	THERM1_M_DP	THERM1_MAIN					
	THERM2_M_DM	THERM2_MAIN					
	THERM2_M_DP	THERM2_MAIN					
	THERM1_A_DM	THERM1_ALT					25
	THERM1_A_DP	THERM1_ALT					25
	THERM2_A_DM	THERM2_ALT					25
	THERM2_A_DP	THERM2_ALT					25

INTERNAL LAYER
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.80HM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6582 | REV. C

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POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31 32
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	31
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		30 32
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		32 33
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		32
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		32
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		25 30
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 33
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
KB LED	KBD_LED1_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 39
	KBD_LED2_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 39
FAN GND	FANL_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FANR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15	25

		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	GND
I/O AREA	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND1
INVERTER	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND2
TRACKPAD	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND3
LVDS	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND4 39
I/O AREA	CHGND5	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND5
I/O AREA	CHGND6	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND6
ENET CTAP CHGND		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	27

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 34 39
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
DDR RAM	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 7 8 15 16 23 34
INTREPID	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
PLLS	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 18
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
ATI M10	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 19 39
	+GPU_MEM	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 21
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 18 19 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 18 19 21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1534	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1535	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	18
1536	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1537	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1538	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1539	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1540	+GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1541	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1542	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1543	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1544	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1545	+GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20		19
1546	+2_5V_SLEEP_NECK1	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1547	+3V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		21
1548	+1_5V_AGP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1549	+1_8V_PVDD_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		19
1550	GPU_VCORE_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1551	+GPU_VDD15_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1552	+2_5V_SLEEP_NECK2	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		21
1553	+1_8V_SLEEP_NECK	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		21
1554	+1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		21
1555	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
SILICON IMIAGE	+3V_SI_PLLVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	+3V_SI_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	+3V_SI_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
FW	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 29
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28 29
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	28
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29 39
USB 2.0	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
INTREPID SSCG	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	31 32
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	33
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		35
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		35
	2_5V_ILIM		MIN_LINE_WIDTH=8		35
	MAX1715_TON		MIN_LINE_WIDTH=8		35
	MAX1715_SKIP		MIN_LINE_WIDTH=8		35
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		35
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	34
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_ILIM		MIN_LINE_WIDTH=8		34
	VCORE_REF		MIN_LINE_WIDTH=8		34
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		34
	VCORE_CC		MIN_LINE_WIDTH=8		34
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34 39
	VCORE_TIME		MIN_LINE_WIDTH=8		34
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 34
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		34
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	19
	1778_ION		MIN_LINE_WIDTH=8		19
	1778_ITH		MIN_LINE_WIDTH=8		19
	1778_ITH_RC		MIN_LINE_WIDTH=8		19
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8		35
	1778_VFB		MIN_LINE_WIDTH=8		19 39
	1778_FCB		MIN_LINE_WIDTH=8		19
	1778_VRNG		MIN_LINE_WIDTH=8		19
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
	1_8V_VFB		MIN_LINE_WIDTH=8		
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		
	LTC3411_ITH		MIN_LINE_WIDTH=8		
	LTC3411_SYNC		MIN_LINE_WIDTH=8		
	LTC3411_SHDN		MIN_LINE_WIDTH=8		
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	

SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 38 OF 44	

FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 13 27
FUNC_TEST=YES JTAG_ASIC_TDI 13
FUNC_TEST=YES JTAG_ASIC_TDO_TP 27
FUNC_TEST=YES JTAG_ASIC_TCK 13 27
FUNC_TEST=YES JTAG_ASIC_TRST_L 13 27
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5
FUNC_TEST=YES CPU_SRESET_L 5
FUNC_TEST=YES CPU_HRESET_L 5 7 23
FUNC_TEST=YES JTAG_CPU_TMS 5 23
FUNC_TEST=YES JTAG_CPU_TDI 5 23
FUNC_TEST=YES JTAG_CPU_TDO_TP 5
FUNC_TEST=YES JTAG_CPU_TCK 5 23
FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39

FUNC_TEST=YES INT_I2C_CLK0 11 13 23
FUNC_TEST=YES INT_I2C_DATA0 11 13 23
FUNC_TEST=YES INT_I2C_CLK1 13 14 25
FUNC_TEST=YES INT_I2C_DATA1 13 14 25
FUNC_TEST=YES CBUS_DET_1_L 17
FUNC_TEST=YES CBUS_DET_2_L 17
FUNC_TEST=YES TMDS_DN<0> 20 22 37
FUNC_TEST=YES TMDS_DP<0> 20 22 37
FUNC_TEST=YES TMDS_DN<1> 20 22 37
FUNC_TEST=YES TMDS_DP<1> 20 22 37
FUNC_TEST=YES TMDS_DN<2> 20 22 37
FUNC_TEST=YES TMDS_DP<2> 20 22 37
FUNC_TEST=YES TMDS_CONN_CLKN 22 37

FUNC_TEST=YES TMDS_CONN_CLKP 22 37
FUNC_TEST=YES VGA_R 22
FUNC_TEST=YES VGA_G 22
FUNC_TEST=YES VGA_B 22
FUNC_TEST=YES VGA_VSYNC 22
FUNC_TEST=YES VGA_HSYNC 22
FUNC_TEST=YES DVI_DDC_CLK_UF 22
FUNC_TEST=YES DVI_DDC_DATA_UF 22
FUNC_TEST=YES DVI_HPD_UF 22
FUNC_TEST=YES LVDS_L0N 19 22 37
FUNC_TEST=YES LVDS_L0P 19 22 37
FUNC_TEST=YES LVDS_L1N 19 22 37
FUNC_TEST=YES LVDS_L1P 19 22 37
FUNC_TEST=YES LVDS_L2N 19 22 37
FUNC_TEST=YES LVDS_L2P 19 22 37
FUNC_TEST=YES CLKLVDS_LN 19 22 37
FUNC_TEST=YES CLKLVDS_LP 19 22 37
FUNC_TEST=YES LVDS_U0N 19 22 37
FUNC_TEST=YES LVDS_U0P 19 22 37
FUNC_TEST=YES LVDS_U1N 19 22 37
FUNC_TEST=YES LVDS_U1P 19 22 37
FUNC_TEST=YES LVDS_U2N 19 22 37
FUNC_TEST=YES LVDS_U2P 19 22 37
FUNC_TEST=YES CLKLVDS_UN 19 22 37
FUNC_TEST=YES CLKLVDS_UP 19 22 37
FUNC_TEST=YES LVDS_DDC_CLK 19 22
FUNC_TEST=YES LVDS_DDC_DATA 19 22
FUNC_TEST=YES BRIGHT_PWM 22
FUNC_TEST=YES TV_GND1 22 38
FUNC_TEST=YES TV_GND2 22 38

FUNC_TEST=YES TV_C 22
FUNC_TEST=YES TV_Y 22
FUNC_TEST=YES TV_COMP 22
FUNC_TEST=YES SND_TO_AUDIO 14 25
FUNC_TEST=YES SND_SYNC 14 25
FUNC_TEST=YES SND_CLKOUT 14 25 36

FUNC_TEST=YES INT_AUDIO_TO_SND 14 25
FUNC_TEST=YES SND_SCLK 14 25 36
FUNC_TEST=YES SND_HW_RESET_L 14 25
FUNC_TEST=YES SND_HP_SENSE_L 14 25
FUNC_TEST=YES SND_LIN_SENSE_L 14 25
FUNC_TEST=YES INT_I2C_DATA2 14 25
FUNC_TEST=YES INT_I2C_CLK2 14 25
FUNC_TEST=YES CHGND4 38
FUNC_TEST=YES SLEEP_LED 23 25

FUNC_TEST=YES BT_USB_DM 14 24 37
FUNC_TEST=YES BT_USB_DP 14 24 37
FUNC_TEST=YES MODEM_USB_DM 14 25 37
FUNC_TEST=YES MODEM_USB_DP 14 25 37
FUNC_TEST=YES PCI_AD<0> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<1> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<2> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<3> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<4> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<5> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<6> 9 12 17 24 26 37

FUNC_TEST=YES PCI_AD<7> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<8> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<9> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<10> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<11> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<12> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<13> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<14> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<15> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<16> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<17> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<18> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<19> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<20> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<21> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<22> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<23> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<24> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<25> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<26> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<27> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<28> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<29> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<30> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<31> 9 12 17 24 26 37
FUNC_TEST=YES PCI_FRAME_L 12 17 24 26 37
FUNC_TEST=YES PCI_TRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_IRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_DEVSEL_L 12 17 24 26 37
FUNC_TEST=YES PCI_STOP_L 12 17 24 26 37

FUNC_TEST=YES PCI_PAR 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<0> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<1> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<2> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<3> 12 17 24 26 37
FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 24
FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 24
FUNC_TEST=YES AIRPORT_PCI_INT_L 14 24
FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 24 37
FUNC_TEST=YES EIDE_OPTICAL_RD_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 24 37
FUNC_TEST=YES SND_AMP_MUTE 25
FUNC_TEST=YES SND_HP_MUTE_INV 25

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_CS1_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_RST_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_WR_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 24 37
FUNC_TEST=YES EIDE_OPTICAL_INT 24 37
FUNC_TEST=YES TPAD_F_TXD 23
FUNC_TEST=YES TPAD_F_RXD 23
FUNC_TEST=YES LID_CLOSED_L 23
FUNC_TEST=YES COMM_RESET_L 14 25
FUNC_TEST=YES COMM_SHUTDOWN 14 25
FUNC_TEST=YES COMM_RING_DET_L 14 25 30
FUNC_TEST=YES KBD_ID 23 30
FUNC_TEST=YES +5V_TPAD_SLEEP 23 38
FUNC_TEST=YES +3V_HALL_EFFECT 23 38
FUNC_TEST=YES KBD_CAPSLOCK_LED 23
FUNC_TEST=YES KBD_FUNCTION_L 23 30
FUNC_TEST=YES KBD_CONTROL_L 23 30
FUNC_TEST=YES KBD_COMMAND_L 23 30
FUNC_TEST=YES KBD_OPTION_L 23 30
FUNC_TEST=YES KBD_SHIFT_L 23 30
FUNC_TEST=YES KBD_X<0> 23 30
FUNC_TEST=YES KBD_X<1> 23 30
FUNC_TEST=YES KBD_X<2> 23 30
FUNC_TEST=YES KBD_X<3> 23 30
FUNC_TEST=YES KBD_X<4> 23 30
FUNC_TEST=YES KBD_X<5> 23 30
FUNC_TEST=YES KBD_X<6> 23 30
FUNC_TEST=YES KBD_X<7> 23 30
FUNC_TEST=YES KBD_X<8> 23 30
FUNC_TEST=YES SRCLK_TP 26
FUNC_TEST=YES SRMOD_TP 26
FUNC_TEST=YES TEB_TP 26
FUNC_TEST=YES TEST_TP 26

FUNC_TEST=YES KBD_X<9> 23 30
FUNC_TEST=YES KBD_Y<0> 23 30
FUNC_TEST=YES KBD_Y<1> 23 30
FUNC_TEST=YES KBD_Y<2> 23 30
FUNC_TEST=YES KBD_Y<3> 23 30
FUNC_TEST=YES KBD_Y<4> 23 30
FUNC_TEST=YES KBD_Y<5> 23 30
FUNC_TEST=YES KBD_Y<6> 23 30
FUNC_TEST=YES KBD_Y<7> 23 30
FUNC_TEST=YES KBD_NUMLOCK_LED 23
FUNC_TEST=YES +BATT_POS 31 38
FUNC_TEST=YES BATT_CLK 31
FUNC_TEST=YES BATT_DATA 31
FUNC_TEST=YES BATT_NEG 31 38
FUNC_TEST=YES PMU_BATT_DET_L 30 31
FUNC_TEST=YES FANR_GND 25 38

FUNC_TEST=YES FANL_GND 25 38
FUNC_TEST=YES FANL_TACH 25
FUNC_TEST=YES FANR_PWM 25
FUNC_TEST=YES FANL_PWM 25
FUNC_TEST=YES RJ45_DP<0> 27 37
FUNC_TEST=YES RJ45_DN<0> 27 37
FUNC_TEST=YES RJ45_DP<1> 27 37
FUNC_TEST=YES RJ45_DN<1> 27 37
FUNC_TEST=YES RJ45_DP<2> 27 37
FUNC_TEST=YES RJ45_DN<2> 27 37
FUNC_TEST=YES RJ45_DP<3> 27 37
FUNC_TEST=YES RJ45_DN<3> 27 37
FUNC_TEST=YES FW_TPO0R 29 38
FUNC_TEST=YES VCORE_VID0
FUNC_TEST=YES VCORE_VID1
FUNC_TEST=YES VCORE_VID2
FUNC_TEST=YES VCORE_VID3
FUNC_TEST=YES VCORE_VID4

FUNC_TEST=YES FW_TPO1P 29 37
FUNC_TEST=YES FW_TPO1N 29 37
FUNC_TEST=YES FW_TPI1P 29 37
FUNC_TEST=YES FW_TPI1N 29 37
FUNC_TEST=YES CHARGE_LED_L 30 31
FUNC_TEST=YES ADAPTER_DET 30 31
FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 24
FUNC_TEST=YES SUTRO_ALS_OUT 23 24
FUNC_TEST=YES KBD_LED1_OUT 23 38
FUNC_TEST=YES KBD_LED2_OUT 23 38
FUNC_TEST=YES COMM_TXD_L 14 25
FUNC_TEST=YES COMM_TRXC 14 25
FUNC_TEST=YES COMM_GPIO_L 14 25
FUNC_TEST=YES COMM_DTR_L 14 25
FUNC_TEST=YES COMM_RTS_L 14 25
FUNC_TEST=YES COMM_RXD 14 25
FUNC_TEST=YES PMU_KB_RESET_L 30
FUNC_TEST=YES PWR_BUTTON_L 23 25
FUNC_TEST=YES +PBUS 38
FUNC_TEST=YES +24V_PBUS 38
FUNC_TEST=YES GPU_VCORE 18 19 38
FUNC_TEST=YES CPU_VCORE_SLEEP 5 34 38
FUNC_TEST=YES VCORE_FB 34 38
FUNC_TEST=YES +1_8V_MAIN 38
FUNC_TEST=YES +3V_PMU 38
FUNC_TEST=YES +5V_DDC_SLEEP 22 38
FUNC_TEST=YES +12_8V_INV 22 38

FUNC_TEST=YES VCORE_MUX_EN 34

FUNC_TEST=YES +5V_INV_SW 22 38
FUNC_TEST=YES LEFT_USB_DM 24 26 37
FUNC_TEST=YES LEFT_USB_DP 24 26 37
FUNC_TEST=YES RIGHT_USB_DM 26 32 37
FUNC_TEST=YES RIGHT_USB_DP 26 32 37
FUNC_TEST=YES NEC_LEFT_USB_PWREN 24 26
FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 24 26
FUNC_TEST=YES NEC_RIGHT_USB_PWREN 26 32
FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 26 32
FUNC_TEST=YES DCDC_EN 19 29 32 33 34
FUNC_TEST=YES BBANG_HRESET_L 23

FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 24 26 30
FUNC_TEST=YES RF_DISABLE_L_SPN 24
FUNC_TEST=YES AIRPORT_CLKRUN_L 24
FUNC_TEST=YES ROM_RW_L 9 12 24
FUNC_TEST=YES ROM_ONBOARD_CS_L 9 24
FUNC_TEST=YES ROM_CS_L 9 12 24
FUNC_TEST=YES CLK33M_AIRPORT 12 24 36
FUNC_TEST=YES AIRPORT_IDSEL 24
FUNC_TEST=YES ROM_OE_L 9 12 24
FUNC_TEST=YES INT_MOD_DTI 14 25
FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39
FUNC_TEST=YES MOD_BITCLK 14 25
FUNC_TEST=YES MOD_CLKOUT 14 25
FUNC_TEST=YES MOD_DTO 14 25
FUNC_TEST=YES MOD_SYNC 14 25
FUNC_TEST=YES SLEEP 23 25 30 33 35
FUNC_TEST=YES 1778_VFB 19 38

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 39 OF 44	

REVISION HISTORY

REV 0.01 - 03/06/2003

3/3
1) Initial check-in of Enterprise schematic after conversion to Concept 14.2

3/10
2) added 8 new 10uF vcore caps
3) added jumpers at 1.5V, 1.8V, 2.5V, 3.3V, 5V, and PBUS supply outputs
4) added 8 more 0.1uF vcore byapass caps

3/11
5) removed dedicated boot banger circuit (U5400,U5200,RP46,U9,U1000)
6) updated firewire to phy to rev A prt number
7) changed cpu PLL config to 1083/833
8) changed reset to U56 (clock slewing chip) to MAIN_RESET_L
9) changed C550 to 138S0536 to limit AVL
10) changed Vcore stuffing options to 1.4V/1.025V using analog mux to support slewing
11) changed stuffing to set Vcore offset to 0mV by default
12) changed comments to eliminate references to L3 in power supply section

3/18
13) changed stuffing options for GPU PCI ID to 0x319
14) changed R164 (DAC1RSET) to 107 ohm pulldown
15) added 10K pulldown to U43 pin A21
16) changed fan controller to ADT7460

3/19
17) added pads for 0.1uF cap from +Adapter to digital gnd for EMC
18) added pads for 0 ohm between chassis and digital gnd near ENET connector for EMC
19) corrected path to correct for last checkin
20) removed BOM table for MAP31
21) REMOVED ALL RELATIVE_PROPAGATION_DELAY AND PROPAGATION_DELAY PROPERTIES TO PRERPARE FOR CONSTRAINT BACK ANNOTATION
22) changed CHGND on R616 to CHGND1
23) ***BOARD RENUMBERED***

3/28
24) integrated M10 pages from Q16 schematic and renumbered them

4/10
25) updated physical constraints for M10 power nets
26) added DP7 for M10 power sequencing
27) added RP27,RP28,RP32, and RP57 for TMDS series termination
28) update PLL CFG high 0010 1.25GHz
low 1011 833MHz
29) update sscg/nosscg stuffing option on intrepid boot straps
30) removed D31 between +Batt and 24V_Pbus
31) add Vcore DAC resistors (R288,R289,R290,R292) for no mux case
32) change intrepid PLL LDO stuffing back to 1.8V main
33) change C640 and C646 to 0.01uF (Apple # 132S1047) for FW check config
34) change I2C pullups (R29 and R102) to 1K
35) changed bootrom part number to 341S1255

4/18
36) changed C756 to 128S0025 (Sanyo only 6.3V 330uF)
37) add pads for 90 ohm chokes to FWB path close to connector (route through the pads)
38) changed Vcore inductor (L36) to molded core part (152S0125)
39) changed Pbus inductor (L37) to molded core part (152S0126)
40) added seperate 1_8V_GPU_TPVDD filter and LDO (U54)

4/21
41) replace disctrete LCL with single chip LCL filters (155S0154) for VGA (L ,L , and L)
42) add 165 ohm chokes on TMDS data pairs at connector (L ,L , and L)
43) move BS1 to bottom side
44) move CPU thermal sensor (Q39) to input 1 on fan controller and power supply sensor (Q66) to input 2
45) added trace from Vcore to fan controller ADC input
46) added FET inverters (Q78) to PWM outputs of fan controller (U3) to prevent spinup at boot
47) added FET (Q79) for +3V_Sleep for M10 power sequencing

4/27
48) changed TMDS data chokes to 90 ohm (155S0128)
49) changed C762 and C766 to 4.7uF 1206 caps
50) changed TMDS data chokes to 90 ohms (155S0128)
51) changed C762 and C766 to 4.7uF 1206
52) changed Q51 to Si7860DP (376S0119)
53) changed Q48 to Si7892DP (376S0120)
54) changed D24 to B340LB (371S0132)
55) changed L30 to 2.2uH Tokin inductor (152S0139)
56) added Q58, R307, and C515 for GPU Vcore control inverter
57) changed R416 to 2.2ohms
58) changed R364 to 102K
59) added 0.1uF 50V C883 to RS- of Max4172 (NO stuff)
60) changed D18 to 1N914
61) changed L38 and L41 to 4.7uH (152S0137)
62) added Q81, R308, R309, and R310 for power sequencing (no stuff)
63) changed Q49 and Q50 to Si7860DP (376S0119)
64) changed L36 to 1.2uH 18.3A (152S0125)
65) added R331 1mohm sense resistor to CPU Vcore
66) added C885 and C884 , 1000uF CPU Vcore outpur caps
67) added Q82, R607, R455, R417, and C886 for 1.5V sleep sequencing
68) added Q83 and 100K R698 for 1.8V sequencing
69) added 15.4K R616 and 10K R672 for 2.5V switcher feedback divider
70) changed pinout of sound connector for sousaphone
71) removed Q44 (5V sound sleep fet)
72) changed Q31 to invert headphone Mute to sousaphone

4/28
73) changed CPU_VCORE_SLEEP location back to across bypass caps to correct after adding reference resistor
74) changed D5 to schottky diode (MBR0540)
75) fixed unnamed net (LTC3411_SHDN_SEQ)
76) changed drain/source polarity of Q76 (FET from +BATT to Pbus)

4/28
77) moved XW15 to connect to CPU_VCORE_SLEEP_UF (before positioning resistor)
78) changed Fan control nets to FanL and FanR from Fan1 and Fan2
79) SWAPPED CONNECTIONS SO THAT OUTPUT 1 FROM FAN CONTROLLER CONNECTS TO LEFT FAN (CPU) AND FAN 2 CONNECTS TO THE RIGHT FAN (GPU)
80) updated power constraints with new fan net names

4/28
81) change Q58 on pg19 to Q80 to consolidate parts
82) CHANGED U55 TO MM1571J FOR COST SAVINGS
83) changed L72,L73,L74 to 90 ohm ferrites
84) added 10K pullup to +5V_MAIN to SND_HP_MUTE
85) repinout Sousaphone connector
86) remore redundant pullups on FANL_TACH and FANR_TACH
87) added TP to all NC on NEC USB2 part for NAND tree testing
88) added NEC_USB bomoption to 0 ohm resistor on NEC_AVSS_F

4/30
89) repinout Sousaphone connector (J12)
90) no stuff R322 to eliminate 3V_sleep pump up
91) updated various text notes with correct reference designators

5/1
92) change L30 to 152S0139 (Tokin CPI-1050-2R2) 11A
93) remove FANR_TACH functional test point
94) add CHGND4 and SLEEP_LED functional test points
95) swap INT_AUDIO_TO_SND and SND_TO_AUDIO on Sousaphone connector (J12)
*** rev 01 released for EVT ***

5/6
96) remove NO STUFF on R477 (set 5V and 3.3V switcher in pulse skipping mode)
97) change R337 to 470K and remove No Stuff and no stuff R336 to change Vcore DAC to 1.35V/1.15V
98) change R321 to 499ohm to set 5mV Vcore offset
99) change L72,L73,L74 to 155S0165 (D part for EVT only)
*** rev 02 released for EVT ***

5/7
100) no stuff Q79 to disable 3V_SLEEP sequencing to work around wake from sleep bug with M10
101) added BOM table to define correct part number for M10 without heatspreader (338S0133)
*** rev 03 released for EVT ***

5/22
102) fixed NO STUFF BOM option for R291
103) add NO STUFF to R223 to correct startup level of GPU_VCORE_CNTL
104) add NO STUFF to R300 to complete 3V sequecing on wake from sleep fix
105) changed R376 to 158K and R321 to 2.74K to set CPU_VCORE offset to 35mV
*** rev 04 released for EVT ***

5/19/03
106) changed both AGP_NV_INT_L and AGP_ATI_INT_L to AGP_INT_L
107) removed redundant 3V_GPU pullup R687 (Intrepid side AGP_INT_L pullup)
108) added R699,R701,R707,R708 as 10k pulldowns to Intrepid USB ports A and C when NEC_USB is stuffed
109) changed SND_HP_MUTE_INV gate/inversion FETS to pullup to +3V_MAIN
110) added R711 as pullup to +3V_GPU on AUXWIN signal from M10 (U44)
111) added R698 as 0 ohm jumper between FW_PHY_PD and Intrepid
112) added U56, U57, R718,R714 for VGA Hsync and VGA Vsync buffering
113) changed L72,L73,L74 to 155S0164 (new high speed part)
114) added NO STUFF BOM option to R223 to correct for sense of GPU_VCORE_CNTL
115) added NO STUFF BOM option to R300 to avoid sleep wake problem

6/3/03
116) Intgrated new 1.8V switcher (LTC3412)(U58)(353S0650) and inductor (L75- 152S0142)
117) changed 2.5V_SLEEP FET (U48) and 1.8V_SLEEP FET (U6) to higher current part (Si6467BDQ - 376S0161)
118) added 10K pulldown (R720) on FW_PHY_PD_INT for when R698 is removed
119) changed R728 and R729 to 1210 0ohm resistors to support switching the entire memory bus between 1.8V and 2.5V
120) added R721 as jumper between +2_5V_SLEEP and +2_5V_GPU

6/4/03
121) NO STUFF R631 to remove MAIN_RESET_L from clock slewing chip
122) changed FWB connector to new part with extra ground tabs (514S0059)

6/5/03
123) changed I2C 0 and 1 pullups (RP12) to 2.2K to improve rise/fall times (sensor check config errors)
124) added CRITICAL flag to new 1.8V switcher (U58), inductor (L75), 1.8V sleep FET (U6), and 2.5V sleep FET (48)
125) removed gnd caps (C651 and C647) on I2S clock at sound connector (J12)
126) added LC filter on SND_SYNC for EMI (L77 and C895)
127) added LC filter on SND_CLKOUT for EMI (80 and C899)
128) added LC filter on INT_AUDIO_TO_SND for EMI (L81 and C896)
129) added LC filter on SND_TO_AUDIO for EMI (L82 and C897)
130) added LC filter on SND_AMP_MUTE for EMI (L76 and C898)
131) added LC filter on SND_HW_RESET_L for EMI (L78 and C900)
132) added LC filter on SND_SCLK for EMI (L79 and C901)
133) added C902 and R804 to prevent latch-up condition in GPU Vcore circuit when using powermiser
134) removed R331 (CPU Vcore positioning resistor)
135) changed C728,C729,C730,C731,C732,C733,C734,C884,C885 to 220uF Rubycon caps (128S0024)
136) add Vcore offset change circuit to modify offset in low (Q86,R805,R806,R807,R808,R809)
137) changed Q83 into dual (2N7002DW) and added R810 to invert 3V_5V_ON before switching RUN/SS

6/6/03
138) rotated J26 (FW B connector)
139) changed D29 to B340B (3A part - 371S0159)

6/9/03
140) modified Vcore offset select circuit with Takashi's changes - changed Gnd reference to VCORE_GND_SNS
141) added double inverter to buffer THERM_L_OC (added Q87,R811,R812)
142) removed redundant pullup on THERM_L_OC (R780)

6/9/03
143) added cap on gate of the second FET in Q87 for possible turn on delay (C903)
144) changed inner shield of FWB connector J26 to connect to chassis gnd
145) changed R336 and R325 to 0 ohm to set Vcore VID to 1.3V/1.15V
146) changed R321 to 2.49K to set Vcore offset to +25mV
147) added 10 ohm resistor (R814) and 1uF cap (C904) to filter power to ADT7460 (Gary Leo)

6/10/03
148) changed R612 to 10K to prevent UIDE DMACK from floating
149) changed C80,C88,C81,C89,C82,C102,C79,C87 to NO STUFF (TMDS common-mode termination)
150) changed R205,R218,R211,R219,R210,R220,R204,R214 to 162 ohm 1% (TMDS common-mode termination)
151) changed RP27,RP32,RP28,RP57 to 10ohm (TMDS series termination)
*** released for EVT2 6/10/03 ***

6/13/03
152) fixed NO STUFF on R291
153) removed NO STUFF from C80,C88,C81,C89,C82,C102,C79,C87 (TMDS common-mode termination)
154) removed NO STUFF from R638 (pullup on slewing chip FSEL)
155) removed NO STUFF from C903 (cap on input to second part of THERM_OC_L buffer)
156) CHANGED R321 TO 1K FOR VCORE OFFSET OF 12MV (VCORE = 1.30V -30MV/+100MV)
*** released for EVT2 6/13/03 ***

6/18/03
157) changed R228 to pullup to 1.8V for DVO interface conpatibility
158) added R234 and INT_TMDS option to maintain internal TMDS capability
159) changed L30 to 3 pin symbol
160) added U5 to use as external TMDS transmitter (DVI)
161) added R41 to create +3V_GPU_SI power for SIL1162 (U5)
162) added L14, C130, C132, and C165 for 3V AVCC filtering for SIL1162 (U5)
163) added L13, C14, C129, C131, C133 for 3V PVCC filtering for SIL1162 (U5)
164) added L15, C255, C233, C218 for 3V Vcc filtering for SIL1162 (U5)
165) added R235 and R237 as options for MAIN_RESET_L to U5
166) added R231. R232, and C284 for Vref for U5
167) added R66, R99, R202, R212, R222, R224, R88, R110, R223 as straps for U5
168) added RP58, RP59, RP60, RP61 for series termination of SIL1162 TMDS output
169) added L16, C304, C327, C647 for filtering GPU VDDR4
170) added R255 and R251 to strap GPU_DVDOMODE correctly for 1.8V DVO
171) added R268 to connect L16 to +3V_GPU_FLT when not using SIL1162
172) added C681, C668, C678, C651 to filter the thermal sensor diff pairs

6/19/03
173) changed GPU_MEM_IO to +GPU_MEM to connect ATI Vref to correct memory voltage
174) swapped TMDS CLKN and CLKP on RP57 and RP58 for layout
175) swapped DN<0> and DP<0> on RP27 for layout
176) corrected un-named nets in TMDS common-mode filters
177) added physical constriants for new Silicon Image power rails
178) CHANGED C728,C731,C734,C733,C730,C732,C729,C885,C885 TO 128S0022
(124S0024 WILL BE DELETED AS A DUPLICATE IN THE LIBRARY)

6/23/03
179) NO STUFF'ed C895,C899,C896,C897,C898,C900, and C901 to fix no sound problem
180) changed C890 to 100pF for improved transient response (Takashi)
181) Removed bypass traces on FWB chokes and stuffed L70 and L71
182) CHANED R491 TO 52.3K 1%, R475 TO 127K 1%, AND R476 TO 4.7M 5% IN A29 ADAPTER DETECT CIRCUIT DIVIDERS TO REDUCE SHUTDOWN CURRENT
183) added R331 as CPU Vcore sense resistor (1 mohm 1% 2512)
184) No STUFF'ed C651 and C678
185) added C688,C690,C846,C905 for thermal pair filtering at fan controller
186) added C906 to prevent shoot-thru on Q64 (currently NO STUFF'ed)
187) added C907 to prevent shoot-thru on Q68 (currently NO STUFF'ed)
188) changed R517 to 100K
189) changed GND reference for input side of Q86 to digital GND (the other FET in Q856 remains on VCORE_GNDSNS

6/24/03
190) added C908 to prevent gate shoot-thru on Q56
191) added R279 to power TMDS PLL from LVDS filter when using external TMDS transmitter
192) changed R325 to 470K to set the low Vcore to 1.10V
193) stuffed Vcore offset switch (R807,R805,R809,Q86)
194) changed R809 to 1.5K 1% to set low Vcore offset to 10mV
195) changed R321 to 3.01K 1% to set high Vcore offset to 30mV

6/25/03
196) rotated L70 and L71 for layout (PCB symbol problem)
197) changed Q53,Q54,Q55 to IRF7832 (376S0148) for better thermal performance
198) NO STUFF'ed C908 (Q56 gate shoot-thru cap)
*** released for DVT 6/26/03 ***

7/2/03
199) CHANGED J9 (CARDBUS) TO 516S0141 (NEW PIN PLATING SPEC)
200) CHANGED J20 (AIRPORT) TO 516S0142 (NEW PIN PLATING SPEC)
201) CHANGED J10 (OPTICAL DRIVE) TO 516S0140 (NEW PIN PLATING SPEC)
202) CHANGED J13 (HARD DRIVE) TO 516S0140 (NEW PIN PLATING SPEC)
203) CHANGED J12 (SOUND) TO 516S0144 (NEW PIN PLATING SPEC)
204) CHANGED J8 (MODEM) TO 516S0143 (NEW PIN PLATING SPEC)
205) ADDED BOM TABLE TO PUT 0 OHM 402 ON L77,L80,L81,L82,L76,L78,L79

7/9/03
207) CORRECTED C889 TO CONNECT TO INPUT (PIN 1) OF U55
208) REMOVED POWER JUMPERS XW25,XW17,XW16,XW10,XW14,XW18
209) CHANGED 197S0035 TO PRIMARY AND 197S0004 AS ALTERNATE FOR Y1 (INTREPID)
210) CHANGED 197S0037 TO PRIMARY AND 197S0603 AS ALTERNATE FOR Y3 (ETHERNET)
211) CHANGED 197S0038 TO PRIMARY AND 197S0608 AS ALTERNATE FOR Y5 (NEC USB2)
212) CHANGED 197S0040 TO PRIMARY AND 197S0008 AS ALTERNATE FOR Y4 (LMU)
213) CHANGED 197S0041 TO PRIMARY AND 197S0604 AS ALTERNATE FOR Y6 (PMU)

7/22/03
214) ADDED 1_32V_VCORE AND 1_30V_VCORE BOM OPTIONS FOR 2 DIFFERENT CPU VCORE SPECS
215) UPDATED CAP MATERIAL TYPES
216) CHANGED FROM 715 PIN TO 667 PIN SYMBOL FOR U44 (M10)

7/28/03
217) CHANGED TMDS TERMINATION FROM 2X 162 TO 2X 49.9 OHMS PER PAIR
218) CHANGED 126S0036 FROM ALT TO PRIMARY, REPLACING 126S0035 FOR CPU VCORE INPUT CAPS
*** RELEASED FOR PRODUCTION 7/28/03 ***

8/4/03
219) CHANGED R99 TO NO STUFF TO FIX I2C ADDRESS OF SIL1162 TMDS TRANSMITTER
220) CHANGED R321 TO 4.02K 1% FOR 1_30_VCORE (40MV OFFSET) AND TO 6.34K 1% FOR 1_32_VCORE (60MV OFFSET)
221) CHANGED R304 TO 470K AND R329 AND R325 TO 0 OHM TO CHANGE LOW VID TO 1.05V ON VCORE
222) CHANGED C611 TO 2200PF, C610 TO 100PF, AND R519 TO 12.7K 1% TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
223) NO STUFF C590 TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
224) CHANGED C583 TO 2200PF, C576 TO 100PF, AND R481 TO 15.0K 1% TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
225) NO STUFF C566 TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT

9/4/03
228) ADDED 197S0052 AS ALTERNATE FOR G1 (98 MHZ FW OSCILLATOR)
229) CHANGED C728-C734,C884,C885 TO 128S0022 TO REMOVE DUPLICATE PART NUMBER
230) CHANGED C883 TO 132S0100 TO CORRECT FOR USE OF OEM PART NUMBER

8/29/05
1) ADDED 338S0223 (88E1111, B1) AS OPTION
2) ADDED 128S0034 AS OPTION
3) REPLACED 740S0006 WITH 740S0018
*** PRODUCTION RELEASE FOR 051-6582-B ***

01/04/07
1) PER RADAR #4312710, ADD 338S0336 AS ALTERNATE OF 338S0168.
2) PER RADAR #4312710, REPLACE 341S1336 WITH 341S2103, DUE TO 335SXXXX EOL, WHICH REPORT TO 341S1336.
*** SERVICE BON UPDATE FOR 051-6582-C ***

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 40 OF 44	

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*** Signal Cross-Reference for the entire design ***

+1_0V_MARVELL     27D2< 38B3>
+1_5V_AGP         12C5< 12D1< 12D4< 15D6< 16C8<
                18C6< 18D6< 19A8< 19B4<> 19D5<>
                21B8< 21D6< 38C3>
+1_5V_AGP_GPU     21C5< 38C3>
+1_5V_AGP_NECK    19B4<> 38B3>
+1_5V_GPU_VDD15   19D3< 38C3>
+1_5V_INTREPID_PLL  8D6< 12D4< 12D8< 14D6<> 38D3>
+1_5V_INTREPID_PLL1  14C3< 38D3>
+1_5V_INTREPID_PLL2  14D3< 38D3>
+1_5V_INTREPID_PLL3  14D3< 38D3>
+1_5V_INTREPID_PLL4  14D3< 38D3>
+1_5V_INTREPID_PLL5  12D3< 38D3>
+1_5V_INTREPID_PLL6  12D6< 38D3>
+1_5V_INTREPID_PLL7  8D5< 38D3>
+1_5V_INTREPID_PLL8  14D3< 38D3>
+1_5V_LDO         35D8< 38D6>
+1_5V_MAIN        38D6>
+1_5V_SLEEP       38D6>
+1_5V_SLEEP_NECK  21A3<> 38B3>
+1_5V_SLEEP_VIN   35D8<> 38D6>
+1_8V_ATI_PVDD    19C5<> 21B6< 21B6< 21D6<> 38C3>
+1_8V_ATI_TPVDD   21D2<>
+1_8V_DVO_F       21B2<
+1_8V_GPU         18A7< 19D8< 20A5< 21A2< 21A6<
                21B1< 21B6< 21C8< 21D6< 21D8< 38C3>
+1_8V_GPU_AVDD    21D5< 38C3>
+1_8V_GPU_AVDDQ   21D4< 21D7< 38C3>
+1_8V_GPU_MEMPLL  21B5< 38C3>
+1_8V_GPU_PLL     21D5< 38C3>
+1_8V_GPU_PNLIO   21A5< 38C3>
+1_8V_GPU_PNLPLL  21B5< 38C3>
+1_8V_GPU_TP_PLL  21B4< 21D1<
+1_8V_GPU_VDDDI   21C7< 21D4< 38C3>
+1_8V_MAIN        38D6> 39A2>
+1_8V_MAIN_LX_F   35A4<>
+1_8V_PVDD_NECK   19B5<> 38B3>
+1_8V_SLEEP       38D6>
+1_8V_SLEEP_NECK  21A3<> 38B3>
+1_95V_FW_DVDD    28C4< 28C7<> 28D5< 38A3>
+1_95V_FW_DVDD_PORT1  28D6< 38A3>
+1_95V_FW_DVDD_RX0  28C5< 38A3>
+1_95V_FW_DVDD_TX0  28C5< 38A3>
+1_95V_FW_PLL400VDD  28D5< 38A3>
+1_95V_FW_PLL500VDD  28D5< 38A3>
+1_95V_FW_PLLVDD  28D5< 28D7<> 38A3>
+2_5V_CG_MAIN     14C6< 38A3>
+2_5V_GPU         21A7< 21B6< 21D3< 21D7< 21D8<
                38B3>
+2_5V_GPU_A2VDD   21D4< 21D7< 38C3>
+2_5V_GPU_PNLIO   21A5< 38C3>
+2_5V_INTREPID    9A8< 10D3< 10D5< 10D7< 10D8< 15D7<
                16B8< 38D3>
+2_5V_MAIN        38D6>
+2_5V_MARVELL     27B8< 27C4<> 38B3>
+2_5V_MARVELL_AVDD  27C4< 38B3>
+2_5V_SLEEP       38D6>
+2_5V_SLEEP_NECK1  19C4<> 38B3>
+2_5V_SLEEP_NECK2  21A3<> 38B3>
+3V_ATI_OSC_SLEEP  18D2< 38C3>
+3V_ATI_SS        18B2< 38C3>
+3V_CG_PLL_MAIN   14C6< 38A3>
+3V_FW            28A3< 28D7<> 29D5< 38A3>
+3V_FW_AVDD       28C6< 38A3>
+3V_FW_AVDD_PORT0  28C6< 38A3>
+3V_FW_AVDD_PORT1  28C6< 38A3>
+3V_FW_AVDD_PORT2  28D6< 38A3>
+3V_FW_ESD        29B3<> 29D2<> 38B3>
+3V_FW_ESD_ILIM   29D4< 38B3>
+3V_FW_UF         28D7<> 38A3>
+3V_GPU           12D1< 18B8< 18C5< 18C7< 18D6<
                19C4< 19C5< 19C7< 19D7< 21A6< 21B1<
                38C3>
+3V_GPU_FLT       21B2< 38C3>
+3V_GPU_SI        20C4< 20C8< 20D8<
+3V_HALL_EFFECT   23C6<> 38B6> 39C4>
+3V_INTREPID_USB  14C3< 38D3>
+3V_LCD           22B4<> 38B6>
+3V_LCD_SW        22A4<> 38B6>
+3V_MAIN          38D6>
+3V_NEC_VDD       26D7< 26D7< 38A3>
+3V_PMU           38D6> 39A2>
+3V_PMU_AVCC      25A4< 30B6< 30D5<> 38C6>
+3V_PMU_ESR       32A2< 38C6>
+3V_PMU_RESET     30B7< 34A3<>
+3V_SI_AVCC       20C7< 38B3>
+3V_SI_PLLVCC     20C7< 38B3>
+3V_SI_VCC        20C6< 38B3>
+3V_SLEEP         38D6>
+3V_SLEEP_NECK    21A3<> 38B3>
+3V_SLP_OK_L      33B4<>
+3V_SLP_ON        33A5<>
+4_6V_BU          32A3<> 33B6< 38C6>
+4_85V_ESR        32A4< 38C6>
+4_85V_RAW        30B4< 32A4<> 38C6>
+5V_DDC_SLEEP     22D3<> 22D5<> 38B6> 39A2>
+5V_DDC_SLEEP_UF  22D6< 38B6>
+5V_HD_SLEEP      24D1<> 33A7<> 38C6>
+5V_INV_SW        22B2<> 38B6> 39D1>
+5V_INV_UF_SW     22B2<> 38B6>
+5V_MAIN          38D6>
+5V_SLEEP         38D6>
+5V_SOUND_SLEEP   38B6>
+5V_TPAD_SLEEP    23C7<> 38B6> 39C4>
+12_8V_INV        22B1<> 38B6> 39A2>
+24V_PBUS         38D6> 39B2>
+ADAPTER          31D8<> 32B7<> 38D6>
+ADAPTER_ILIM     32B6<> 38C6>
+ADAPTER_OR_BATT  32A5<> 38C6>
+ADAPTER_SENSE    31D5<> 38C6>
+ADAPTER_SW       31D6<> 38C6>
+BATT             38D6>
+BATT_14V_FUSE    31D1<> 38C6>
+BATT_24V_FUSE    31B1< 31D2<> 38C6>
+BATT_POS         31A4<> 38C6> 39C3>
+BATT_RSNS        31B2< 38C6>
+BATT_VSNS        31A4< 38C6>
+FW_FUSE          29D7<> 38A3>
+FW_PWR_OR        28B8< 28D8<> 29D5<> 38A3>
+FW_PWR_PORTA     29C5< 38A3>
+FW_SW            29D5<> 38A3>
+FW_VP0           29C2<> 38A3>
+FW_VP1           29A3<> 38A3>
+GPU_MCLK         21C7< 21D4< 38C3>
+GPU_MEM          18A6<> 18B8< 21B4< 21B7< 21C6<
                21C8< 21D2< 38C3>
+GPU_MEMCORE      21C5< 38C3>
+GPU_VDD15_NECK   19B5<> 38B3>
+GPU_VDD15_UF     19B5<> 19D4<> 38C3>
+HD_LOGIC_SLEEP   24C2<> 38C6>
+PBUS             38D6> 39B2>
+VCC_CBUS_SW      17B1<> 17B2<> 17D2<> 38D3>
+VPP_CBUS_SW      17B1<> 17B2<> 17D2<> 38C3>
1V20_REF          31C7< 32C8< 38D1>
1V65_REF          31A5<
1_5V_2_5V_OK      35C5< 38B1>
1_5V_BOOST        35C6<> 38C1>
1_5V_BST          35C5<> 38C1>
1_5V_DH           35C5<> 38C1>
1_5V_DL           35B5<> 38C1>
1_5V_FB           35B5< 35B7< 38C1>
1_5V_ILIM         35C5<> 38C1>
1_5V_LX           35B5<> 38C1>
1_5V_SLEEP_EN_L   35C7<> 35D7<>
1_8V_SLEEP_PWREN_L  35A3<>
1_8V_SW           35A5<> 38A1>
1_8V_VFB          38A1>
2_5V_BOOST        35C4<> 38D1>
2_5V_BST          35C4<> 38D1>
2_5V_DH           35C4<> 38D1>
2_5V_DL           35B4<> 38D1>
2_5V_ILIM         35C5<> 38C1>
2_5V_LX           35B4<> 38D1>
2_5V_SLEEP_PWREN_L  35C2<>
2_34V_REF         30A4<
3V_5V_OK          33B4<> 35A8<> 35D6<
3V_5V_OK_INV      35A8<>
3V_BG             33C4<>
3V_BOOST          33C4<>
3V_BOOST_ESR      33D3<>
3V_ITH            33C4<>
3V_ITH_RC         33C3<
3V_PMU_VTAP       32B3<
3V_RSNS           33D2< 38D1>
3V_RUNSS          33C4<
3V_SLEEP_PWREN_L  33A3<>

3V_SNSM           33C4< 37A2>
3V_SNSP           33C4< 37A2>
3V_SW             33C4<> 38D1>
3V_TG             33D4<>
3V_VOSNS          33C4<>
5V_BG             33C5<>
5V_BOOST          33C5<>
5V_BOOST_ESR      33D6<>
5V_HD_PWREN       33A8<>
5V_ITH            33C5<>
5V_ITH_RC         33C6<
5V_RSNS           33D7< 38D1>
5V_RUNSS          33C5<
5V_SLEEP_PWREN    33A8<>
5V_SNSM           33C5< 37A2>
5V_SNSP           33C5< 37A2>
5V_SW             33C5<> 38D1>
5V_TG             33C5<>
5V_VOSNS          33C5<>
1625_BG           32C5<>
1625_BST          32C5<
1625_BST_ESR      32C5<>
1625_COMP         31D2< 32C6<
1625_DIV          32C8<
1625_ENABLE       32D7<>
1625_ENABLE_L     32D6<>
1625_EXTVCC       32D5<> 38D1>
1625_FCB          32C6<
1625_INTVCC       32C5<> 38D1>
1625_RUNSS        32C6<
1625_SGND         32B7<> 38D1>
1625_TG           32C5<>
1625_VFB          32B5<>
1625_VIN          32C6< 38D1>
1625_VSW          32C4<> 38D1>
1772_ACIN         31B5<
1772_ACOK_L       31B5<> 31C4<>
1772_BST          31B4<>
1772_BST_ESR      31C3<
1772_CCI          31B5<>
1772_CCS          31B5<
1772_CCV          31B5<>
1772_CCV_RC       31B5<
1772_CELLS        31B4<
1772_CLS          31A4<
1772_CSIN         31B4<> 37A2>
1772_CSIP         31B4<> 37A2>
1772_CSSN         31C5< 37A2>
1772_CSSP         31C5< 37A2>
1772_DCIN         31B5< 38C6>
1772_DHI          31B4<>
1772_DLO          31B4<>
1772_DLOV         31B4<> 38C6>
1772_GND          31A5<> 38C6>
1772_ICHG         31B5<>
1772_ICTL         31B5<>
1772_IINP         31B5<
1772_LDO          31C4<> 38C6>
1772_LX           31B4<> 38C6>
1772_REF          31B5<>
1772_VCTL         31B5<
1778_BG           19A5<> 38B1>
1778_BST          19A5<> 38B1>
1778_BST_RC       19A4<> 38B1>
1778_FCB          19A5< 38B1>
1778_GND          19A5< 19A7<> 38B1>
1778_ION          19A5<> 38B1>
1778_ITH          19A5<> 38B1>
1778_ITH_RC       19A7< 38B1>
1778_SHDN_L       19A6<
1778_SHDN_L_D3COLD  19A7<>
1778_TG           19A5<> 38B1>
1778_VCC          19A5<> 38B1>
1778_VFB          19A2< 19A5< 38B1> 39A1>
1778_VIN          19A5< 38B1>
1778_VRNG         19A5< 38B1>
3405_MODE         27D5<
3405_VFB          27D4<>
3707_FCB          33C5<
3707_FSET         33C5<
3707_INTVCC       33D4<> 38D1>
3707_SGND         33B5<> 38D1>
3707_STBY         33C5<>
A29_CLS_ADJ       31A5<>
A29_CURRENT_ADJ   31C4<>
A29_DETECT        30A2< 31A5<> 31C4<>
A29_DET_L         30A3<
AB_SEL_LOW        34A6<>
AC_DIV            31C8<
AC_ENABLE_GATE    31D6<>
AC_ENABLE_L       31C6<>
AC_GTR_18V        31C4<>
AC_IN             27B8<> 29C7< 30B3< 31C5<> 31C7<>
AC_IN_FW_CNTL     29C7<>
AC_IN_L           31C2<> 31C6<>
AC_IN_L_RC        31C2<>
ADAPTER_DET       30A4<> 31D8<> 39C2>
ADAPTER_I_REG     31D3<>
ADT7460_ADR_EN_L  25B3<>
ADT7460_FAN1_PWM  25B3<>
ADT7460_FAN2_PWM  25B3<>
ADT7460_THERM     25A5<> 25B3<>
ADT7460_VCC       25C4<
ADT7460_VCORE_MON  5C8<> 25B4<>
AGP8X_DET_PU      18C6<>
AGP_AD<0>         12D2<> 18C7<>
AGP_AD<15..0>     37D5>
AGP_AD<1>         12C2<> 18C7<>
AGP_AD<2>         12C2<> 18C7<>
AGP_AD<3>         12C2<> 18C7<>
AGP_AD<4>         12C2<> 18C7<>
AGP_AD<5>         12C2<> 18C7<>
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AGP_AD<7>         12C2<> 18C7<>
AGP_AD<8>         12C2<> 18C7<>
AGP_AD<9>         12C2<> 18C7<>
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AGP_AD<12>        12C2<> 18C7<>
AGP_AD<13>        12C2<> 18C7<>
AGP_AD<14>        12C2<> 18C7<>
AGP_AD<15>        12C2<> 18C7<>
AGP_AD<16>        12C2<> 18C7<>
AGP_AD<31..16>    37D5>
AGP_AD<17>        12C2<> 18C7<>
AGP_AD<18>        12C2<> 18C7<>
AGP_AD<19>        12C2<> 18C7<>
AGP_AD<20>        12C2<> 18C7<>
AGP_AD<21>        12C2<> 18C7<>
AGP_AD<22>        12C2<> 18C7<>
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AGP_AD<26>        12C2<> 18D7<>
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AGP_AD<28>        12B2<> 18D7<>
AGP_AD<29>        12B2<> 18D7<>
AGP_AD<30>        12B2<> 18D7<>
AGP_AD<31>        12B2<> 18D7<>
AGP_AD_STB<0>     12A2<> 12B2< 18D6<> 37D5>
AGP_AD_STB<1>     12A2<> 12B2< 18D6<> 37D5>
AGP_AD_STB_L<0>   12A2<> 12B2< 18D6<> 37D5>
AGP_AD_STB_L<1>   12A2<> 12A2< 18D6<> 37D5>
AGP_ATI_RESET_L   18B7<
AGP_ATI_VREF      18B7<
AGP_ATI_VREFG     18B7<
AGP_BUSY_L        12C4<> 12D2< 18D6>
AGP_CBE<0>        12B2<> 18B7<>
AGP_CBE<1..0>     37D5>
AGP_CBE<1>        12B2<> 18B7<>
AGP_CBE<2>        12B2<> 18B7<>
AGP_CBE<3..2>     37D5>
AGP_CBE<3>        12B2<> 18C7<>
AGP_DEVSEL_L      12B2<> 12C2< 18B7<> 37D5>
AGP_FRAME_L       12B2<> 12C2< 18B7<> 37D5>
AGP_GNT_L         12C2< 12D2<> 18B7< 37D5>
AGP_INT_L         14B5<> 18B7<>
AGP_IRDY_L        12B2<> 12C2< 18B7<> 37D5>
AGP_PAR           12B2<> 18B7> 37D5>
AGP_PIPE_L        12A2<> 12B2<
AGP_RBF_L         12A2<> 12C2< 18C6> 37D5>
AGP_REQ_L         12C2< 12D2<> 18B7<> 37D5>
AGP_SBA<0>        12B2< 18C6>
AGP_SBA<7..0>     37D5>
AGP_SBA<1>        12B2<> 18C6>
AGP_SBA<2>        12B2<> 18C6>
AGP_SBA<3>        12B2<> 18C6>
AGP_SBA<4>        12B2<> 18C6>

AGP_SBA<5>        12B2<> 18C6>
AGP_SBA<6>        12B2<> 18C6>
AGP_SBA<7>        12B2<> 18C6<>
AGP_SB_STB        12B2<> 12B2< 18C6<> 37D5>
AGP_SB_STB_L      12A2<> 12A2< 18C6<> 37D5>
AGP_ST<0>         12A2<> 18C6<
AGP_ST<1>         12A2<> 18C6<
AGP_ST<2>         12A2<> 18C6<
AGP_STOP_L        12B2<> 12C2< 18B7<> 37D5>
AGP_STP_L         18C6<
AGP_SUS_STAT_L_PU  18C6<
AGP_TRDY_L        12B2<> 12C2< 18B7<> 37D5>
AGP_WBF_L         12A4<> 12B2< 18B7>
AIRPORT_CLKRUN_L  24C6<> 39C1>
AIRPORT_IDSEL     24C5<> 39B1>
AIRPORT_PCI_GNT_L  12D7<> 24D5<> 39C4>
AIRPORT_PCI_INT_L  14B5<> 14D7<> 24D5<> 39C4>
AIRPORT_PCI_REQ_L  12A7< 12D7<> 24D6<> 39D4>
AIRPORT_PME_L_TP  24D5<>
AMP_CONTROL       25C5<> 25D5<>
ATI_AGP_FBSKEW<0>  19C2< 19C7<>
ATI_AGP_FBSKEW<1>  19C2< 19C7<>
ATI_BUS_CFG<0>    19B2< 19C7<>
ATI_BUS_CFG<1>    19B2< 19C7<>
ATI_BUS_CFG<2>    19B2< 19C7<>
ATI_CLK27M_IN     18C1< 19B7<
ATI_CLK27M_OSC    18D2<
ATI_CLK27M_OSC_SS  18B2< 18D1<
ATI_DBI_HI_PU     18C6<>
ATI_DBI_LO_PU     18C6<>
ATI_DVODMODE      21A3<
ATI_GPIO7_SPN     19C7<>
ATI_GPIO8_PD      19C7<>
ATI_GPIO9_SPN     19C7<>
ATI_GPIO10_SPN    19C7<>
ATI_GPIO11_SPN    19C7<>
ATI_GPIO12_SPN    19C7<>
ATI_GPIO13_SPN    19C7<>
ATI_HSYNC         19D5<> 22C8<
ATI_MEMTEST       18A6<>
ATI_MEMVMODE0     18A7<
ATI_MEMVMODE1     18A7<
ATI_OSC_OE        18D3<
ATI_PVDD_BYP      21D6<>
ATI_R2SET         19D6<>
ATI_RSET          19D6<>
ATI_RSTB_MSK      18C6<>
ATI_SSCLK_IN      18B1< 19B7<>
ATI_SSCLK_UF      18B1<>
ATI_TESTEN        19B7<
ATI_TMDS_CLKN     19B7> 20B4<
ATI_TMDS_CLKP     19B7> 20B4<
ATI_TMDS_DN<0>    19B7> 20B4<
ATI_TMDS_DN<1>    19B7> 20A4<
ATI_TMDS_DN<2>    19B7> 20A4<
ATI_TMDS_DP<0>    19B7> 20B4<
ATI_TMDS_DP<1>    19B7> 20A4<
ATI_TMDS_DP<2>    19B7> 20A4<
ATI_TPVDD_BYP     21D1<>
ATI_VSYNC         19D5<> 22C8<
ATI_X1CLK_SKEW<0>  19C2< 19C7<>
ATI_X1CLK_SKEW<1>  19B2< 19C7<>
BATTV_HIGH        31B7<>
BATTV_LOW         31B8<>
BATT_14PBUS_EN    31C1<>
BATT_14V_GATE     31C1<>
BATT_24PBUS_EN    31C2<>
BATT_24V_GATE     31C1<>
BATT_CLK          31A4<> 39C3>
BATT_DATA         31A4<> 39C3>
BATT_DIV          31A5<
BATT_LOW          31A6<>
BATT_LOW_L        31B6<>
BATT_NEG          31A4<> 38C6> 39C3>
BBANG_HRESET_L    23A4< 23C4<> 39C1>
BBANG_JTAG_TCK    23B3< 23C4<>
BBANG_TCK_EN      23B3<
BCKFD_PROT_EN_L   31C6<>
BCKFD_PROT_GATE   31D6<>
BRIGHT_PWM        22A1<> 39A7>
BRIGHT_PWM_UF     22A2<>
BT_USB_DM         14B1< 24B2<> 37B2> 39B6>
BT_USB_DP         14C1< 24B2<> 37B2> 39B6>
CAPSLOCK_LED      23A8<
CAPSLOCK_LED_L    23B8< 30C7<
CBUS_ADDR<0>      17B1<> 17B4>
CBUS_ADDR<1>      17B1<> 17B4>
CBUS_ADDR<2>      17B1<> 17B4>
CBUS_ADDR<3>      17B1<> 17B4>
CBUS_ADDR<4>      17B1<> 17B4>
CBUS_ADDR<5>      17B1<> 17B4>
CBUS_ADDR<6>      17B1<> 17B4>
CBUS_ADDR<7>      17B1<> 17B4>
CBUS_ADDR<8>      17B1<> 17B4>
CBUS_ADDR<9>      17B1<> 17B4>
CBUS_ADDR<10>     17B4> 17C1<>
CBUS_ADDR<11>     17B1<> 17B4>
CBUS_ADDR<12>     17B1<> 17B4>
CBUS_ADDR<13>     17B1<> 17B4>
CBUS_ADDR<14>     17B1<> 17B4>
CBUS_ADDR<15>     17B1<> 17B4>
CBUS_ADDR<16>     17B1<> 17B4<
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CBUS_ADDR<18>     17B2<> 17B4>
CBUS_ADDR<19>     17B2<> 17B4>
CBUS_ADDR<20>     17B2<> 17B4>
CBUS_ADDR<21>     17B2<> 17B4>
CBUS_ADDR<22>     17A4> 17B2<>
CBUS_ADDR<23>     17A4> 17B2<>
CBUS_ADDR<24>     17A4> 17B2<>
CBUS_ADDR<25>     17A4> 17B2<>
CBUS_ADDR_16_UF   17B5<>
CBUS_BVD1_L       17B2<> 17C4<
CBUS_BVD2_L       17B2<> 17C4<
CBUS_CE1_L        17C1<> 17C4>
CBUS_CE2_L        17B4> 17C2<>
CBUS_DATA<0>      17A1<> 17A4<>
CBUS_DATA<1>      17A1<> 17A4<>
CBUS_DATA<2>      17A1<> 17A4<>
CBUS_DATA<3>      17A4<> 17C1<>
CBUS_DATA<4>      17A4<> 17C1<>
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CBUS_DATA<11>     17A4<> 17C2<>
CBUS_DATA<12>     17A4<> 17C2<>
CBUS_DATA<13>     17A4<> 17C2<>
CBUS_DATA<14>     17A4<> 17C2<>
CBUS_DATA<15>     17A4<> 17C2<>
CBUS_DET_1_L      17C2<> 17C4< 39B8>
CBUS_DET_2_L      17A2<> 17C4< 39B8>
CBUS_INPACK_L     17B2<> 17B4<
CBUS_INT_L        14B5<> 14B7< 17A7<>
CBUS_IORD_L       17B2<> 17C4>
CBUS_IOWR_L       17B2<> 17C4>
CBUS_MFUNC1_PD    17A7< 17A7<>
CBUS_MFUNC2_PD    17A7< 17A7<>
CBUS_MFUNC3_PD    17A7< 17A7<>
CBUS_MFUNC4_PD    17A7< 17A7<>
CBUS_MFUNC5_PD    17A7< 17A7<>
CBUS_MFUNC6_PD    17A7< 17A7<
CBUS_OE_L         17C1<> 17C4>
CBUS_PCI_GNT_L    12D7<> 17A7<
CBUS_PCI_IDSEL    17B7<
CBUS_PCI_PERR_L   17B7<> 17D7<
CBUS_PCI_REQ_L    12A7< 12D7<> 17A7>
CBUS_PCI_RESET_L  17A7<
CBUS_PCI_SERR_L   17B7> 17D7<
CBUS_READY        17B1<> 17C4<
CBUS_REG_L        17B2<> 17C4>
CBUS_RESET_L      17B2<> 17C4>
CBUS_SUSPEND_PU   17A7< 17D7<
CBUS_VCCD0_L      17C4<>
CBUS_VCCD1_L      17C4<>
CBUS_VPPD0        17C4<>
CBUS_VPPD1        17C5<>
CBUS_VS1          17B2<> 17C4<>
CBUS_VS2          17B2<> 17C4<>
CBUS_WAIT_L       17B2<> 17B4<
CBUS_WE_L         17B1<> 17C4>
CBUS_WP_L         17A1<> 17B4<
CG_ADDRSEL        14B7<
CG_CLKOUT         14B6<>
CG_FSEL           14B7< 14C5<>
CG_LOCK           14B7<>

CG_RESET_L        14B7<
CHARGE_DISABLE    31A7<>
CHARGE_LED_L      30C6<> 30D7< 31D8<> 39D2>
CHGND1            38A6>
CHGND2            38A6>
CHGND3            38A6>
CHGND4            38A6> 39B6>
CHGND5            38A6>
CHGND6            38A6>
CLK10M_PMU_XIN    30B6<
CLK10M_PMU_XOUT   30B6<
CLK10M_PMU_XOUT_UF  30B7<
CLK18M_INT_EXT    14A6<> 36B1>
CLK18M_INT_XIN    14A5< 36B1>
CLK18M_INT_XOUT   14A5<> 36B1>
CLK18M_XTAL_IN    14A5< 36B1>
CLK25M_ENET_XIN   27A7< 36B1>
CLK25M_ENET_XOUT  27A7<> 36B1>
CLK25M_XTAL_IN    27A7<
CLK27M_GPU_XIN    36B1>
CLK27M_GPU_XOUT   36B1>
CLK27M_XTAL_IN    36B1>
CLK32K_PMU_XIN    30B3<>
CLK32K_PMU_XOUT   30B3<>
CLK32K_PMU_XOUT_UF  30B2<>
CLK33M_AIRPORT    12D8< 24D5<> 36C1> 39B1>
CLK33M_AIRPORT_UF  12C7<> 36C1>
CLK33M_CBUS       12D8< 17A7< 36C1>
CLK33M_CBUS_UF    12C7<> 36C1>
CLK33M_USB2       12C8< 26B7< 36C1>
CLK33M_USB2_UF    12C7<> 36C1>
CLK66M_AGP_15V_TP  12C4>
CLK66M_GPU_AGP    12C8< 18B7< 36C1>
CLK66M_GPU_AGP_UF  12C7<> 36C1>
CLKENET_LINK_GBE_REF  13C5< 27C8< 36B1>
CLKENET_LINK_GTX  13C5<> 36A1>
CLKENET_LINK_RX   13D5< 27C8< 36B1>
CLKENET_LINK_TX   13D5< 27D8< 36A1>
CLKENET_PHY_GBE_REF  27C7<> 36B1>
CLKENET_PHY_GTX   13C6< 27C7< 36A1>
CLKENET_PHY_RX    27C7<> 36B1>
CLKENET_PHY_TX    27D7<> 36B1>
CLKFW_LINK_LCLK   13C3<> 36A1>
CLKFW_LINK_PCLK   13C3<> 28C3< 36A1>
CLKFW_PHY_LCLK    13C2< 28B8< 36A1>
CLKFW_PHY_PCLK    28B4> 28C3< 36A1>
CLKLVDS_LN        19B5> 22A4<> 37C2> 39B7>
CLKLVDS_LP        19B5> 22A4<> 37C2> 39B7>
CLKLVDS_UN        19B5> 22A4<> 37C2> 39B7>
CLKLVDS_UP        19B5> 22A4<> 37C2> 39A7>
COMM_DTR_L        14C2> 25D1<> 39B2>
COMM_GPIO_L       14C2<> 25D2<> 39C2>
COMM_RESET_L      14C5<> 25C4<> 39C4>
COMM_RING_DET_L   14B5<> 14C7< 25C3<> 30C6<> 39C4>
COMM_RTS_L        14C2> 25D1<> 39B2>
COMM_RXD          14C2<> 25D1<> 39B2>
COMM_SHUTDOWN     14C5<> 25C4<> 39C4>
COMM_TRXC         14C2<> 25D2<> 39C2>
COMM_TXD_L        14C2<> 25D2<> 39C2>
COMP_DISABLE      22C2<>
COMP_ENABLE       22C1<>
COMP_RC           32C6<
CPU_AACK_L        5A7< 8B6<> 8C2< 36D5>
CPU_ADDR<0>       5C7<> 8D6<>
CPU_ADDR<0..31>   36D5>
CPU_ADDR<1>       5C7<> 8D6<>
CPU_ADDR<2>       5C7<> 8D6<>
CPU_ADDR<3>       5C7<> 8D6<>
CPU_ADDR<4>       5C7<> 8D6<>
CPU_ADDR<5>       5C7<> 8C6<>
CPU_ADDR<6>       5C7<> 8C6<>
CPU_ADDR<7>       5C7<> 8C6<>
CPU_ADDR<8>       5C7<> 8C6<>
CPU_ADDR<9>       5C7<> 8C6<>
CPU_ADDR<10>      5B7<> 8C6<>
CPU_ADDR<11>      5B7<> 8C6<>
CPU_ADDR<12>      5B7<> 8C6<>
CPU_ADDR<13>      5B7<> 8C6<>
CPU_ADDR<14>      5B7<> 8C6<>
CPU_ADDR<15>      5B7<> 8C6<>
CPU_ADDR<16>      5B7<> 8C6<>
CPU_ADDR<17>      5B7<> 8C6<>
CPU_ADDR<18>      5B7<> 8C6<>
CPU_ADDR<19>      5B7<> 8C6<>
CPU_ADDR<20>      5B7<> 8C6<>
CPU_ADDR<21>      5B7<> 8C6<>
CPU_ADDR<22>      5B7<> 8C6<>
CPU_ADDR<23>      5B7<> 8C6<>
CPU_ADDR<24>      5B7<> 8C6<>
CPU_ADDR<25>      5B7<> 8C6<>
CPU_ADDR<26>      5B7<> 8C6<>
CPU_ADDR<27>      5B7<> 8C6<>
CPU_ADDR<28>      5B7<> 8C6<>
CPU_ADDR<29>      5B7<> 8C6<>
CPU_ADDR<30>      5B7<> 8C6<>
CPU_ADDR<31>      5B7<> 8B6<>
CPU_ARTRY_L       5A7<> 8B6<> 8D2< 36D5>
CPU_AVDD          5C3< 38D3>
CPU_BG_L          5C7< 8C2< 8D6<> 36D5>
CPU_BR_L          5C7> 8D2< 8D6< 36D5>
CPU_BUS_VSEL      5C3< 7A6<
CPU_CHKSTP_OUT_L  5B3<> 5C2< 39D8>
CPU_CHKS_L        5A3< 5D2<
CPU_CI_L          5A7> 8B6<> 36D5>
CPU_CLKOUT_SPN    5C3>
CPU_CLK_EN        8A6<> 30C4<>
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CPU_DATA<0..31>   36D5>
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CPU_DATA<2>       6D8<> 8D4<>
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CPU_DATA<6>       6D8<> 8D4<>
CPU_DATA<7>       6D8<> 8D4<>
CPU_DATA<8>       6D8<> 8D4<>
CPU_DATA<9>       6C8<> 8D4<>
CPU_DATA<10>      6C8<> 8D4<>
CPU_DATA<11>      6C8<> 8D4<>
CPU_DATA<12>      6C8<> 8C4<>
CPU_DATA<13>      6C8<> 8C4<>
CPU_DATA<14>      6C8<> 8C4<>
CPU_DATA<15>      6C8<> 8C4<>
CPU_DATA<16>      6C8<> 8C4<>
CPU_DATA<17>      6C8<> 8C4<>
CPU_DATA<18>      6C8<> 8C4<>
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CPU_DATA<30>      6C8<> 8C4<>
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CPU_DATA<37>      6B8<> 8C4<> 8D8<
CPU_DATA<38>      6B8<> 8B4<> 8D8<
CPU_DATA<39>      6B8<> 8B4<> 8D8<
CPU_DATA<40>      6B8<> 8B4<> 8C8<
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CPU_DATA<49>      6B8<> 8A8< 8B4<>
CPU_DATA<50>      6B8<> 8A8< 8B4<>
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CPU_DATA<52>      6B8<> 8A8< 8B4<>
CPU_DATA<53>      6B8<> 8A8< 8B4<>
CPU_DATA<54>      6B8<> 8A8< 8B4<>
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CPU_DATA<57>      6B8<> 8B3< 8B4<>
CPU_DATA<58>      6B8<> 8B3< 8B4<>
CPU_DATA<59>      6B8<> 8B3< 8B4<>

CPU_DATA<60>      6B8<> 8B3< 8B4<>
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CPU_DATA<62>      6A8<> 8B3< 8B4<>
CPU_DATA<63>      6A8<> 8B3< 8B4<>
CPU_DBG_L         5C3< 8A4<> 8C2< 36D5>
CPU_DRDY_L        5C3> 8A4< 8C2< 36D5>
CPU_DRDY_L_UF     36D5>
CPU_DTI<0>        5C3< 8A4<>
CPU_DTI<0..2>     36D5>
CPU_DTI<1>        5C3< 8A4<>
CPU_DTI<2>        5C3< 8A4<>
CPU_EDTI          5B2< 5C3<
CPU_EMODE0_L      5A3< 7A4<
CPU_EMODE1_L      5A3< 5C2<
CPU_GBL_L         5A7<> 8B6< 36D5>
CPU_HIT_L         5A7> 8B6< 8D2< 36D5>
CPU_HRESET_INV    7A7<>
CPU_HRESET_L      5B3< 5C2< 7A5< 7A8< 23A2<> 39C8>
CPU_L1TSTCLK      5B2< 5B3<
CPU_L2TSTCLK      5B3< 5C2<
CPU_LSSD_MODE     5B3< 5C2<
CPU_MCP_L         5B3< 5D2<
CPU_M_DM          25A8< 25B6<
CPU_M_DP          25B6< 25B8<
CPU_PLL_CFG<0>    5C3< 7D3<
CPU_PLL_CFG<1>    5C3< 7D3<
CPU_PLL_CFG<2>    5C3< 7D3<
CPU_PLL_CFG<3>    5C3< 7D3<
CPU_PLL_CFG<4>    5C3< 7D3<>
CPU_PLL_CFGEXT    7D4<>
CPU_PLL_FS00      7C4<
CPU_PLL_FS01      7C4<
CPU_PLL_FS10      7C4<
CPU_PLL_STOP_BASE  7C7<
CPU_PLL_STOP_OC   7C4<> 7C8<> 30B6<>
CPU_PMONIN_L      5A3< 5C2<
CPU_PULLDOWN      5A2< 5A3< 5A3< 5C7<>
CPU_PULLUP        5A3< 5C2<
CPU_QACK_L        5B3> 8B6<> 36D5>
CPU_QREQ_L        5B3> 8B6< 8C2< 36D5>
CPU_SHD0_L        5A7<> 5D2<
CPU_SHD1_L        5A7<> 5D2<
CPU_SMI_L         5B3< 5C2< 30C4<>
CPU_SRESET_L      5B2< 5B3< 39C8>
CPU_SRWX_L        5A3< 5C2<
CPU_TA_L          5B3< 8A4<> 8D2< 36D5>
CPU_TBEN          5B3< 5D2< 8A6<>
CPU_TBST_L        5A7> 8B6<> 36D5>
CPU_TEA_L         5B3< 8A4< 8C2< 36D5>
CPU_TSIZ<0>       5A7> 8B6<>
CPU_TSIZ<0..2>    36D5>
CPU_TSIZ<1>       5A7> 8B6<>
CPU_TSIZ<2>       5A7> 8B6<>
CPU_TS_L          5C7<> 8D2< 8D6<> 36D5>
CPU_TT<0>         5A7<> 8B6<>
CPU_TT<0..4>      36C5>
CPU_TT<1>         5A7<> 8B6<>
CPU_TT<2>         5A7<> 8B6<>
CPU_TT<3>         5A7<> 8B6<>
CPU_TT<4>         5A7<> 8B6<>
CPU_VCORE_HI_OC   7B8< 30D4<> 34C8< 34D7<
CPU_VCORE_PWR_SEQ  34D8<>
CPU_VCORE_SEQ     34D8<
CPU_VCORE_SEQ_L   34D8<
CPU_VCORE_SLEEP   5C2< 5D8<> 34C1< 34D2< 38D3> 39B2>

CPU_VCORE_SLEEP_F  34C2<>
CPU_VCORE_SNUB    34B3<
CPU_WT_L          5A7> 8B6<> 36C5>
CSLOT_ADDR3_SPN   13B7>
CSLOT_ADDR4_SPN   13B7>
CSLOT_ADDR5_SPN   13B7>
CSLOT_ADDR6_SPN   13B7>
CSLOT_ADDR7_SPN   13B7>
CSLOT_ADDR8_SPN   13B7>
CSLOT_ADDR9_SPN   13B7>
CSLOT_CE1_L_SPN   13C7>
CSLOT_CE2_L_SPN   13C7>
CSLOT_IORD_L_SPN  13C7>
CSLOT_IOWAIT_L_PU  13C7<
CSLOT_IOWR_L_SPN  13C7>
CSLOT_OE_L_SPN    13C7>
CSLOT_WE_L_SPN    13C7>
CURRENT_THRESHOLD  31C4<
CY25811_S0        18B2<
CY25811_S1        18B2<
DCDC_EN           19A7<> 29C7<> 32B7<> 33B6<> 34C8<>
                39C1>
DCDC_EN_L         33B6<> 33B7<> 35C7<>
DDC_CLK_ISO       22D4<>
DDR_VREF          11D1< 11D3<> 11D5<> 11D6<> 11D8<>
                38D3>
DVI_DDC_CLK       22D4<>
DVI_DDC_CLK_UF    22C5<> 22D3<> 39C7>
DVI_DDC_DATA      22C4<>
DVI_DDC_DATA_UF   22C5<> 39C7>
DVI_HPD           22C4<>
DVI_HPD_DIV       22C3<
DVI_HPD_UF        22C3< 22C5<> 39C7>
DVI_TRUN_ON_ILIM  22D2<
DVI_TURN_ON       22D3<>
DVI_TURN_ON_BASE  22D2<
EEPROM_ADDR       23D4<
EEPROM_WP_PD      23D3<>
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EIDE_ADDR<2..0>   37B5>
EIDE_ADDR<1>      13B7> 24B8<
EIDE_ADDR<2>      13B7> 24B8<
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EIDE_CS1_L        13B7> 24B8< 37B5>
EIDE_DATA<0>      13C7<> 24C8<
EIDE_DATA<15..0>  37B5>
EIDE_DATA<1>      13C7<> 24C8<
EIDE_DATA<2>      13C7<> 24C8<
EIDE_DATA<3>      13C7<> 24C8<
EIDE_DATA<4>      13C7<> 24C8<
EIDE_DATA<5>      13B7<> 24B8<
EIDE_DATA<6>      13B7<> 24C8<
EIDE_DATA<7>      13B7<> 24C8<
EIDE_DATA<8>      13B7<> 24D8<
EIDE_DATA<9>      13B7<> 24D8<
EIDE_DATA<10>     13B7<> 24D8<
EIDE_DATA<11>     13B7<> 24D8<
EIDE_DATA<12>     13B7<> 24D8<
EIDE_DATA<13>     13B7<> 24D8<
EIDE_DATA<14>     13B7<> 24C8<
EIDE_DATA<15>     13B7<> 24C8<
EIDE_DMACK_L      13A7<> 24A8< 37B5>
EIDE_DMARQ        13A7< 24B8< 37B5>
EIDE_INT          13A7< 24A8< 37B5>
EIDE_IOCHRDY      13B7< 24A8< 37B5>
EIDE_OPTICAL_ADDR<0>  24A5<> 24B7< 39A4>
EIDE_OPTICAL_ADDR<2..0>  37B5>
EIDE_OPTICAL_ADDR<1>  24A5<> 24B7< 39A4>
EIDE_OPTICAL_ADDR<2>  24A6<> 24B7< 39A4>
EIDE_OPTICAL_CS0_L  24A5<> 24B7< 37B5> 39D4>
EIDE_OPTICAL_CS1_L  24A6<> 24B7< 37B5> 39D4>
EIDE_OPTICAL_DATA<0>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<15..0>  37B5>
EIDE_OPTICAL_DATA<1>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<2>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<3>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<4>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<5>  24A5<> 24B7< 39C4>
EIDE_OPTICAL_DATA<6>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<7>  24A5<> 24C7< 39B4>
EIDE_OPTICAL_DATA<8>  24A6<> 24D7< 39B4>
EIDE_OPTICAL_DATA<9>  24A6<> 24D7< 39B4>
EIDE_OPTICAL_DATA<10>  24A6<> 24D7< 39B4>
EIDE_OPTICAL_DATA<11>  24A6<> 24D7< 39B4>
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EIDE_OPTICAL_DATA<13>  24A6<> 24C7< 39B4>
EIDE_OPTICAL_DATA<14>  24A6<> 24C7< 39B4>
EIDE_OPTICAL_DATA<15>  24A6<> 24C7< 39B4>
EIDE_OPTICAL_DMAACK_L  24A6<> 24A7< 37A5> 39A4>
EIDE_OPTICAL_DMA_RQ  24A6<> 24B7< 37A5> 39A4>
EIDE_OPTICAL_INT  24A5<> 24A7< 37A5> 39D4>
EIDE_OPTICAL_IOCHRDY  24A5<> 24A7< 37A5> 39D4>
EIDE_OPTICAL_RD_L  24A6<> 24A7< 37B5> 39A4>
EIDE_OPTICAL_RST_L  24A7< 24B5<> 37A5> 39D4>
EIDE_OPTICAL_WR_L  24A5<> 24A7< 37A5> 39D4>
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EIDE_RST_L        13B7> 24A8< 37B5>
EIDE_WR_L         13A7> 24A8< 37B5>
ENET_COL          13C5< 27B7< 37A5>
ENET_COMA         27B7<>
ENET_CRS          13C5< 27B7> 37A5>
ENET_CTAP_CHGND   27A1< 38A6>

ENET_ENERGY_DET   14B5<> 27B7<>
ENET_HSDACM       27A7<>
ENET_HSDACP       27A7<>
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ENET_LINK_RXD<7..0>  37A5>
ENET_LINK_RXD<1>  13C5< 27C7>
ENET_LINK_RXD<2>  13C5< 27C7>
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ENET_LINK_TXD<7..0>  37A5>
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ENET_LINK_TXD<6>  13A4< 13D5>
ENET_LINK_TXD<7>  13A4< 13D5>
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ENET_LINK_TX_ER   13D5<> 37A5>
ENET_MDC          13C5> 27B7< 37A5>
ENET_MDIO         13C5<> 27B7<> 37A5>
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ENET_PHY_TXD<7..0>  37A5>
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ENET_PHY_TXD<6>   13A5> 27C7<
ENET_PHY_TXD<7>   13A5> 27C7<
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ENET_PHY_TX_ER    13D6> 27C7< 37A5>
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ENET_RST_L        27B7<
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ENET_RX_ER        13C5< 27B7> 37A5>
ENET_VSSC         27A7<>
EXT_SWING         20A5<>
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FANL_PWM          25A3<> 25B2<> 39B3>
FANL_TACH         25A3<> 25B2<> 39B3>
FANR_GND          25B2<> 38B6> 39B3>
FANR_PWM          25A2<> 25B1<> 39B3>
FANR_TACH         25B2< 25B2<>
FB_4_85V_BU       32A5<
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FP_PWR_EN_L       22B3<>
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FWB_TPB1          28A4<
FWPLL_BYP         28C8<>
FW_BIAS0          28A5<>
FW_BIAS1          28A5<>
FW_BMODE          28B7<
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FW_LINK_DATA<7..0>  37A5>
FW_LINK_DATA<1>   13D3<> 28B8<
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FW_LINK_DATA<7>   13C3<> 28A8<
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FW_LKON           13C3<> 28B5<>
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FW_OSC_EN         28A3<
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FW_PC_PU          28B7<
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FW_PHY_CNTL<1..0>  37A5>
FW_PHY_CNTL<1>    28B4<> 28C3<
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FW_PHY_DATA<7..0>  37A5>
FW_PHY_DATA<1>    28B8<>
FW_PHY_DATA<2>    28B8<>
FW_PHY_DATA<3>    28A8<>
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FW_PHY_DATA<7>    28A8<>
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FW_PHY_LREQ       13C2< 28B8< 37A5>
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FW_PHY_RESET_L    28A8<
FW_PINT           13C3<> 28B4> 37A5>
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FW_PORT1_SEL      28B6<
FW_PWREN_L        29C6<>
FW_PWR_GATE       29D6<>
FW_R0             28A5<>
FW_R1             28A5<>
FW_TESTM          28A7<
FW_TPA0N          28B1<> 29C4<> 37D2>
FW_TPA0N_CONN     29C3<>
FW_TPA0P          28B1<> 29C4<> 37D2>
FW_TPA0P_CONN     29C3<>
FW_TPA1N          28B1<> 29A4<> 37C2>
FW_TPA1P          28B1<> 29A4<> 37C2>
FW_TPB0N          28B1<> 29C4<> 37D2>
FW_TPB0N_CONN     29C3<>
FW_TPB0P          28B1<> 29C4<> 37D2>
FW_TPB0P_CONN     29C3<>
FW_TPB1N          28B1<> 29A4<> 37C2>
FW_TPB1P          28B1<> 29A4<> 37C2>
FW_TPB2_PD        28A5<>
FW_TPI0N          37C2>
FW_TPI0P          37C2>
FW_TPI1N          29A3<> 37C2> 39D2>
FW_TPI1P          29A3<> 37C2> 39D2>
FW_TPO0N          37C2>
FW_TPO0P          37C2>
FW_TPO0R          29C2<> 38A3> 39A3>
FW_TPO1N          29A3<> 37C2> 39D2>
FW_TPO1P          29A3<> 37C2> 39D2>
FW_VGND0          29C2<> 38A3>
FW_VGND1          29A3<> 38A3>
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FW_XI             28A5<> 36A1>
GAIN_SETTING2     23C7<>
GPU_AGP_TEST      18D6<
GPU_AUXWIN        19C5<>
GPU_B             19D6<> 22D8<
GPU_C             19D6<> 22A8<
GPU_CLK27M_OUT    36C1>
GPU_CLK27M_UF     36C1>
GPU_COMP          19D6<> 22A8<
GPU_CORE_OK       19A6<> 19D4<> 21D2<> 21D7<>
GPU_DVI_DDC_CLK   19C5<> 22D3<>
GPU_DVI_DDC_DATA  19C5<> 22C3<>
GPU_DVOD<0>       19D7<> 20B7<
GPU_DVOD<0..11>   37D5>
GPU_DVOD<1>       19D7<> 20B7<
GPU_DVOD<2>       19D7<> 20B7<
GPU_DVOD<3>       19D7<> 20B7<
GPU_DVOD<4>       19D7<> 20B7<
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GPU_DVOD<6>       19D7<> 20A7<
GPU_DVOD<7>       19D7<> 20A7<
GPU_DVOD<8>       19D7<> 20A7<
GPU_DVOD<9>       19D7<> 20A7<
GPU_DVOD<10>      19D7<> 20A7<
GPU_DVOD<11>      19D7<> 20A7<
GPU_DVOD_DE       19C7<> 20A7<
GPU_DVO_CLKP      19C7<> 20A7< 36B1>
GPU_DVO_HSYNC     19C7<> 20A7< 37C5>
GPU_DVO_VSYNC     19C7<> 20A7< 37C5>
GPU_FBCLK0        36B1>
GPU_FBCLK0_L      36B1>
GPU_FBCLK1        36B1>
GPU_FBCLK1_L      36B1>
GPU_G             19D6<> 22D8<
GPU_HPD           19C5<> 22C3<>
GPU_MEM_IO        38C3>
GPU_MEM_IO_FLT    21C2< 38C3>
GPU_R             19D6<> 22D8<
GPU_SSCLK_IN      36B1>

GPU_SSCLK_UF      36C1>
GPU_THERM_DM      18A6<>
GPU_THERM_DP      18A6<>
GPU_TV_GND1       22B8<> 38B6>
GPU_TV_GND2       22A8<> 38B6>
GPU_VCORE         18A6<> 19A3<> 19B5<> 19D4< 38C3>
                39B2>
GPU_VCORE_CNTL    19A3<>
GPU_VCORE_CNTL_L  19A4<> 19B7<>
GPU_VCORE_NECK    19B5<> 38B3>
GPU_VCORE_PWR_SEQ  19A8<>
GPU_VCORE_SEQ     19A8<
GPU_VCORE_SEQ_L   19A8<
GPU_VCORE_SW      19A4<> 38B1>
GPU_VCORE_VDDCI   18A5<> 38C3>
GPU_Y             19D6<> 22B8<
HD_ADDR<0>        24C2<> 24C3<
HD_ADDR<2..0>     37C5>
HD_ADDR<1>        24C2<> 24C3<
HD_ADDR<2>        24B3<> 24C1<>
HD_CS0_L          24C2<> 24C3< 37B5>
HD_CS1_L          24B3<> 24C1<> 37B5>
HD_DATA<0>        24C2<> 24D3<
HD_DATA<15..0>    37C5>
HD_DATA<1>        24C2<> 24D3<
HD_DATA<2>        24D2<> 24D3<
HD_DATA<3>        24D2<> 24D3<
HD_DATA<4>        24C3< 24D2<>
HD_DATA<5>        24C3< 24D2<>
HD_DATA<6>        24C3< 24D2<>
HD_DATA<7>        24C3< 24D2<>
HD_DATA<8>        24C3< 24D1<>
HD_DATA<9>        24C3< 24D1<>
HD_DATA<10>       24C3< 24D1<>
HD_DATA<11>       24D1<> 24D3<
HD_DATA<12>       24B3< 24D1<>
HD_DATA<13>       24B3< 24D1<>
HD_DATA<14>       24C1<> 24C3<
HD_DATA<15>       24B3< 24C1<>
HD_DIOR_L         24A3< 24C2<> 37B5>
HD_DIOW_L         24A3< 24C1<> 37B5>
HD_DMACK_L        24A3< 24C2<> 37B5>
HD_DMARQ          13C6< 24C2<> 37B5>
HD_INTRQ          13C6< 24C1<> 37B5>
HD_IOCHRDY        24A3< 24C1<> 37B5>
HD_RESET_L        24A3< 24D2<> 37B5>
HIGH_VCORE        19A2<>
HIGH_VCORE_DIV    19A3<
HPD_4V_REF        22C3<
HPD_BASE          22C1<
HPD_ON            22C2<>
HPD_ON_RC         22C2<
HPD_PWR_SNS_EN    19C7<> 22C3<>
HPD_PWR_SW        22C2<>
IAC_FB            31D4<
IAC_RC_COMP       31D4<
INTREPID_ACS_REF  8A6<
INT_AGPPVT        12D4<>
INT_AGP_FB_IN     12C4< 36C1>
INT_AGP_FB_OUT    12C4<> 36C1>
INT_AGP_VREF      12B4< 12D4<> 18D5< 38D3>
INT_AUDIO_TO_SND  14B2< 25D8<> 39C6>
INT_AUDIO_TO_SND_F  25D7<> 25D7<
INT_CPUFB_IN      8A6< 8B6< 36D1>
INT_CPUFB_IN_NORM  8A4< 36D1>
INT_CPUFB_LONG    8A4< 36D1>
INT_CPUFB_OUT     8A6<> 8A6< 36D1>
INT_CPUFB_OUT_NORM  8A4< 36D1>
INT_CPUFB_OUT_SHORT  8A5< 36D1>
INT_DDRCLK2_N_TP  9B6<>
INT_DDRCLK2_P_TP  9B6<>
INT_DDRCLK5_N_TP  9B6<>
INT_DDRCLK5_P_TP  9B6<>
INT_ENET_RST_L    14B5<> 27B8<
INT_EXTINT3_PU    14B5<> 14B7<
INT_EXTINT8_PU    14B5<> 14C7<
INT_EXTINT10_PU   14A7< 14B5<>
INT_EXTINT11_PU   14A7< 14B5<>
INT_EXTINT12_PU   14A7< 14B5<>
INT_EXTINT13_PU   14B5<> 14B7<
INT_EXTINT14_PU   14B5<> 14C7<
INT_EXTINT16_PU   14B5<> 14B7<
INT_GPIO1_PU      14C5<> 14C7< 34C8<
INT_GPIO9_PU      14A7< 14B5<>
INT_GPIO12_PU     14B5<> 14B7<
INT_GPIO15_PU     14B5<> 14C7<
INT_I2C_CLK0      11A3<> 11A8<> 13C2< 13C3<> 23D2<
                23D4<> 39B8>
INT_I2C_CLK1      13C2< 13C3<> 14B7< 25B4<> 39B8>
INT_I2C_CLK2      14A2<> 25C4<> 25D7<> 39C6>
INT_I2C_DATA0     11A3<> 11A8<> 13C2< 13C3<> 23D2<>
                23D4<> 39B8>
INT_I2C_DATA1     13B2< 13C3<> 14B7< 25B4<> 39B8>
INT_I2C_DATA2     14A2<> 25C4<> 25C7<> 39C6>
INT_JTAG_TEI      13C2< 13C5<
INT_MEM_REF_H     9B6< 38D3>
INT_MEM_VREF      9A7< 9B6<> 38D3>
INT_MOD_BITCLK_UF  14A3<> 14A7<
INT_MOD_CLKOUT_UF  14A3<> 14B7<
INT_MOD_DTI       14A2< 25C3<> 39B1>
INT_MOD_DTI_UF    14A7<
INT_MOD_DTO_UF    14A3<> 14B7<
INT_MOD_SYNC_UF   14A3<> 14A7<
INT_PCI_FB_IN     12C7< 36C1>
INT_PCI_FB_OUT    12C7<> 36C1>
INT_PEND_PROC_INT  14A5<> 30C4<>
INT_PROC_SLEEP_REQ_L  14A5< 30B4<>
INT_PU_RESET_L    13D3< 25D4<> 30A2< 30C4<>
INT_REF_CLK_IN    14A5< 14B5< 36C1>
INT_REF_CLK_OUT   14A5> 14B7< 36C1>
INT_RESET_L       9B3< 13D3< 30C7< 30D4<>
INT_ROM_CS_L      12A6< 12C7>
INT_ROM_OE_L      12A6< 12C7>
INT_ROM_RW_L      12A6< 12C7>
INT_SND_CLKOUT    14A3<>
INT_SND_SCLK      14A3<>
INT_SND_SYNC      14B3<>
INT_SND_TO_AUDIO  14B3<>
INT_SUSPEND_ACK_L  8B6< 30B6<>
INT_SUSPEND_REQ_L  8B6< 30B6<> 30C7<
INT_TST_MONIN_PD  13C2< 13C5<
INT_TST_MONOUT_TP  13C5>
INT_TST_PLLEN_PD  13C5< 13D2<
INT_WATCHDOG_L    14A5> 30C6<>
INV_ON_PWM        19C6<> 22A3<
IO_RESET_L        17A7< 23D6< 26B8< 27B8< 30C6<>
                30D7<
JTAG_ASIC_TCK     13C5< 13D2< 27A5< 39D8>
JTAG_ASIC_TDI     13C5< 13D2< 39D8>
JTAG_ASIC_TDO_TP  27A5> 39D8>
JTAG_ASIC_TMS     13C5< 13D2< 27A5< 39D8>
JTAG_ASIC_TRST_L  13C2< 13C5< 27A5< 39D8>
JTAG_CPU_TCK      5B2< 5B3< 23B2> 39C8>
JTAG_CPU_TDI      5B2< 5C3< 23D4> 39C8>
JTAG_CPU_TDO_TP   5C3> 39C8>
JTAG_CPU_TMS      5B2< 5B3< 23C4> 39C8>
JTAG_CPU_TRST_L   5A3< 5B3< 23D4<> 39B1> 39C8>
JTAG_ENET_TDI     13C5> 13D2< 27A5<
KBD_CAPSLOCK_LED  23A7<> 39B4>
KBD_COMMAND_L     23A5< 23A7<> 30C6<> 39B4>
KBD_CONTROL_L     23A5< 23A7<> 30A8< 30C6<> 39B4>
KBD_FUNCTION_L    23A5< 23A7<> 30B6<> 39B4>
KBD_ID            23A7<> 23B5< 30B6<> 39C4>
KBD_LED1_OUT      23A5<> 23A7<> 38B6> 39C2>
KBD_LED2_OUT      23A5<> 23A7<> 38B6> 39C2>
KBD_LED_EN        23A5<>
KBD_LED_SET       23A5<
KBD_NUMLOCK_LED   23B7<> 39C3>
KBD_OPTION_L      23A5< 23B7<> 30A8< 30B6<> 39B4>
KBD_SHIFT_L       23A5< 23B7<> 30A8< 30C6<> 39B4>
KBD_X<0>          23A5< 23B7<> 30C6<> 39B4>
KBD_X<1>          23A5< 23B7<> 30C6<> 39B4>
KBD_X<2>          23B5< 23B7<> 30C6<> 39B4>
KBD_X<3>          23B5< 23B7<> 30C6<> 39A4>
KBD_X<4>          23B5< 23B7<> 30C6<> 39A4>
KBD_X<5>          23B5< 23B7<> 30C6<> 39A4>
KBD_X<6>          23B5< 23B7<> 30C6<> 39A4>
KBD_X<7>          23B5< 23B7<> 30C6<> 39A4>
KBD_X<8>          23B5< 23B7<> 30C6<> 39A4>
KBD_X<9>          23B5< 23B7<> 30C6<> 39D3>
KBD_Y<0>          23B7<> 30D6<> 39D3>
KBD_Y<1>          23B7<> 30D6<> 39D3>
KBD_Y<2>          23B7<> 30D6<> 39D3>
KBD_Y<3>          23B7<> 30D6<> 39D3>
KBD_Y<4>          23B7<> 30D6<> 39D3>
KBD_Y<5>          23B7<> 30D6<> 39D3>
KBD_Y<6>          23B7<> 30C6<> 39C3>
KBD_Y<7>          23B7<> 30C6<> 39C3>

LCD_DIGON_L       22A6<
LCD_PWREN_L       22A5<>
LED_LINK10        27B5<>
LED_LINK100       27B5<>
LED_RX_SPN        27B5>
LEFT_USB_DM       24B2<> 26B3< 37A2> 39D1>
LEFT_USB_DP       24B2<> 26A3< 37A2> 39D1>
LID_CLOSED_L      23A7<> 39C4>
LM2594_IN         28D8<> 38B3>
LT1962_INT_ADJ    14D6<
LT1962_INT_BYP    14D6<>
LTC1625_ITH       31D3<>
LTC1962_1V5_VIN   38A1>
LTC1962_1V5_VOUT  38A1>
LTC1962_INT_VIN   14D7<> 38A1>
LTC1962_L3_VIN    38A1>
LTC1962_L3_VOUT   38A1>
LTC3405_SW        27D4<> 38B3>
LTC3411_GND       38A1>
LTC3411_ITH       38A1>
LTC3411_ITH_RC    38A1>
LTC3411_SHDN      38A1>
LTC3411_SYNC      38A1>
LTC3411_VCC       38B1>
LTC3412_GND       35A6<>
LTC3412_ITH       35A6<>
LTC3412_ITH_RC    35A6<
LTC3412_PGOOD     35A4<>
LTC3412_RT        35A6<
LTC3412_RUNSS     35A6<>
LTC3412_SYNC      35A6<>
LTC3412_VFB       35A6<>
LTC3412_VFB_DIV   35A6<
LTC3707_START_RC  33B6<>
LVDS_DDC_CLK      19C5<> 22B5<> 39A7>
LVDS_DDC_DATA     19C5<> 22B5<> 39A7>
LVDS_L0N          19B5> 22B4<> 37C2> 39C7>
LVDS_L0P          19B5> 22B4<> 37C2> 39C7>
LVDS_L1N          19B5> 22B4<> 37C2> 39C7>
LVDS_L1P          19B5> 22B4<> 37C2> 39C7>
LVDS_L2N          19B5> 22B4<> 37C2> 39C7>
LVDS_L2P          19B5> 22B4<> 37C2> 39C7>
LVDS_L3N_TP       19B5>
LVDS_L3P_TP       19B5>
LVDS_U0N          19C5> 22A4<> 37C2> 39B7>
LVDS_U0P          19C5> 22A4<> 37C2> 39B7>
LVDS_U1N          19C5> 22A4<> 37C2> 39B7>
LVDS_U1P          19C5> 22A4<> 37C2> 39B7>
LVDS_U2N          19B5> 22A4<> 37B2> 39B7>
LVDS_U2P          19B5> 22A4<> 37B2> 39B7>
LVDS_U3N_TP       19B5>
LVDS_U3P_TP       19B5>
MAIN_RESET_L      14C7< 17A7< 17D5< 18C8< 20B8<
                24D6<> 26B8< 30D4<> 30D7< 39C1>
MAX1715_FB2       35B1< 35B4<
MAX1715_GND       35B5<> 35C5< 38C1>
MAX1715_ON_RC     35C7<>
MAX1715_REF       35B5<> 38C1>
MAX1715_SKIP      35C4< 38C1>
MAX1715_TON       35C5< 38C1>
MAX1715_VCC       35D5< 38C1>
MAX1717_AB_SEL    34A7< 34C6<
MAX4172_OUT       31D4<>
MAXBUS_SLEEP      5A2< 5D1< 5D5< 7B7< 7D8< 8B8< 8C3<
                8C8< 8D1< 8D8< 15D8< 16D8< 23B3<
                23B3< 34D8< 38D3>
MDI0_PD           27B4<
MDI1_PD           27B4<
MDI2_PD           27B4<
MDI3_PD           27B3<
MDI_M<0>          27B5<> 37D2>
MDI_M<1>          27B5<> 37D2>
MDI_M<2>          27B5<> 37D2>
MDI_M<3>          27B5<> 37D2>
MDI_P<0>          27B5<> 37D2>
MDI_P<1>          27B5<> 37D2>
MDI_P<2>          27B5<> 37D2>
MDI_P<3>          27B5<> 37D2>
MEM_ADDR<0>       9B5< 9D6<>
MEM_ADDR<12..0>   36A5>
MEM_ADDR<1>       9B5< 9D6<>
MEM_ADDR<2>       9B5< 9D6<>
MEM_ADDR<3>       9B5< 9D6<>
MEM_ADDR<4>       9B5< 9D6<>
MEM_ADDR<5>       9B5< 9D6<>
MEM_ADDR<6>       9B5< 9D6<>
MEM_ADDR<7>       9B5< 9D6<>
MEM_ADDR<8>       9B5< 9D6<>
MEM_ADDR<9>       9A5< 9D6<>
MEM_ADDR<10>      9A5< 9D6<>
MEM_ADDR<11>      9A5< 9D6<>
MEM_ADDR<12>      9A5< 9D6<>
MEM_BA<0>         9A5< 9D6<>
MEM_BA<1..0>      36A5>
MEM_BA<1>         9A5< 9C6<>
MEM_CAS_L         9A5< 9C6<> 36A5>
MEM_CKE<0>        9B6<> 9C5<
MEM_CKE<3..0>     36A5>
MEM_CKE<1>        9B6<> 9C5<
MEM_CKE<2>        9B6<> 9C5<
MEM_CKE<3>        9B6<> 9C5<
MEM_CS_L<0>       9C5< 9C6<>
MEM_CS_L<3..0>    36A5>
MEM_CS_L<1>       9C5< 9C6<>
MEM_CS_L<2>       9C5< 9C6<>
MEM_CS_L<3>       9C5< 9C6<>
MEM_DATA<0>       9D8<> 10C7<>
MEM_DATA<7..0>    36C5>
MEM_DATA<1>       9D8<> 10C7<>
MEM_DATA<2>       9D8<> 10C7<>
MEM_DATA<3>       9D8<> 10C7<>
MEM_DATA<4>       9D8<> 10C7<>
MEM_DATA<5>       9D8<> 10C7<>
MEM_DATA<6>       9D8<> 10C7<>
MEM_DATA<7>       9D8<> 10C7<>
MEM_DATA<8>       9D8<> 10C7<>
MEM_DATA<15..8>   36C5>
MEM_DATA<9>       9D8<> 10C7<>
MEM_DATA<10>      9D8<> 10C7<>
MEM_DATA<11>      9D8<> 10C7<>
MEM_DATA<12>      9D8<> 10B7<>
MEM_DATA<13>      9C8<> 10B7<>
MEM_DATA<14>      9C8<> 10B7<>
MEM_DATA<15>      9C8<> 10B7<>
MEM_DATA<16>      9C8<> 10C5<>
MEM_DATA<31..16>  36C5>
MEM_DATA<17>      9C8<> 10C5<>
MEM_DATA<18>      9C8<> 10C5<>
MEM_DATA<19>      9C8<> 10C5<>
MEM_DATA<20>      9C8<> 10C5<>
MEM_DATA<21>      9C8<> 10C5<>
MEM_DATA<22>      9C8<> 10C5<>
MEM_DATA<23>      9C8<> 10C5<>
MEM_DATA<24>      9C8<> 10C5<>
MEM_DATA<25>      9C8<> 10C5<>
MEM_DATA<26>      9C8<> 10C5<>
MEM_DATA<27>      9C8<> 10C5<>
MEM_DATA<28>      9C8<> 10C5<>
MEM_DATA<29>      9C8<> 10B5<>
MEM_DATA<30>      9C8<> 10B5<>
MEM_DATA<31>      9C8<> 10B5<>
MEM_DATA<32>      9C8<> 10C3<>
MEM_DATA<47..32>  36B5>
MEM_DATA<33>      9C8<> 10C3<>
MEM_DATA<34>      9C8<> 10C3<>
MEM_DATA<35>      9C8<> 10C3<>
MEM_DATA<36>      9C8<> 10C3<>
MEM_DATA<37>      9C8<> 10C3<>
MEM_DATA<38>      9C8<> 10C3<>
MEM_DATA<39>      9B8<> 10C3<>
MEM_DATA<40>      9B8<> 10C3<>
MEM_DATA<41>      9B8<> 10C3<>
MEM_DATA<42>      9B8<> 10C3<>
MEM_DATA<43>      9B8<> 10C3<>
MEM_DATA<44>      9B8<> 10C3<>
MEM_DATA<45>      9B8<> 10B3<>
MEM_DATA<46>      9B8<> 10B3<>
MEM_DATA<47>      9B8<> 10B3<>
MEM_DATA<48>      9B8<> 10C1<>
MEM_DATA<55..48>  36B5>
MEM_DATA<49>      9B8<> 10C1<>
MEM_DATA<50>      9B8<> 10C1<>
MEM_DATA<51>      9B8<> 10C1<>
MEM_DATA<52>      9B8<> 10C1<>
MEM_DATA<53>      9B8<> 10C1<>
MEM_DATA<54>      9B8<> 10C1<>
MEM_DATA<55>      9B8<> 10C1<>
MEM_DATA<56>      9B8<> 10C1<>

MEM_DATA<63..56>  36A5>
MEM_DATA<57>      9B8<> 10C1<>
MEM_DATA<58>      9B8<> 10C1<>
MEM_DATA<59>      9B8<> 10C1<>
MEM_DATA<60>      9B8<> 10C1<>
MEM_DATA<61>      9B8<> 10B1<>
MEM_DATA<62>      9B8<> 10B1<>
MEM_DATA<63>      9B8<> 10B1<>
MEM_DQM<0>        9C6<> 10C7<> 36C5>
MEM_DQM<1>        9C6<> 10B7<> 36C5>
MEM_DQM<2>        9C6<> 10C5<>
MEM_DQM<3..2>     36B5>
MEM_DQM<3>        9C6<> 10B5<>
MEM_DQM<4>        9C6<> 10C3<>
MEM_DQM<5..4>     36B5>
MEM_DQM<5>        9C6<> 10B3<>
MEM_DQM<6>        9C6<> 10C1<> 36B5>
MEM_DQM<7>        9C6<> 10B1<> 36A5>
MEM_DQS<0>        9C6<> 10C7<> 36C5>
MEM_DQS<1>        9C6<> 10B7<> 36C5>
MEM_DQS<2>        9C6<> 10C5<>
MEM_DQS<3..2>     36B5>
MEM_DQS<3>        9C6<> 10B5<>
MEM_DQS<4>        9C6<> 10C3<>
MEM_DQS<5..4>     36B5>
MEM_DQS<5>        9C6<> 10B3<>
MEM_DQS<6>        9C6<> 10C1<> 36B5>
MEM_DQS<7>        9C6<> 10B1<> 36A5>
MEM_MUXSEL_H<0>   9B6<> 10A6<
MEM_MUXSEL_H<1..0>  36A5>
MEM_MUXSEL_H<1>   9B6<> 10A4<
MEM_MUXSEL_L<0>   9B6<> 10A6<
MEM_MUXSEL_L<1..0>  36A5>
MEM_MUXSEL_L<1>   9B6<> 10A4<
MEM_RAS_L         9A5< 9C6<> 36A5>
MEM_WE_L          9A5< 9C6<> 36A5>
MLB_ALS_GAIN_SW   23C4<> 23C8<>
MLB_ALS_OP_COMP   23D7<
MLB_ALS_OP_IN     23D7<
MLB_ALS_OUT       23C4<> 23D6<
MLB_ALS_OUT_FB    23D7<>
MLB_PHOTODIODE    23D8<>
MODEM_USB_DM      14B1< 25C3<> 37A2> 39B6>
MODEM_USB_DP      14B1< 25C3<> 37A2> 39B6>
MOD_BITCLK        14A2< 25C3<> 39B1>
MOD_CLKOUT        14A2< 25C4<> 39A1>
MOD_DTO           14A2< 25C4<> 39A1>
MOD_SYNC          14A2< 25C3<> 39A1>
MPIC_CPU_INT_L    5B2< 5B3< 14B5>
NEC_AMC_TP        26A5<
NEC_AVDD          26D6< 38A3>
NEC_AVSS_F        26A5< 26B4<
NEC_CRUN_L        26A7<>
NEC_IDSEL         26B7<
NEC_IO_RESET_L    26B7< 26B7<
NEC_LEFT_USB_OVERCURRENT  24B2<> 26C1< 39D1>
NEC_LEFT_USB_PWREN  24B2<> 26B5<> 39D1>
NEC_LEGC          26A7<
NEC_MAIN_RESET_L  26A7< 26B7<
NEC_NANDTESTEN_TP  26A5<
NEC_NANDTESTOUT_TP  26A4<>
NEC_NC1_TP        26B5<>
NEC_NC2_TP        26B5<>
NEC_OCI<1>        26B5< 26C3<
NEC_OCI<2>        26B5< 26C3<
NEC_OCI<3>        26B5<
NEC_OCI<4>        26B5<
NEC_OCI<5>        26B5<
NEC_PCI_INTA_L    26A7< 26B7>
NEC_PCI_INTB_L    26A7< 26B7>
NEC_PCI_INTC_L    26A7< 26B7>
NEC_PCI_PERR_L    26B7<> 26C8<
NEC_PCI_SERR_L    26B7> 26C8<
NEC_PME_L         26A7> 26B7<
NEC_PPON3_TP      26B5>
NEC_PPON4_TP      26B5>
NEC_PPON5_TP      26B5>
NEC_RIGHT_USB_OVERCURRENT  26C1< 32A7<> 39C1>
NEC_RIGHT_USB_PWREN  26B5<> 32A7<> 39C1>
NEC_RREF          26B5<>
NEC_SMI_L_TP      26A7>
NEC_USB_DAM       26B4< 26C3<> 37B2>
NEC_USB_DAP       26A4< 26C3<> 37B2>
NEC_USB_DBM       26A4< 26C3<> 37B2>
NEC_USB_DBP       26A4< 26C3<> 37B2>
NEC_USB_RSDM1     26C5<> 37B2>
NEC_USB_RSDM2     26C5<> 37B2>
NEC_USB_RSDP1     26C5<> 37B2>
NEC_USB_RSDP2     26C5<> 37B2>
NEC_XT1           26D5< 36B1>
NEC_XT2           26D5<> 36B1>
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NTEST1_TP         26B5<
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PMU_BATT0_DET_L  30B4<>
PMU_BATT1_DET_L_PU  30B4<> 30D2<
PMU_BATT_DET_L   30B3< 30D2< 31A4<> 39C3>
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PMU_CHARGE_V     30C4<> 31B8<>
PMU_CHRG_BATT_S  30C4<> 31A8<>
PMU_CLK          14C2<> 30C4<>
PMU_CNVSS        30B6< 30C7<>
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PMU_FROM_INT     14C2<> 30C4<>
PMU_I2C_CLK      30B4<> 30C2<
PMU_I2C_DATA     30B4<> 30C2<
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PMU_INT_NMI      148S<> 148T< 30D4<>
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PMU_NMI_BUTTON_L  25C1< 30C2< 30C4<>
PMU_NMI_L        30C2< 30C4<>
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PMU_PME_L        148S<> 268K< 30B2< 30C4<>
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PMU_POWER_UP_L   29C7<> 30C6<> 30D7< 33B8<
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PMU_SLEEP_LED_L  23C2<> 30C4<>
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POWER_UP         29C7<>
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RAM_ADDR<7>      9B4< 11B3<> 11B8<>
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RAM_WE_L         9A4< 11B3<> 11B8<> 36A5>
RF_DISABLE_L_SPN  24D6<> 39C1>
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RIGHT_USB_DP     26A3< 32A7<> 37A2> 39D1>
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ROM_ONBOARD_CS_L  9B3< 24C6<> 39B1>
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ST7_ICP_SEL_PD   23A2< 23D6<
ST7_KBD_LED_OUT  23A4< 23C4<>
ST7_OSC1         23D5<
ST7_OSC2         23D5<>
ST7_PB6_PD       23B2< 23C4<>
ST7_RESET_L      23D5<>
ST7_SENSOR4_SCK_PD  23B2< 23D4<>
ST7_SENSOR4_SDA_PD  23B2< 23D4<>
ST7_SENSOR5_SCK_PU  23B2< 23D4<>
ST7_SENSOR5_SDA_PU  23B2< 23D4<>
ST7_SLEEP_LED_H  23C2<> 23C4<>
ST7_XTAL_IN      23C5<
STOP_AGP_L       12D2< 12D4<>
SUPPLY_M_DM      25B6< 25B8<
SUPPLY_M_DP      25B6< 25B8<
SUTRO_ALS_GAIN_SW  23C4<> 24B2<> 39C2>
SUTRO_ALS_OUT    23C4<> 24B2<> 39C2>
SYSCLK_CPU       5C3> 8A6< 36D1>
SYSCLK_CPU_UF    8A6<> 36D1>
SYSCLK_DDRCLK_A0  9D4< 11D8<> 36D1>
SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 36D1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 36D1>
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SYSCLK_DDRCLK_A1_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A1_UF  9B6<> 9D5< 36D1>
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SYSCLK_DDRCLK_B0_L  9C4< 11D3<> 36C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 36D1>
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THERM1_DP        25A5< 25B5< 25B5<> 37A2>
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THERM1_M_DP      37A2>
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THERM2_DP        25A5< 25B5< 25B5<> 37A2>
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THERM2_M_DP      37A2>
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THERM_L_OC       25A4<> 30B4<>
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TMDS_CLKP        20B3< 20C2< 20C3< 22C7<> 37B2>
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TMDS_CONN_CLKP   22C6<> 22C7<> 37B2> 39D7>
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TMDS_CONN_DN<2>  22B6<> 22D5<>
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                 39A8>
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TPAD_F_TXD       23A7<> 39C4>
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TV_Y             22A6<> 39D6>
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UIDE_INTRQ       13C7< 37C5>
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USB2_PCI_GNT_L   12C7<> 26B7<
USB2_PCI_INT_L   148S<> 14C7< 26A8<
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USB_OC_EF_L      14B2< 14D7<
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VCORE_GNDDIV_TEST  34A3<>
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VCORE_GNDSNS_TEST  34A3<>
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VCORE_TON        34B6< 38C1>
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VCORE_VID2       39A3>
VCORE_VID3       39A3>
VCORE_VID4       39A3>
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VGA_G            22C5<> 22D7< 39D7>
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VGA_HSYNC_BUF    22C8<>
VGA_R            22C5<> 22D7< 39D7>
VGA_VSYNC        22C5<> 22C7< 39D7>
VGA_VSYNC_BUF    22C8<>
ZV_LCDDATA20_PU  19C7<>
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APPLE COMPUTER INC.

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*** Part Cross-Reference for the entire design ***

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RP38	RPAK4P	28
RP39	RPAK10P2C	17
RP40	RPAK4P	30
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RP43	RPAK10P2C	23
RP44	RPAK4P	25
RP45	RPAK4P	26
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RP51	RPAK4P	14
RP52	RPAK4P	23 26
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RP61	RPAK2P	20
SH1	SHLD_3P_EMI	4
SP1	SPKR_CLIP_P84	4
SP2	SPKR_CLIP_P84	4
SP3	SPKR_CLIP_P84	4
SP4	SPKR_CLIP_P84	4
SP5	SPKR_CLIP_P84	4
SP6	SPKR_CLIP_P84	4
T1	XFR_ENET_1000BT	27
U1	SN74AUC1G04	7

U2	SN74AUC1G08	23
U3	ADT7460	25
U4	SN74AUC1G08	23
U5	SIL1162	20
U7	VREG_LT1962	14
U9	CBTV4020	10
U10	CBTV4020	10
U11	PI3B3257	34
U12	CBTV4020	10
U13	CBTV4020	10
U14	LTC3405	27
U15	COMPARATOR_LMC7211	31
U16	LTC1778	19
U17	FEPR_1MX8	9
U18	LTC1625	32
U19	PWR_CNTRL_TPS2211	17
U20	MAX1717	34
U21	COMPARATOR_LMC7211	32
U22	MAX1715	35
U23	AMP_MAX4172	31
U24	7432	22 30
U25	VREG_LP2951	32
U26	PCI1510GGU	17
U27	COMPARATOR_LMC7211	30
U28	LTC3707	33
U29	TSB81BA3A	28
U30	VREG_LP2951	32
U31	MAX1772	31
U32	EEPROM_16KX8_M2412BB	23
U33	M16C62	30
U34	VREG_LM2594	28
U35	MAX1915	23
U36	LTC1761	28
U37	VREG_LT1962	28
U38	COMPARATOR_LMC7211	31
U39	UPD720101_FBGA	26
U40	OPAMP_MAX4236EUT	23
U42	CLK_GEN_CY28512	14
U43	APOLLO_MPC7445_360	5 6
U44	RAGE_MBLTY_M10_CSP64_667	18 19 21
U45	INTREPID	8 9 12 13 14 15
U46	COMPARATOR_LMC7211	22
U47	CLK_GEN_CY25811	18
U49	TRANSCEIVER_88E1111	27
U50	OPAMP_LMC7111	31
U51	MAX6804	30
U52	FEPR_256KX8_ST72264_BGA	23
U54	VREG_MM1571J	21
U55	VREG_MM1571J	21
U56	741G32	22
U57	741G32	22
U58	LTC3412	35
XW1	SHORT	35
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XW5	SHORT	34
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XW7	SHORT	34
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XW9	SHORT	25
XW11	JUMPER	35
XW12	SHORT	22
XW13	SHORT	22
XW15	SHORT	34
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XW29	SHORT	21
XW30	SHORT	21
XW31	SHORT	5
Y1	CRYSTAL	14
Y3	CRYSTAL	27
Y4	CRYSTAL	23
Y5	CRYSTAL	26
Y6	CRYSTAL	30
Y7	CRYSTAL_4PIN	30
ZT1	HOLE_VIA	4
ZT2	MTGHOLE	4
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ZT79	HOLE_VIA	4
ZT80	HOLE_VIA	4
ZT81	HOLE_VIA	4
ZT82	HOLE_VIA	4
ZT83	MTGHOLE	4