CR=1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
01		?	?	?	?

820-1173-01
TANGENT EVT
07/26/00

TABLE OF CONTENTS

DIMENSIONS ARE IN MILLIMETERS
XX :
X.XX :
X.XXX :
ANGLES :
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL, FINISH NOTED AS APPLICABLE | SIZE D

Apple Computer Inc.

TITLE
SCHEMATIC, MLB, P21

DRAWING NUMBER 051-0997 | REV. 01

SHT 1 OF 47

MAXBUS LOGIC LEVELS ARE EITHER 1.8V OR 2.5V

J29
SM
F10X30
(1 OF 2)

5 3 A<0>	K2	MAX_A0	MAX_D0	G23	D<0> 3 5
MSB 5 3 A<1>	C7	MAX_A1	MAX_D1	K28	D<1> 3 5
5 3 A<2>	K8	MAX_A2	MAX_D2	K26	D<2> 3 5
5 3 A<3>	B8	MAX_A3	MAX_D3	G21	D<3> 3 5
5 3 A<4>	J5	MAX_A4	MAX_D4	J29	D<4> 3 5
5 3 A<5>	B12	MAX_A5	MAX_D5	H26	D<5> 3 5
5 3 A<6>	K4	MAX_A6	MAX_D6	J25	D<6> 3 5
5 3 A<7>	E9	MAX_A7	MAX_D7	K14	D<7> 3 5
5 3 A<8>	J7	MAX_A8	MAX_D8	J15	D<8> 3 5
5 3 A<9>	H10	MAX_A9	MAX_D9	G17	D<9> 3 5
5 3 A<10>	K6	MAX_A10	MAX_D10	E29	D<10> 3 5
5 3 A<11>	D12	MAX_A11	MAX_D11	H18	D<11> 3 5
5 3 A<12>	F10	MAX_A12	MAX_D12	H30	D<12> 3 5
5 3 A<13>	B14	MAX_A13	MAX_D13	G19	D<13> 3 5
5 3 A<14>	C9	MAX_A14	MAX_D14	C29	D<14> 3 5
5 3 A<15>	C15	MAX_A15	MAX_D15	F30	D<15> 3 5
5 3 A<16>	F12	MAX_A16	MAX_D16	E27	D<16> 3 5
5 3 A<17>	E15	MAX_A17	MAX_D17	G25	D<17> 3 5
5 3 A<18>	E11	MAX_A18	MAX_D18	H28	D<18> 3 5
5 3 A<19>	E13	MAX_A19	MAX_D19	F26	D<19> 3 5
5 3 A<20>	G9	MAX_A20	MAX_D20	F28	D<20> 3 5
5 3 A<21>	B10	MAX_A21	MAX_D21	F24	D<21> 3 5
5 3 A<22>	C11	MAX_A22	MAX_D22	E25	D<22> 3 5
5 3 A<23>	D10	MAX_A23	MAX_D23	D30	D<23> 3 5
5 3 A<24>	H12	MAX_A24	MAX_D24	D26	D<24> 3 5
5 3 A<25>	D18	MAX_A25	MAX_D25	C27	D<25> 3 5
5 3 A<26>	D14	MAX_A26	MAX_D26	F22	D<26> 3 5
5 3 A<27>	C13	MAX_A27	MAX_D27	D28	D<27> 3 5
5 3 A<28>	G11	MAX_A28	MAX_D28	E23	D<28> 3 5
5 3 A<29>	D16	MAX_A29	MAX_D29	C25	D<29> 3 5
5 3 A<30>	B16	MAX_A30	MAX_D30	E21	D<30> 3 5
5 3 A<31> LSB	B18	MAX_A31	MAX_D31	F20	D<31> 3 5
			MAX_D32	F16	D<32> 3 5
			MAX_D33	D20	D<33> 3 5
			MAX_D34	E17	D<34> 3 5
			MAX_D35	F18	D<35> 3 5
			MAX_D36	E19	D<36> 3 5
			MAX_D37	G13	D<37> 3 5
			MAX_D38	B22	D<38> 3 5
			MAX_D39	G15	D<39> 3 5
			MAX_D40	C21	D<40> 3 5
			MAX_D41	H20	D<41> 3 5
			MAX_D42	H16	D<42> 3 5
			MAX_D43	J23	D<43> 3 5
			MAX_D44	H22	D<44> 3 5
			MAX_D45	J17	D<45> 3 5
			MAX_D46	J21	D<46> 3 5
			MAX_D47	K22	D<47> 3 5
			MAX_D48	K20	D<48> 3 5
			MAX_D49	J27	D<49> 3 5
			MAX_D50	G29	D<50> 3 5
			MAX_D51	J19	D<51> 3 5
			MAX_D52	K24	D<52> 3 5
			MAX_D53	H24	D<53> 3 5
			MAX_D54	G27	D<54> 3 5
			MAX_D55	A19	D<55> 3 5
			MAX_D56	B20	D<56> 3 5
			MAX_D57	B24	D<57> 3 5
			MAX_D58	A21	D<58> 3 5
			MAX_D59	A17	D<59> 3 5
			MAX_D60	C19	D<60> 3 5
			MAX_D61	D24	D<61> 3 5
			MAX_D62	D22	D<62> 3 5
			MAX_D63	C23	D<63> 3 5 LS BIT

16 SYSCLK_PROCA	K10	SYSCLK0	
16 SYSCLK_PROCB	K16	SYSCLK1	
16 SYSCLK_ANLYZR	A25	SYSCLK2	
5 3 AACK*	C17	MAX_AACK	
35 5 3 ARTRY*	H14	MAX_ARTRY	
3 BG<0>*	A11	MAX_BG0	
3 BG<1>*	H8	MAX_BG1	
35 3 BR<0>*	G7	MAX_BR0	
35 3 BR<1>*	B26	MAX_BR1	
5 3 CI*	C5	MAX_CI	
4 CKSTP_OUT*	D2	MAX_CKSTPOUT	
3 DBG<0>*	A15	MAX_DBG0	
3 DBG<1>*	J9	MAX_DBG1	
35 3 DRDY<0>*	K12	MAX_DRDY0	
35 3 DRDY<1>*	K18	MAX_DRDY1	
5 3 DTI<0> MSB	A5	MAX_DTI0	
5 3 DTI<1>	F14	MAX_DTI1	
5 3 DTI<2> LSB	A9	MAX_DTI2	
5 3 GBL*	B6	MAX_GBL	
35 3 HIT<0>*	D6	MAX_HIT0	
35 3 HIT<1>*	B28	MAX_HIT1	
36 4 CPU_HRESET*	B4	MAX_HRESET	
35 27 CPU_INT<0>*	E1	MAX_INT0	
35 27 CPU_INT<1>*	B29	MAX_INT1	
35 27 PM_CNT_EN*	A8	MAX_PMONIN	
5 3 QACK*	A6	MAX_QACK	
3 QREQ<0>*	A12	MAX_QREQ0	
3 QREQ<1>*	A27	MAX_QREQ1	
36 35 SMI<0>*	C2	MAX_SMI0	
36 35 SMI<1>*	B30	MAX_SMI1	
27 4 SRESET<0>*	C1	MAX_SRESET0	
27 4 SRESET<1>*	A30	MAX_SRESET1	
35 5 3 TA*	A7	MAX_TA	
35 27 TIMEBASE_EN	A10	MAX_TBEN	
5 3 TBST*	F4	MAX_TBST	
35 5 3 TEA*	A13	MAX_TEA	
35 5 3 TS*	J13	MAX_TS	
5 3 TSIZ<0>	D4	MAX_TSIZ0	
5 3 TSIZ<1>	E3	MAX_TSIZ1	
5 3 TSIZ<2>	F6	MAX_TSIZ2	
5 3 TT<0>	E5	MAX_TT0	
5 3 TT<1>	F8	MAX_TT1	
5 3 TT<2>	H6	MAX_TT2	
5 3 TT<3>	G5	MAX_TT3	
5 3 TT<4>	J11	MAX_TT4	
5 3 WT*	D8	MAX_WT	
	E7	VGER_EDTI	
	H4	VGER_HPR0	
	A23	VGER_IARTRY1	
	J1	VGER_INT2	
	E30	VGER_INT3	
36 35 SMI<2>*	K1	VGER_SMI2	
36 35 SMI<3>*	G30	VGER_SMI3	
27 4 SRESET<2>*	H1	VGER_SRESET2	
27 4 SRESET<3>*	C30	VGER_SRESET3	
	G3	VGER_WAIT	

ESP_TCK	H2	CPU_TCK	4
ESP_TDI	F1	CPU_TDI	4
ESP_TDO	J3	CPU_TDO	4
ESP_TMS	F2	CPU_TMS	4
ESP_TRST	G2	CPU_TRST*	4
IIC_SCL	K29	UNI_IIC_CLK	7 8 19 35
IIC_SDA	J30	UNI_IIC_DAT	7 8 19 35
STOP_PLL0	A2	CPU0_PLL_STOP	36
STOP_PLL1	A4	CPU1_PLL_STOP	36
TOPINSERTED	B2	TOPINSERTED	
BOTTOMINSERTED	K30	TOPINSERTED AND BOTTOMINSERTED SHORTED ON PROC MODULE	
1.8V_2.5V_SEL	A3	2.5V_1.8V*	3 35
MAINCLK_FS0	A1	MAINCLK_FS0	16
MAINCLK_FS1	C3	MAINCLK_FS1	16
MAINCLK_FS2	B3	MAINCLK_FS2	16
THERMISTER	A29		

1_8V_TO_PROC 37

MAXBUS_IO_RAIL
(FROM PROCESSOR MODULE)
2 3 4 10 19 35

J29
SM
F10X30
(2 OF 2)

	C4		
	E6		
	G4	1_8VDD	
	J2		
	J6		
	A22		
	A24		
	A26		
	A28		
	C22		
	C24		
	C26		
	C28		
	A14	3_3VDD	
	A16		
	A18		
	A20		
	C16		
	C18		
	C20		
	J22		
	J24		
	J26		
	J28		
	E22		
	E24		
	E26		
	E28		
	C8		
	C10		
	C12		
	C14		
	G24		
	G26		
	G28		
	E8		
	E10		
	E12	5_0VDD	
	E14		
	E16		
	E18		
	E20		
	G8		
	G10		
	G12		
	G14		
	G16		
	G18		
	G20		
	G22		
	J8		
	J10		
	J12		
	J14		
	J16		
	J18		
	J20		

OVDD	C6		
	E2		
	E4	MIN_LINE_WIDTH=25	
	G6		
	J4		
	B5		
	B7		
	B9		
	B11		
	B13		
	B15		
	B17		
	B19		
	B21		
	B23		
	B25		
	B27		
	D5		
	D7		
	D9		
	D11		
	D13		
	D15		
	D17		
	D19		
	D21		
	D23		
	D25		
	D27		
	D29		
GND	F3		
	F5		
	F7		
	F9		
	F11		
	F13		
	F15		
	F17		
	F19		
	F21		
	F23		
	F25		
	F27		
	F29		
	H3		
	H5		
	H7		
	H9		
	H11		
	H13		
	H15		
	H17		
	H19		
	H21		
	H23		
	H25		
	H27		
	H29		
	K3		
	K5		
	K7		
	K9		
	K11		
	K13		
	K15		
	K17		
	K19		
	K21		
	K23		
	K25		
	K27		
	D3		

+3.3V
PLACE NEAR PROC CONNECTOR
C203 150UF 20% 6.3V TANT SMD POSCAP

+5V
PLACE NEAR PROC CONNECTOR
C192 150UF 20% 6.3V TANT SMD POSCAP

+12V
B1 12VDC
39 FAN_PWR D1 12V_FAN
39 FAN_GND G1 GND_FAN

3_3V_TRICKLE
22 36 37 39
R13 1K 5% 1/16W MF 603
ADDRESS = 6 (AC/AD)

R12 0 5% 1/16W MF 402
NO STUFF
STUFF TO ALLOW SYSTEM TO BE POWERED UP WITHOUT PROC MODULE INSTALLED
36 POWERUP_OR

MIN_LINE_WIDTH=25
OVDD
225 UF, 440 MOHM CALCULATED
C401 150UF 20% 6.3V TANT SMD POSCAP

MAXBUS_IO_RAIL
2 3 4 10 19 35
C402 0.01UF 20% 50V CERM 402
C403 0.01UF 20% 50V CERM 402
C387 0.01UF 20% 50V CERM 402
C386 0.01UF 20% 50V CERM 402
SPACE OUT EVENLY ALONG CONNECTOR
FOR IMAGE CURRENT RETURN PATH

AREA BETWEEN CONNECTOR AND UNI-N HAS THREE GROUND PLANES AND MAXBUS_IO_RAIL

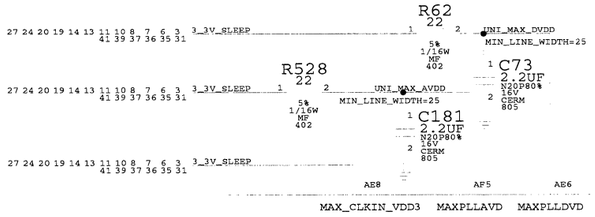
ZH10
1
235R156
MLB MOUNTING SCREW

ZH11
1
315R197
PROC MOUNTING HOLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
462-4102	3	SCREW, M3.5X0.6X4.0MM	X1,X2,X3	---
805-2312	3	5.6MM,2X SCREW STANDOFF	X4,X5,X6	---

PROCESSOR MODULE CONNECTOR

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-0997	REV. 01
	SCALE NONE	SHT 2 OF 47	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343T0453	1	IC,ASIC,UNI-N,REV1.5X,P21,343S0343	U28	

UNI-N 1.5 IS #343S0343

MAXBUS LOGIC LEVELS ARE EITHER 1.8V OR 2.5V

PROVIDE EASY PROBE ACCESS TO BR/BG

MAXBUS PADS HAVE BUS KEEPERS,
NO PULLUPS NEEDED

16	SYSCLK_UNI	AH2	MAXCLK
35 2	BR<0>*	AJ13	BR_0
2	BG<0>*	AF17	BG_0
35 2	BR<1>*	AF14	BR_1
2	BG<1>*	AF15	BG_1
35 5 2	TS*	AD15	TS
5 2	A<0>	AK4	A_0
5 2	A<1>	AH4	A_1
5 2	A<2>	AH3	A_2
5 2	A<3>	AF6	A_3
5 2	A<4>	AH5	A_4
5 2	A<5>	AJ2	A_5
5 2	A<6>	AJ4	A_6
5 2	A<7>	AJ3	A_7
5 2	A<8>	AD9	A_8
5 2	A<9>	AK3	A_9
5 2	A<10>	AH10	A_10
5 2	A<11>	AJ8	A_11
5 2	A<12>	AH9	A_12
5 2	A<13>	AE9	A_13
5 2	A<14>	AH7	A_14
5 2	A<15>	AE10	A_15
5 2	A<16>	AK8	A_16
5 2	A<17>	AE11	A_17
5 2	A<18>	AJ7	A_18
5 2	A<19>	AH8	A_19
5 2	A<20>	AJ9	A_20
5 2	A<21>	AF8	A_21
5 2	A<22>	AJ6	A_22
5 2	A<23>	AD11	A_23
5 2	A<24>	AF11	A_24
5 2	A<25>	AF9	A_25
5 2	A<26>	AH6	A_26
5 2	A<27>	AF7	A_27
5 2	A<28>	AF10	A_28
5 2	A<29>	AJ5	A_29
5 2	A<30>	AD10	A_30
5 2	A<31>	AK5	A_31
5 2	CI*	AE16	CI
5 2	GBL*	AJ14	GBL
5 2	TBST*	AK9	TBST
5 2	TSIZ<0>	AJ10	TSIZ_0
5 2	TSIZ<1>	AK10	TSIZ_1
5 2	TSIZ<2>	AF12	TSIZ_2
5 2	TT<0>	AE12	TT_0
5 2	TT<1>	AF13	TT_1
5 2	TT<2>	AJ11	TT_2
5 2	TT<3>	AE13	TT_3
5 2	TT<4>	AH11	TT_4
5 2	WT*	AJ16	WT
5 2	AACK*	AK14	AACK
35 5 2	ARTRY*	AJ12	ARTRY
35 2	HIT<0>*	AK13	HIT_0
35 2	HIT<1>*	AH12	HIT_1
2	QREQ<0>*	AH14	QREQ_0
2	QREQ<1>*	AE15	QREQ_1
5 2	QACK*	AF16	QACK
36	UNI_SUSPEND_REQ*	AB29	SUSPENDREQ
36	UNI_SUSPEND_ACK*	Y26	SUSPENDACK

U28
UNI-N-1.5
(1 OF 5)
PBGA-UNIN-1.5

MAXBUS
INTERFACE

D_0	AJ28	D<0>	2 5
D_1	AB25	D<1>	2 5
D_2	AE28	D<2>	2 5
D_3	AH28	D<3>	2 5
D_4	AH30	D<4>	2 5
D_5	AC24	D<5>	2 5
D_6	AD25	D<6>	2 5
D_7	AH21	D<7>	2 5
D_8	AJ21	D<8>	2 5
D_9	AJ23	D<9>	2 5
D_10	AG29	D<10>	2 5
D_11	AE21	D<11>	2 5
D_12	AE29	D<12>	2 5
D_13	AF23	D<13>	2 5
D_14	AH29	D<14>	2 5
D_15	AE26	D<15>	2 5
D_16	AE25	D<16>	2 5
D_17	AC25	D<17>	2 5
D_18	AJ30	D<18>	2 5
D_19	AH25	D<19>	2 5
D_20	AH27	D<20>	2 5
D_21	AH23	D<21>	2 5
D_22	AH26	D<22>	2 5
D_23	AD22	D<23>	2 5
D_24	AD21	D<24>	2 5
D_25	AF25	D<25>	2 5
D_26	AJ25	D<26>	2 5
D_27	AJ27	D<27>	2 5
D_28	AE22	D<28>	2 5
D_29	AK27	D<29>	2 5
D_30	AJ29	D<30>	2 5
D_31	AF21	D<31>	2 5
D_32	AF18	D<32>	2 5
D_33	AH20	D<33>	2 5
D_34	AH22	D<34>	2 5
D_35	AF20	D<35>	2 5
D_36	AJ24	D<36>	2 5
D_37	AH19	D<37>	2 5
D_38	AD19	D<38>	2 5
D_39	AK21	D<39>	2 5
D_40	AE20	D<40>	2 5
D_41	AK23	D<41>	2 5
D_42	AK22	D<42>	2 5
D_43	AF24	D<43>	2 5
D_44	AK26	D<44>	2 5
D_45	AJ22	D<45>	2 5
D_46	AJ26	D<46>	2 5
D_47	AG28	D<47>	2 5
D_48	AF26	D<48>	2 5
D_49	AF29	D<49>	2 5
D_50	AB24	D<50>	2 5
D_51	AF22	D<51>	2 5
D_52	AD26	D<52>	2 5
D_53	AK28	D<53>	2 5
D_54	AF28	D<54>	2 5
D_55	AK18	D<55>	2 5
D_56	AE19	D<56>	2 5
D_57	AJ19	D<57>	2 5
D_58	AJ18	D<58>	2 5
D_59	AH17	D<59>	2 5
D_60	AH18	D<60>	2 5
D_61	AH24	D<61>	2 5
D_62	AF19	D<62>	2 5
D_63	AJ20	D<63>	2 5
DBG_0	AJ15	DBG<0>*	2
DBG_1	AD16	DBG<1>*	2
DRDY_0	AH13	DRDY<0>*	2 35
DRDY_1	AE14	DRDY<1>*	2 35
DTI_0	AH15	DTI<0>	2 5
DTI_1	AK17	DTI<1>	2 5
DTI_2	AH16	DTI<2>	2 5
TA	AE18	TA*	2 5 35
TEA	AE17	TEA*	2 5 35

35 2 2.5V_1.8V* AJ17 MAXREF
HIGH = 2.5V, LOW = 1.8V MAXBUS I/O RAIL

UNI_AB6 R7 SPARE1

R237
49.9
1%
1/16W
MF
603
35 19 10 4 2 MAXBUS_IO_RAIL

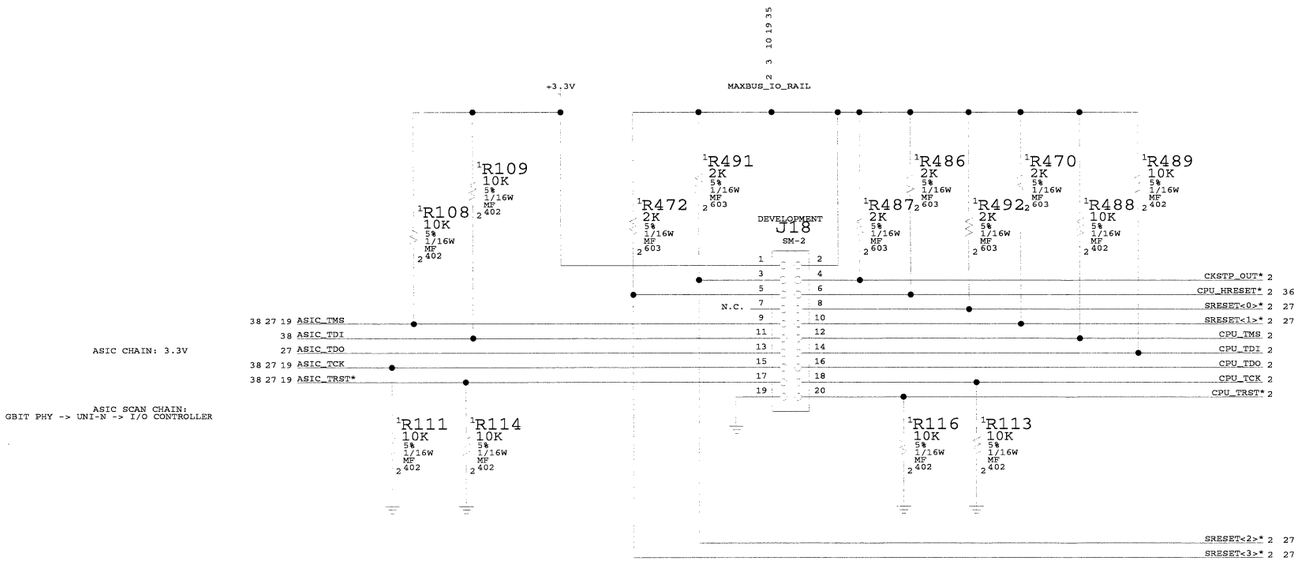
MAXPLLAVS
AE7

MAXBUS INTERFACE (UNI-N/1)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-0997 | REV. 01

SCALE NONE | SHT 3 OF 47



ASIC CHAIN: 3.3V

ASIC SCAN CHAIN:
GBIT PHY -> UNI-N -> I/O CONTROLLER

PROCESSOR CHAIN: 1.8/2.5V

NEW CONNECTOR: 511S0018 CON_F20SM-KX
OLD CONNECTOR: 515-1387 CON_M20ST_100P

ESP INTERFACE

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-0997	01
	SCALE	SHT OF	
	NONE	4 47	

CR-5

AACK*	DELAY_RULE=J29.C17:U28.AK14:450P:530P	2 3	
ARTRY*	DELAY_RULE=J29.H14:U28.AJ12:415P:495P	2 3	35
CI*	DELAY_RULE=J29.C5:U28.AE16:525P:605P	2 3	
GBL*	DELAY_RULE=J29.B6:U28.AJ14:500P:580P	2 3	
QACK*	DELAY_RULE=J29.A6:U28.AF16:500P:580P	2 3	
TA*	DELAY_RULE=J29.A7:U28.AE18:480P:560P	2 3	35
TBST*	DELAY_RULE=J29.F4:U28.AK9:435P:515P	2 3	
TEA*	DELAY_RULE=J29.A13:U28.AE17:485P:565P	2 3	35
TS*	DELAY_RULE=J29.J13:U28.AD15:400P:480P	2 3	35
WT*	DELAY_RULE=J29.D8:U28.AJ16:360P:440P	2 3	
A<0>	DELAY_RULE=J29.K2:U28.AK4:415P:495P	2 3	
A<1>	DELAY_RULE=J29.C7:U28.AH4:380P:460P	2 3	
A<10>	DELAY_RULE=J29.K6:U28.AH10:370P:450P	2 3	
A<11>	DELAY_RULE=J29.D12:U28.AJ8:420P:500P	2 3	
A<12>	DELAY_RULE=J29.F10:U28.AH9:365P:445P	2 3	
A<13>	DELAY_RULE=J29.B14:U28.AR9:430P:510P	2 3	
A<14>	DELAY_RULE=J29.C9:U28.AH7:520P:600P	2 3	
A<15>	DELAY_RULE=J29.C15:U28.AE10:480P:560P	2 3	
A<16>	DELAY_RULE=J29.F12:U28.AK8:515P:595P	2 3	
A<17>	DELAY_RULE=J29.E15:U28.AE11:315P:395P	2 3	
A<18>	DELAY_RULE=J29.E11:U28.AJ7:465P:545P	2 3	
A<19>	DELAY_RULE=J29.E13:U28.AH8:465P:545P	2 3	
A<2>	DELAY_RULE=J29.K8:U28.AH3:425P:505P	2 3	
A<20>	DELAY_RULE=J29.G9:U28.AJ9:325P:405P	2 3	
A<21>	DELAY_RULE=J29.B10:U28.AF8:405P:485P	2 3	
A<22>	DELAY_RULE=J29.C11:U28.AJ6:405P:485P	2 3	
A<23>	DELAY_RULE=J29.D10:U28.AD11:470P:550P	2 3	
A<24>	DELAY_RULE=J29.H12:U28.AF11:400P:480P	2 3	
A<25>	DELAY_RULE=J29.D18:U28.AF9:380P:460P	2 3	
A<26>	DELAY_RULE=J29.D14:U28.AH6:500P:580P	2 3	
A<27>	DELAY_RULE=J29.C13:U28.AF7:435P:515P	2 3	
A<28>	DELAY_RULE=J29.G11:U28.AF10:520P:600P	2 3	
A<29>	DELAY_RULE=J29.D16:U28.AJ5:475P:555P	2 3	
A<3>	DELAY_RULE=J29.B8:U28.AF6:485P:565P	2 3	
A<30>	DELAY_RULE=J29.B16:U28.AD10:465P:545P	2 3	
A<31>	DELAY_RULE=J29.B18:U28.AK5:375P:455P	2 3	
A<4>	DELAY_RULE=J29.J5:U28.AH5:390P:470P	2 3	
A<5>	DELAY_RULE=J29.B12:U28.AJ2:450P:530P	2 3	
A<6>	DELAY_RULE=J29.K4:U28.AJ4:390P:470P	2 3	
A<7>	DELAY_RULE=J29.E9:U28.AJ3:390P:470P	2 3	
A<8>	DELAY_RULE=J29.J7:U28.AD9:425P:505P	2 3	
A<9>	DELAY_RULE=J29.H10:U28.AK3:400P:480P	2 3	
D<0>	DELAY_RULE=J29.G23:U28.AJ28:355P:435P	2 3	
D<1>	DELAY_RULE=J29.K28:U28.AB25:375P:455P	2 3	
D<10>	DELAY_RULE=J29.E29:U28.AG29:350P:430P	2 3	
D<11>	DELAY_RULE=J29.H18:U28.AE21:350P:430P	2 3	
D<12>	DELAY_RULE=J29.H30:U28.AE29:335P:415P	2 3	
D<13>	DELAY_RULE=J29.G19:U28.AF23:305P:385P	2 3	
D<14>	DELAY_RULE=J29.C29:U28.AH29:350P:430P	2 3	
D<15>	DELAY_RULE=J29.F30:U28.AE26:310P:390P	2 3	
D<16>	DELAY_RULE=J29.E27:U28.AE25:350P:430P	2 3	
D<17>	DELAY_RULE=J29.G25:U28.AC25:330P:410P	2 3	
D<18>	DELAY_RULE=J29.H28:U28.AJ30:375P:455P	2 3	
D<19>	DELAY_RULE=J29.F26:U28.AH25:375P:455P	2 3	
D<2>	DELAY_RULE=J29.K26:U28.AE28:285P:365P	2 3	
D<20>	DELAY_RULE=J29.F28:U28.AH27:350P:430P	2 3	
D<21>	DELAY_RULE=J29.F24:U28.AH23:360P:440P	2 3	
D<22>	DELAY_RULE=J29.E25:U28.AH26:345P:425P	2 3	
D<23>	DELAY_RULE=J29.D30:U28.AD22:315P:395P	2 3	
D<24>	DELAY_RULE=J29.D26:U28.AD21:360P:440P	2 3	
D<25>	DELAY_RULE=J29.C27:U28.AF25:340P:420P	2 3	
D<26>	DELAY_RULE=J29.F22:U28.AJ25:315P:395P	2 3	
D<27>	DELAY_RULE=J29.D28:U28.AJ27:345P:425P	2 3	
D<28>	DELAY_RULE=J29.E23:U28.AE22:290P:370P	2 3	
D<29>	DELAY_RULE=J29.C25:U28.AK27:510P:590P	2 3	
D<3>	DELAY_RULE=J29.G21:U28.AH28:275P:355P	2 3	
D<30>	DELAY_RULE=J29.E21:U28.AJ29:310P:390P	2 3	
D<31>	DELAY_RULE=J29.F20:U28.AF21:315P:395P	2 3	
D<32>	DELAY_RULE=J29.F16:U28.AF18:305P:385P	2 3	
D<33>	DELAY_RULE=J29.D20:U28.AH20:480P:560P	2 3	
D<34>	DELAY_RULE=J29.E17:U28.AH22:265P:345P	2 3	
D<35>	DELAY_RULE=J29.F18:U28.AF20:280P:360P	2 3	
D<36>	DELAY_RULE=J29.E19:U28.AJ24:495P:575P	2 3	
D<37>	DELAY_RULE=J29.G13:U28.AH19:515P:595P	2 3	
D<38>	DELAY_RULE=J29.B22:U28.AD19:475P:555P	2 3	
D<39>	DELAY_RULE=J29.G15:U28.AK21:335P:415P	2 3	
D<4>	DELAY_RULE=J29.J29:U28.AH30:340P:420P	2 3	
D<40>	DELAY_RULE=J29.C21:U28.AE20:480P:560P	2 3	
D<41>	DELAY_RULE=J29.H20:U28.AK23:245P:325P	2 3	
D<42>	DELAY_RULE=J29.H16:U28.AK22:335P:415P	2 3	
D<43>	DELAY_RULE=J29.J23:U28.AF24:430P:510P	2 3	
D<44>	DELAY_RULE=J29.H22:U28.AK26:360P:440P	2 3	
D<45>	DELAY_RULE=J29.J17:U28.AJ22:310P:390P	2 3	
D<46>	DELAY_RULE=J29.J21:U28.AJ26:375P:455P	2 3	
D<47>	DELAY_RULE=J29.K22:U28.AG28:380P:460P	2 3	
D<48>	DELAY_RULE=J29.K20:U28.AF26:355P:435P	2 3	
D<49>	DELAY_RULE=J29.J27:U28.AF29:380P:460P	2 3	
D<5>	DELAY_RULE=J29.H26:U28.AC24:330P:410P	2 3	
D<50>	DELAY_RULE=J29.G29:U28.AB24:310P:390P	2 3	
D<51>	DELAY_RULE=J29.J19:U28.AF22:295P:375P	2 3	
D<52>	DELAY_RULE=J29.K24:U28.AD26:255P:335P	2 3	
D<53>	DELAY_RULE=J29.H24:U28.AK28:415P:495P	2 3	
D<54>	DELAY_RULE=J29.G27:U28.AF28:345P:425P	2 3	
D<55>	DELAY_RULE=J29.A19:U28.AK18:440P:520P	2 3	
D<56>	DELAY_RULE=J29.B20:U28.AE19:425P:505P	2 3	
D<57>	DELAY_RULE=J29.B24:U28.AJ19:500P:580P	2 3	
D<58>	DELAY_RULE=J29.A21:U28.AJ18:490P:570P	2 3	
D<59>	DELAY_RULE=J29.A17:U28.AH17:440P:520P	2 3	
D<6>	DELAY_RULE=J29.J25:U28.AD25:325P:405P	2 3	
D<60>	DELAY_RULE=J29.C19:U28.AH18:465P:545P	2 3	
D<61>	DELAY_RULE=J29.D24:U28.AH24:515P:595P	2 3	
D<62>	DELAY_RULE=J29.D22:U28.AF19:480P:560P	2 3	
D<63>	DELAY_RULE=J29.C23:U28.AJ20:505P:585P	2 3	
D<7>	DELAY_RULE=J29.K14:U28.AH21:275P:355P	2 3	
D<8>	DELAY_RULE=J29.J15:U28.AJ21:245P:325P	2 3	
D<9>	DELAY_RULE=J29.G17:U28.AJ23:275P:355P	2 3	
DTI<0>	DELAY_RULE=J29.A5:U28.AH15:515P:595P	2 3	
DTI<1>	DELAY_RULE=J29.F14:U28.AK17:370P:450P	2 3	
DTI<2>	DELAY_RULE=J29.A9:U28.AH16:465P:545P	2 3	
TSIZ<0>	DELAY_RULE=J29.D4:U28.AJ10:430P:510P	2 3	
TSIZ<1>	DELAY_RULE=J29.E3:U28.AK10:425P:505P	2 3	
TSIZ<2>	DELAY_RULE=J29.F6:U28.AF12:445P:525P	2 3	
TT<0>	DELAY_RULE=J29.B5:U28.AE12:390P:470P	2 3	
TT<1>	DELAY_RULE=J29.F8:U28.AF13:385P:465P	2 3	
TT<2>	DELAY_RULE=J29.H6:U28.AJ11:425P:505P	2 3	
TT<3>	DELAY_RULE=J29.G5:U28.AE13:405P:485P	2 3	
TT<4>	DELAY_RULE=J29.J11:U28.AH11:435P:515P	2 3	

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-0997 | REV. 01

SCALE NONE | SHT 5 OF 47

CR=6

MEMORY BUS LOADING:

ADDRESS, SDRAS, SDCAS, SDWE: 3 TO 48 LOADS (2 CLOCKS TO SETTLE)
DATA, DQM: 1 TO 6 LOADS
CKE, CS: 0 TO 6 LOADS

MEMORY CONTROLLER (UNI-N/2)

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-0997	REV. 01
	SCALE NONE	SHT 6	OF 47

8 7 6 MADDR<0..12>

8 7 6 MDATA<0..63>

J21 (DIMM A)

41 39 37 36 35 31 11 10 8 7 6 3 27 24 20 19 14 13 3_3V_SLEEP

TH

0	8 7 6 MDATA<0>	2	86	8 7 6 MDATA<32>	32
1	8 7 6 MDATA<1>	3	87	8 7 6 MDATA<33>	33
2	8 7 6 MDATA<2>	4	88	8 7 6 MDATA<34>	34
3	8 7 6 MDATA<3>	5	89	8 7 6 MDATA<35>	35
		6	90		
4	8 7 6 MDATA<4>	7	91	8 7 6 MDATA<36>	36
5	8 7 6 MDATA<5>	8	92	8 7 6 MDATA<37>	37
6	8 7 6 MDATA<6>	9	93	8 7 6 MDATA<38>	38
7	8 7 6 MDATA<7>	10	94	8 7 6 MDATA<39>	39
8	8 7 6 MDATA<8>	11	95	8 7 6 MDATA<40>	40
		12	96		
9	8 7 6 MDATA<9>	13	97	8 7 6 MDATA<41>	41
10	8 7 6 MDATA<10>	14	98	8 7 6 MDATA<42>	42
11	8 7 6 MDATA<11>	15	99	8 7 6 MDATA<43>	43
12	8 7 6 MDATA<12>	16	100	8 7 6 MDATA<44>	44
13	8 7 6 MDATA<13>	17	101	8 7 6 MDATA<45>	45
		18	102		
14	8 7 6 MDATA<14>	19	103	8 7 6 MDATA<46>	46
15	8 7 6 MDATA<15>	20	104	8 7 6 MDATA<47>	47
	MECC<0> (N.C.)	21	105	MECC<4> (N.C.)	
	MECC<1> (N.C.)	22	106	MECC<5> (N.C.)	
		23	107		
	N.C.	24	108	N.C.	
	N.C.	25	109	N.C.	
		26	110		
	8 7 6 WE_A*	27	111	SDCAS_A* 6 7 8	
	8 7 6 DQM<0>*	28	112	DQM<4>* 6 7 8	
	8 7 6 DQM<1>*	29	113	DQM<5>* 6 7 8	
	7 6 CS<0>*	30	114	CS<1>* 6 7	
	OE1*/N.C./D.U.	31	115	SDRAS_A* 6 7 8	
		32	116		
A0	8 7 6 MADDR<0>	33	117	8 7 6 MADDR<1>	A1
A2	8 7 6 MADDR<2>	34	118	8 7 6 MADDR<3>	A3
A4	8 7 6 MADDR<4>	35	119	8 7 6 MADDR<5>	A5
A6	8 7 6 MADDR<6>	36	120	8 7 6 MADDR<7>	A7
A8	8 7 6 MADDR<8>	37	121	8 7 6 MADDR<9>	A9
A10/AP	8 7 6 MADDR<10>	38	122	MBA0 6 7 8	BA0
BA1	8 7 6 MBA1	39	123	8 7 6 MADDR<11>	A11
		40	124		
		41	125	MCLK<1> 16	
	16 MCLK<0>	42	126	8 7 6 MADDR<12>	A12
		43	127		
	OE2*/N.C./D.U.	44	128	CKE<0> 6	
	7 6 CS<0>*	45	129	CS<1>* 6 7	
	8 7 6 DQM<2>*	46	130	DQM<6>* 6 7 8	
	8 7 6 DQM<3>*	47	131	DQM<7>* 6 7 8	
	WE*/N.C./D.U.	48	132	A13	
		49	133		
	N.C.	50	134	N.C.	
	N.C.	51	135	N.C.	
	MECC<2> (N.C.)	52	136	MECC<6> (N.C.)	
	MECC<3> (N.C.)	53	137	MECC<7> (N.C.)	
		54	138		
16	8 7 6 MDATA<16>	55	139	8 7 6 MDATA<48>	48
17	8 7 6 MDATA<17>	56	140	8 7 6 MDATA<49>	49
18	8 7 6 MDATA<18>	57	141	8 7 6 MDATA<50>	50
19	8 7 6 MDATA<19>	58	142	8 7 6 MDATA<51>	51
		59	143		
20	8 7 6 MDATA<20>	60	144	8 7 6 MDATA<52>	52
	N.C.	61	145	N.C.	
	N.C./N.C./VREF	62	146	N.C./N.C./VREF	
	6 CKE<1>	63	147	N.C./N.C./REGISTER_EN	
		64	148		
21	8 7 6 MDATA<21>	65	149	8 7 6 MDATA<53>	53
22	8 7 6 MDATA<22>	66	150	8 7 6 MDATA<54>	54
23	8 7 6 MDATA<23>	67	151	8 7 6 MDATA<55>	55
		68	152		
24	8 7 6 MDATA<24>	69	153	8 7 6 MDATA<56>	56
25	8 7 6 MDATA<25>	70	154	8 7 6 MDATA<57>	57
26	8 7 6 MDATA<26>	71	155	8 7 6 MDATA<58>	58
27	8 7 6 MDATA<27>	72	156	8 7 6 MDATA<59>	59
		73	157		
28	8 7 6 MDATA<28>	74	158	8 7 6 MDATA<60>	60
29	8 7 6 MDATA<29>	75	159	8 7 6 MDATA<61>	61
30	8 7 6 MDATA<30>	76	160	8 7 6 MDATA<62>	62
31	8 7 6 MDATA<31>	77	161	8 7 6 MDATA<63>	63
		78	162		
	16 MCLK<2>	79	163	MCLK<3> 16	
	N.C.	80	164	N.C.	
	WP	81	165	SA0	
35 19 8 7 2	UNI_IIC_DAT	82	166	SA1 ADDR=0 (A0)	
35 19 8 7 2	UNI_IIC_CLK	83	167	SA2	
		84	168		

NOTES ON MULTI-USE PINS:
FAST PAGE/UNBUFFERED/REGISTERED

3_3V_SLEEP

C209 10UF N20P80% 16V CERM 1210

R93 82 5% 1/16W MF 603

ITSON

DS5 RED SM

LED TO WARN THAT POWER IS PRESENT AT DIMMS

3_3V_SLEEP

C64 10UF N20P80% 16V CERM 1210

J22 (DIMM B)

36 35 31 27 24 10 8 7 6 3 20 19 14 13 11 41 39 37 3_3V_SLEEP

TH

0	8 7 6 MDATA<0>	2	86	8 7 6 MDATA<32>	32
1	8 7 6 MDATA<1>	3	87	8 7 6 MDATA<33>	33
2	8 7 6 MDATA<2>	4	88	8 7 6 MDATA<34>	34
3	8 7 6 MDATA<3>	5	89	8 7 6 MDATA<35>	35
		6	90		
4	8 7 6 MDATA<4>	7	91	8 7 6 MDATA<36>	36
5	8 7 6 MDATA<5>	8	92	8 7 6 MDATA<37>	37
6	8 7 6 MDATA<6>	9	93	8 7 6 MDATA<38>	38
7	8 7 6 MDATA<7>	10	94	8 7 6 MDATA<39>	39
8	8 7 6 MDATA<8>	11	95	8 7 6 MDATA<40>	40
		12	96		
9	8 7 6 MDATA<9>	13	97	8 7 6 MDATA<41>	41
10	8 7 6 MDATA<10>	14	98	8 7 6 MDATA<42>	42
11	8 7 6 MDATA<11>	15	99	8 7 6 MDATA<43>	43
12	8 7 6 MDATA<12>	16	100	8 7 6 MDATA<44>	44
13	8 7 6 MDATA<13>	17	101	8 7 6 MDATA<45>	45
		18	102		
14	8 7 6 MDATA<14>	19	103	8 7 6 MDATA<46>	46
15	8 7 6 MDATA<15>	20	104	8 7 6 MDATA<47>	47
	MECC<0> (N.C.)	21	105	MECC<4> (N.C.)	
	MECC<1> (N.C.)	22	106	MECC<5> (N.C.)	
		23	107		
	N.C.	24	108	N.C.	
	N.C.	25	109	N.C.	
		26	110		
	8 7 6 WE_A*	27	111	SDCAS_A* 6 7 8	
	8 7 6 DQM<0>*	28	112	DQM<4>* 6 7 8	
	8 7 6 DQM<1>*	29	113	DQM<5>* 6 7 8	
	7 6 CS<2>*	30	114	CS<3>* 6 7	
	OE1*/N.C./D.U.	31	115	SDRAS_A* 6 7 8	
		32	116		
A0	8 7 6 MADDR<0>	33	117	8 7 6 MADDR<1>	A1
A2	8 7 6 MADDR<2>	34	118	8 7 6 MADDR<3>	A3
A4	8 7 6 MADDR<4>	35	119	8 7 6 MADDR<5>	A5
A6	8 7 6 MADDR<6>	36	120	8 7 6 MADDR<7>	A7
A8	8 7 6 MADDR<8>	37	121	8 7 6 MADDR<9>	A9
A10/AP	8 7 6 MADDR<10>	38	122	MBA0 6 7 8	BA0
BA1	8 7 6 MBA1	39	123	8 7 6 MADDR<11>	A11
		40	124		
		41	125	MCLK<5> 16	
	16 MCLK<4>	42	126	8 7 6 MADDR<12>	A12
		43	127		
	OE2*/N.C./D.U.	44	128	CKE<2> 6	
	7 6 CS<2>*	45	129	CS<3>* 6 7	
	8 7 6 DQM<2>*	46	130	DQM<6>* 6 7 8	
	8 7 6 DQM<3>*	47	131	DQM<7>* 6 7 8	
	WE*/N.C./D.U.	48	132	A13	
		49	133		
	N.C.	50	134	N.C.	
	N.C.	51	135	N.C.	
	MECC<2> (N.C.)	52	136	MECC<6> (N.C.)	
	MECC<3> (N.C.)	53	137	MECC<7> (N.C.)	
		54	138		
16	8 7 6 MDATA<16>	55	139	8 7 6 MDATA<48>	48
17	8 7 6 MDATA<17>	56	140	8 7 6 MDATA<49>	49
18	8 7 6 MDATA<18>	57	141	8 7 6 MDATA<50>	50
19	8 7 6 MDATA<19>	58	142	8 7 6 MDATA<51>	51
		59	143		
20	8 7 6 MDATA<20>	60	144	8 7 6 MDATA<52>	52
	N.C.	61	145	N.C.	
	N.C./N.C./VREF	62	146	N.C./N.C./VREF	
	6 CKE<3>	63	147	N.C./N.C./REGISTER_EN	
		64	148		
21	8 7 6 MDATA<21>	65	149	8 7 6 MDATA<53>	53
22	8 7 6 MDATA<22>	66	150	8 7 6 MDATA<54>	54
23	8 7 6 MDATA<23>	67	151	8 7 6 MDATA<55>	55
		68	152		
24	8 7 6 MDATA<24>	69	153	8 7 6 MDATA<56>	56
25	8 7 6 MDATA<25>	70	154	8 7 6 MDATA<57>	57
26	8 7 6 MDATA<26>	71	155	8 7 6 MDATA<58>	58
27	8 7 6 MDATA<27>	72	156	8 7 6 MDATA<59>	59
		73	157		
28	8 7 6 MDATA<28>	74	158	8 7 6 MDATA<60>	60
29	8 7 6 MDATA<29>	75	159	8 7 6 MDATA<61>	61
30	8 7 6 MDATA<30>	76	160	8 7 6 MDATA<62>	62
31	8 7 6 MDATA<31>	77	161	8 7 6 MDATA<63>	63
		78	162		
	16 MCLK<6>	79	163	MCLK<7> 16	
	N.C.	80	164	N.C.	
	WP	81	165	SA0	
35 19 8 7 2	UNI_IIC_DAT	82	166	SA1 ADDR=1 (A2)	
35 19 8 7 2	UNI_IIC_CLK	83	167	SA2	
		84	168		

SDRAM DIMMS

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-0997 | REV. 01

SCALE NONE | SHT 7 OF 47

8 7 6 MADDR<0..12>

8 7 6 MDATA<0..63>

41 39 37 36
13 11 10 8 7 6 3 3_3V_SLEEP
35 31 27 24 20 19 14

J23
TH

0	8 7 6 MDATA<0>	2	86	8 7 6 MDATA<32>	32
1	8 7 6 MDATA<1>	3	87	8 7 6 MDATA<33>	33
2	8 7 6 MDATA<2>	4	88	8 7 6 MDATA<34>	34
3	8 7 6 MDATA<3>	5	89	8 7 6 MDATA<35>	35
		6	90		
4	8 7 6 MDATA<4>	7	91	8 7 6 MDATA<36>	36
5	8 7 6 MDATA<5>	8	92	8 7 6 MDATA<37>	37
6	8 7 6 MDATA<6>	9	93	8 7 6 MDATA<38>	38
7	8 7 6 MDATA<7>	10	94	8 7 6 MDATA<39>	39
8	8 7 6 MDATA<8>	11	95	8 7 6 MDATA<40>	40
		12	96		
9	8 7 6 MDATA<9>	13	97	8 7 6 MDATA<41>	41
10	8 7 6 MDATA<10>	14	98	8 7 6 MDATA<42>	42
11	8 7 6 MDATA<11>	15	99	8 7 6 MDATA<43>	43
12	8 7 6 MDATA<12>	16	100	8 7 6 MDATA<44>	44
13	8 7 6 MDATA<13>	17	101	8 7 6 MDATA<45>	45
		18	102		
14	8 7 6 MDATA<14>	19	103	8 7 6 MDATA<46>	46
15	8 7 6 MDATA<15>	20	104	8 7 6 MDATA<47>	47
	MECC<0> (N.C.)	21	105	MECC<4> (N.C.)	
	MECC<1> (N.C.)	22	106	MECC<5> (N.C.)	
		23	107		
	N.C.	24	108	N.C.	
	N.C.	25	109	N.C.	
		26	110		
	8 7 6 WE_A*	27	111	SDCAS_A* 6 7 8	
	7 6 DQM<0>*	28	112	DQM<4>* 6 7	
	7 6 DQM<1>*	29	113	DQM<5>* 6 7	
	8 6 CS<4>*	30	114	CS<5>* 6 8	
	OE1*/N.C./D.U.	31	115	SDRAS_A* 6 7 8	
		32	116		
A0	0 8 7 6 MADDR<0>	33	117	8 7 6 MADDR<1> 1	A1
A2	2 8 7 6 MADDR<2>	34	118	8 7 6 MADDR<3> 3	A3
A4	4 8 7 6 MADDR<4>	35	119	8 7 6 MADDR<5> 5	A5
A6	6 8 7 6 MADDR<6>	36	120	8 7 6 MADDR<7> 7	A7
A8	8 8 7 6 MADDR<8>	37	121	8 7 6 MADDR<9> 9	A9
A10/AP	10 8 7 6 MADDR<10>	38	122	MBA0 6 7 8	BA0
BA1	8 7 6 MBA1	39	123	8 7 6 MADDR<11> 11	A11
		40	124		
		41	125	MCLK<9> 16	
	16 MCLK<8>	42	126	8 7 6 MADDR<12> 12	A12
		43	127		
	OE2*/N.C./D.U.	44	128	CKE<4> 6	
	8 6 CS<4>*	45	129	CS<5>* 6 8	
	7 6 DQM<2>*	46	130	DQM<6>* 6 7	
	7 6 DQM<3>*	47	131	DQM<7>* 6 7	
	WE*/N.C./D.U.	48	132	A13	
		49	133		
	N.C.	50	134	N.C.	
	N.C.	51	135	N.C.	
	MECC<2> (N.C.)	52	136	MECC<6> (N.C.)	
	MECC<3> (N.C.)	53	137	MECC<7> (N.C.)	
		54	138		
16	8 7 6 MDATA<16>	55	139	8 7 6 MDATA<48>	48
17	8 7 6 MDATA<17>	56	140	8 7 6 MDATA<49>	49
18	8 7 6 MDATA<18>	57	141	8 7 6 MDATA<50>	50
19	8 7 6 MDATA<19>	58	142	8 7 6 MDATA<51>	51
		59	143		
20	8 7 6 MDATA<20>	60	144	8 7 6 MDATA<52>	52
	N.C.	61	145	N.C.	
	N.C./N.C./VREF	62	146	N.C./N.C./VREF	
	6 CKE<5>	63	147	N.C./N.C./REGISTER_EN	
		64	148		
21	8 7 6 MDATA<21>	65	149	8 7 6 MDATA<53>	53
22	8 7 6 MDATA<22>	66	150	8 7 6 MDATA<54>	54
23	8 7 6 MDATA<23>	67	151	8 7 6 MDATA<55>	55
		68	152		
24	8 7 6 MDATA<24>	69	153	8 7 6 MDATA<56>	56
25	8 7 6 MDATA<25>	70	154	8 7 6 MDATA<57>	57
26	8 7 6 MDATA<26>	71	155	8 7 6 MDATA<58>	58
27	8 7 6 MDATA<27>	72	156	8 7 6 MDATA<59>	59
		73	157		
28	8 7 6 MDATA<28>	74	158	8 7 6 MDATA<60>	60
29	8 7 6 MDATA<29>	75	159	8 7 6 MDATA<61>	61
30	8 7 6 MDATA<30>	76	160	8 7 6 MDATA<62>	62
31	8 7 6 MDATA<31>	77	161	8 7 6 MDATA<63>	63
		78	162		
	16 MCLK<10>	79	163	MCLK<11> 16	
	N.C.	80	164	N.C.	
	WP	81	165	SA0	
35 19 7 2	UNI_IIC_DAT	82	166	SA1 ADDR=2 (A4)	
35 19 7 2	UNI_IIC_CLK	83	167	SA2	
		84	168		

DIMM C

3_3V_SLEEP
C63
10UF
N20P80%
16V
2 CERM
1210

3_3V_SLEEP
C211
10UF
N20P80%
16V
2 CERM
1210

1_8V_TERM 37

L46
FERR-250-OHM
1 2
SM
SDRAM_TERM_POWER
MIN_LINE_WIDTH=25

C210
150UF
20%
2.5V
TANT
SMD
POSCAP

8 7 6 SDRAS_A*	R426 54.9	1% 1/16W	603	C374 2.2UF N20P80% 16V CERM 805
8 7 6 SDCAS_A*	R425 54.9	1% 1/16W	603	
8 7 6 WE_A*	R428 54.9	1% 1/16W	603	
8 7 6 MBA0	R442 54.9	1% 1/16W	603	
8 7 6 MBA1	R444 54.9	1% 1/16W	603	
0 8 7 6 MADDR<0>	R446 54.9	1% 1/16W	603	C362 2.2UF N20P80% 16V CERM 805
1 8 7 6 MADDR<1>	R427 54.9	1% 1/16W	603	
2 8 7 6 MADDR<2>	R447 54.9	1% 1/16W	603	
3 8 7 6 MADDR<3>	R429 54.9	1% 1/16W	603	C363 2.2UF N20P80% 16V CERM 805
4 8 7 6 MADDR<4>	R448 54.9	1% 1/16W	603	
5 8 7 6 MADDR<5>	R440 54.9	1% 1/16W	603	
6 8 7 6 MADDR<6>	R450 54.9	1% 1/16W	603	C372 2.2UF N20P80% 16V CERM 805
7 8 7 6 MADDR<7>	R430 54.9	1% 1/16W	603	
8 8 7 6 MADDR<8>	R445 54.9	1% 1/16W	603	
9 8 7 6 MADDR<9>	R441 54.9	1% 1/16W	603	C371 2.2UF N20P80% 16V CERM 805
10 8 7 6 MADDR<10>	R449 54.9	1% 1/16W	603	
11 8 7 6 MADDR<11>	R443 54.9	1% 1/16W	603	
12 8 7 6 MADDR<12>	R439 54.9	1% 1/16W	603	C373 2.2UF N20P80% 16V CERM 805

DC TERMINATION
PLACE NEAR DIMM C

PLACEMENT NOTE:
DIMM A IS NEAREST UNI-N
DIMM C IS FARTHEST UNI-N

MORE SDRAM DIMMS

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-0997	REV. 01
	SCALE NONE	SHT 8 OF 47	

33 MHZ PCI ACCESS / EMERGENCY OVERRIDE ROM SOCKET

BOOT MEMORY, PCI SLOT E

UNI-N MUST TRISTATE/DRIVE LOW SIGNALS DURING SLEEP

UNI-N PCI BUS ALSO USED FOR ROM:
AD<0..20> = ROM ADDRESS
AD<24-31> = ROM DATA

J26
F-ST-53643
SM
84
PLUG
+5V +3.3V +3.3V

9 6	ROMOE*	2	1	ROMWE*	6 9
41 24 15 13 12 9	33PCI_AD<1>	4	3	33PCI_AD<0>	9 12 13 15 24 41
		6	5	33PCI_AD<2>	9 12 13 15 24 41
41 24 15 13 12 9	33PCI_AD<3>	8	7		
41 24 15 13 12 9	33PCI_AD<5>	10	9	33PCI_AD<4>	9 12 13 15 24 41
		12	11	33PCI_AD<6>	9 12 13 15 24 41
41 24 15 13 12 9	33PCI_AD<7>	14	13		
41 24 15 13 12 9	33PCI_AD<8>	16	15	33PCI_CBE<0>*	12 13 15 24 41
		18	17	33PCI_AD<9>	9 12 13 15 24 41
41 24 15 13 12 9	33PCI_AD<10>	20	19		
41 24 15 13 12 9	33PCI_AD<12>	22	21	33PCI_AD<11>	9 12 13 15 24 41
		24	23	33PCI_AD<13>	9 12 13 15 24 41
41 24 15 13 12 9	33PCI_AD<14>	26	25		
41 24 15 13 12	33PCI_CBE<1>*	28	27	33PCI_AD<15>	9 12 13 15 24 41
	ROM_CS*	30	29	33PCI_PAR	12 13 15 24 41
		32	31	33PCI_STOP*	12 13 15 24 35 41
41 35 24 15 13 12	33PCI_DEVSEL*	34	33		
9	ROM_ONBOARD_CS*	36	35	33PCI_TRDY*	12 13 15 24 35 41
41 35 24 15 13 12	33PCI_IRDY*	38	37		
		40	39	33PCI_FRAME*	12 13 15 24 35 41
41 24 15 13 12	33PCI_CBE<2>*	42	41		
41 24 15 13 12 9	33PCI_AD<17>	44	43	33PCI_AD<16>	9 12 13 15 24 41
		46	45	33PCI_AD<18>	9 12 13 15 24 41
41 24 15 13 12 9	33PCI_AD<19>	48	47		
41 24 15 13 12 9	33PCI_AD<21>	50	49	33PCI_AD<20>	9 12 13 15 24 41
		52	51	33PCI_AD<22>	12 13 15 24 41
41 24 15 13 12	33PCI_AD<23>	54	53		
41 24 15 13 12	33PCI_CBE<3>*	56	55	NIGEL_IDSEL	
		58	57	33PCI_AD<24>	9 12 13 15 24 41
41 24 15 13 12 9	33PCI_AD<25>	60	59		
41 24 15 13 12 9	33PCI_AD<27>	62	61	33PCI_AD<26>	9 12 13 15 24 41
		64	63	33PCI_AD<28>	9 12 13 15 24 41
41 24 15 13 12 9	33PCI_AD<29>	66	65		
41 24 15 13 12 9	33PCI_AD<31>	68	67	33PCI_AD<30>	9 12 13 15 24 41
		70	69	PME*	13 14 19 20 27 36 38
35 12	NIGEL_PCI_REQ0* (REQ0*)	72	71		
		74	73	NIGEL_PCI_GNT0* (GNT0*)	12
18	NIGEL_PCI_CLK	76	75	RESERVED	
		78	77	MAIN_RESET*	9 12 13 14 33 36 41
	RESERVED	80	79	EXTINT12	27 35

83

R76
22
5%
1/16W
MF
402
1 — 2 — 33PCI_AD<21> 9 12 13 15 24 41

J17
F-ST-53643
SM
84
PLUG
+3.3V +3.3V

35 15 13 12	33PCI_ACK64*	2	1	33PCI_REQ64*	12 13 15 35
	RESERVED	4	3		
		6	5	33PCI_CBE<7>*	12 13 15 35
35 15 13 12	33PCI_CBE<6>*	8	7	33PCI_CBE<5>*	12 13 15 35
35 15 13 12	33PCI_CBE<4>*	10	9		
		12	11	33PCI_PAR64	12 13 15 35
35 15 13 12	33PCI_AD<63>	14	13	33PCI_AD<62>	12 13 15 35
35 15 13 12	33PCI_AD<61>	16	15		
		18	17	33PCI_AD<60>	12 13 15 35
35 15 13 12	33PCI_AD<59>	20	19	33PCI_AD<58>	12 13 15 35
35 15 13 12	33PCI_AD<57>	22	21		
		24	23	33PCI_AD<56>	12 13 15 35
35 15 13 12	33PCI_AD<55>	26	25	33PCI_AD<54>	12 13 15 35
35 15 13 12	33PCI_AD<53>	28	27		
		30	29	33PCI_AD<52>	12 13 15 35
35 15 13 12	33PCI_AD<51>	32	31	33PCI_AD<50>	12 13 15 35
35 15 13 12	33PCI_AD<49>	34	33		
		36	35	33PCI_AD<48>	12 13 15 35
35 15 13 12	33PCI_AD<47>	38	37	33PCI_AD<46>	12 13 15 35
35 15 13 12	33PCI_AD<45>	40	39		
		42	41	33PCI_AD<44>	12 13 15 35
35 15 13 12	33PCI_AD<43>	44	43	33PCI_AD<42>	12 13 15 35
35 15 13 12	33PCI_AD<41>	46	45		
		48	47	33PCI_AD<40>	12 13 15 35
35 15 13 12	33PCI_AD<39>	50	49	33PCI_AD<38>	12 13 15 35
35 15 13 12	33PCI_AD<37>	52	51		
		54	53	33PCI_AD<36>	12 13 15 35
35 15 13 12	33PCI_AD<35>	56	55	33PCI_AD<34>	12 13 15 35
35 15 13 12	33PCI_AD<33>	58	57		
		60	59	33PCI_AD<32>	12 13 15 35
41 35 12	FW_PCI_REQ* (REQ1)	62	61		
		64	63	RESERVED FW_PCI_GNT* (GNT1)	12 41
35 13 12	RESERVED 33SLOT1_REQ* (REQ2)	66	65		
		68	67	RESERVED 33SLOT1_GNT* (GNT2)	12 13
35 13 12	RESERVED 33SLOT2_REQ* (REQ3)	70	69		
		72	71	RESERVED 33SLOT2_GNT* (GNT3)	12 13
35 13 12	RESERVED 33SLOT3_REQ* (REQ4)	74	73		
		76	75	RESERVED 33SLOT3_GNT* (GNT4)	12 13
35 24 12	RESERVED KWEST_PCI_REQ* (REQ5)	78	77		
	RESERVED	80	79	RESERVED KWEST_PCI_GNT* (GNT5)	12 24

83

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341T0601	1	IC, BOOTROM, P21	U7	

PROGRAMMING VOLTAGE IS 5V FOR MICRON, 3.3V FOR INTEL

+5V +3.3V +3.3V

LEAKAGE PATHS?

R421
0
5%
1/16W
MF
402
1 — 2 — ROM_VPP

NO STUFF
R420
0
5%
1/16W
MF
402

MIN_LINE_WIDTH=25

C352
0.01UF
20%
50V
CERM
402

C68
0.01UF
20%
50V
CERM
402

VPP 11 — 30 VCC 31

U7
FEPR-1MX8
110
TSOP

41 24 15 13 12 9	33PCI_AD<0>	21	A0	DQ0	25 33PCI_AD<24> 9 12 13 15 24 41
41 24 15 13 12 9	33PCI_AD<1>	20	A1	DQ1	26 33PCI_AD<25> 9 12 13 15 24 41
41 24 15 13 12 9	33PCI_AD<2>	19	A2	DQ2	27 33PCI_AD<26> 9 12 13 15 24 41
41 24 15 13 12 9	33PCI_AD<3>	18	A3	DQ3	28 33PCI_AD<27> 9 12 13 15 24 41
41 24 15 13 12 9	33PCI_AD<4>	17	A4	DQ4	32 33PCI_AD<28> 9 12 13 15 24 41
41 24 15 13 12 9	33PCI_AD<5>	16	A5	DQ5	33 33PCI_AD<29> 9 12 13 15 24 41
41 24 15 13 12 9	33PCI_AD<6>	15	A6	DQ6	34 33PCI_AD<30> 9 12 13 15 24 41
41 24 15 13 12 9	33PCI_AD<7>	14	A7	DQ7	35 33PCI_AD<31> 9 12 13 15 24 41
41 24 15 13 12 9	33PCI_AD<8>	8	A8		
41 24 15 13 12 9	33PCI_AD<9>	7	A9		
41 24 15 13 12 9	33PCI_AD<10>	36	A10		
41 24 15 13 12 9	33PCI_AD<11>	6	A11		
41 24 15 13 12 9	33PCI_AD<12>	5	A12		
41 24 15 13 12 9	33PCI_AD<13>	4	A13		
41 24 15 13 12 9	33PCI_AD<14>	3	A14		
41 24 15 13 12 9	33PCI_AD<15>	2	A15		
41 24 15 13 12 9	33PCI_AD<16>	1	A16		
41 24 15 13 12 9	33PCI_AD<17>	40	A17		
41 24 15 13 12 9	33PCI_AD<18>	13	A18		
41 24 15 13 12 9	33PCI_AD<19>	37	A19		
41 24 15 13 12 9	33PCI_AD<20>	38	A20		

MSB
A20 NOT USED FOR 1 MBYTE DEVICE

9	ROM_ONBOARD_CS*	22 CE
9 6	ROMOE*	24 OE
9 6	ROMWE*	9 WE
	BOOTWP*	12 WP
		10 PWD
		GND
		23 — 39

+3.3V

R140
10K
5%
1/16W
MF
402
ENSURE FLASH NOT SELECTED
WHEN ENTERING SLEEP MODE

R138
1K
5%
1/16W
MF
603
6 ROMCS* — 1 — 2
OVERRIDE ROM MODULE INTERCEPTS ROM CHIP SELECT

+3.3V

ENABLE WRITES TO BOOT BLOCK

R412
1K
5%
1/16W
MF
603

DISABLE WRITES TO BOOT BLOCK

NO STUFF
R411
10K
5%
1/16W
MF
402
14 13 12 9 MAIN_RESET* — 1
41 36 33
RESET FLASH AT RESTART

R438
49.9
1%
1/16W
MF
603
2 — FLASH_PWD*

FLASH EEPROM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-0997	01
SCALE NONE	SHT 9 OF 47	

CR-10

MAXBUS INTERFACE DECOUPLING

35 19 4 3 2 MAXBUS_IO_RAIL

C4 C99 C137 C156 C177 C244 C308 C340 C428
C5 C101 C138 C157 C178 C245 C309 C343 C429
C6 C102 C139 C158 C182 C246 C310 C345 C430
C7 C140 C159 C184 C247 C311 C397
C8 C122 C141 C160 C185 C248 C312 C398 C432
C9 C123 C142 C165 C188 C249 C313 C399 C433
C10 C124 C143 C166 C189 C250 C314 C400 C434
C125 C144 C167 C411 C435
C12 C126 C146 C168 C205 C316 C414 C436
C74 C78 C75 C79 — 2.2UF N20P80% 16V CERM 805

SDRAM DECOUPLING

27 24 20 19 14 13 11 10 8 7 6 3 41 39 37 36 35 31 3_3V_SLEEP

C445 C471 C484 C497 C510 C523 C536 C549
C446 C472 C485 C498 C524 C537 C550
C447 C473 C486 C499 C525 C551
C448 C461 C474 C487 C500 C526 C539 C552
C449 C462 C475 C488 C501 C527 C540 C553
C450 C463 C476 C489 C502 C528 C541 C554

AGP/PCI DECOUPLING

27 24 20 19 14 13 11 10 8 7 6 3 41 39 37 36 35 31 3_3V_SLEEP

C451 C464 C477 C490 C503 C529 C542 C555
C530 C543 C556

19 14 AGP_IO_RAIL

C452 C465 C504 C517
C453 C466 C492 C505 C518 C531 C544 C557
C454 C493 C506 C519 C532 C545 C558
C455 C481 C494 C507 C520 C533 C546 C559
C90 C92 C91 C93 — 2.2UF N20P80% 16V CERM 805

1394/ETHERNET DECOUPLING

27 24 20 19 14 13 11 10 8 7 6 3 41 39 37 36 35 31 3_3V_SLEEP

C14 C127 C148 C169 C206 C253 C317 C415
C25 C128 C170 C208 C254 C318 C416
C26 C129 C150 C171 C215 C259 C319 C422 C439
C94 C130 C151 C216 C265 C320 C423 C440
C95 C133 C173 C240 C289 C333 C424 C441
C96 C241 C305 C336 C425 C442
C97 C135 C154 C175 C242 C306 C337 C426 C443
C98 C136 C155 C176 C243 C307 C338 C427 C444
C76 C88 C77 C89 — 2.2UF N20P80% 16V CERM 805

CORE DECOUPLING

37 20 19 10 6 1_8V_SLEEP

C456 C469 C482 C495 C508 C521 C534 C547 C560
C457 C470 C483 C496 C509 C522 C535 C548 C561

37 20 19 10 6 1_8V_SLEEP

C145 C131 C132 C147 — 2.2UF N20P80% 16V CERM 805

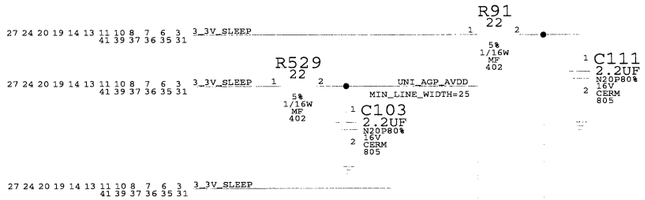
PLACE AROUND PERIMETER OF CORE POWER PINS NEAR CORNERS

UNI-N POWER DECOUPLING

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-0997 | REV. 01

SCALE NONE | SHT 10 OF 47



F7 E5 C3

AGP_CLKIN_VDD3 AGPPLLAVD AGPPLLDVD

U28
UNI-N-1.5
(3 OF 5)
PBGA-UNIN-1.5

AGPREQ	14 AGP_REQ* DELAY_RULE=:::130% NET_SPACING_TYPE=AGP2	C4	AGPAD_0	E18	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<0> 14
			AGPAD_1	C19	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<1> 14
			AGPAD_2	B19	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<2> 14
			AGPAD_3	E16	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<3> 14
			AGPAD_4	A19	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<4> 14
			AGPAD_5	C18	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<5> 14
			AGPAD_6	E17	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<6> 14
			AGPAD_7	B18	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<7> 14
			AGPAD_8	A18	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<8> 14
			AGPAD_9	C17	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<9> 14
AGPGNT	14 AGP_GNT* DELAY_RULE=:::130% NET_SPACING_TYPE=AGP2	E9	AGPAD_10	B17	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<10> 14
			AGPAD_11	A17	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<11> 14
			AGPAD_12	C16	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<12> 14
			AGPAD_13	G15	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<13> 14
			AGPAD_14	B16	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<14> 14
			AGPAD_15	C15	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<15> 14
			AGPAD_16	E14	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<16> 14
AGPCLK	18 UNI_EXT_PCICLK F6		AGPAD_17	F13	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<17> 14
			AGPAD_18	A13	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<18> 14
			AGPAD_19	B13	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<19> 14
AGPPAR	14 AGP_PAR DELAY_RULE=:::130% NET_SPACING_TYPE=AGP2	B14	AGPAD_20	C13	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<20> 14
AGPFRAME	14 AGP_FRAME* DELAY_RULE=:::130% NET_SPACING_TYPE=AGP2	B15	AGPAD_21	A12	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<21> 14
AGPTRDY	14 AGP_TRDY* DELAY_RULE=:::130% NET_SPACING_TYPE=AGP2	C14	AGPAD_22	B12	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<22> 14
AGPIRDY	14 AGP_IRDY* DELAY_RULE=:::130% NET_SPACING_TYPE=AGP2	A14	AGPAD_23	C12	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<23> 14
AGPSTOP	14 AGP_STOP* DELAY_RULE=:::130% NET_SPACING_TYPE=AGP2	E13	AGPAD_24	B11	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<24> 14
AGPDEVSEL	14 AGP_DEVSEL* DELAY_RULE=:::130% NET_SPACING_TYPE=AGP2	B7	AGPAD_25	C11	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<25> 14
			AGPAD_26	B10	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<26> 14
			AGPAD_27	E11	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<27> 14
AGPCBE_0	14 AGP_CBE<0>* DELAY_RULE=:::130% NET_SPACING_TYPE=AGP2	G14	AGPAD_28	C10	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<28> 14
AGPCBE_1	14 AGP_CBE<1>* DELAY_RULE=:::130% NET_SPACING_TYPE=AGP2	E15	AGPAD_29	A9	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<29> 14
AGPCBE_2	14 AGP_CBE<2>* DELAY_RULE=:::130% NET_SPACING_TYPE=AGP2	A8	AGPAD_30	B9	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<30> 14
AGPCBE_3	14 AGP_CBE<3>* DELAY_RULE=:::130% NET_SPACING_TYPE=AGP2	C9	AGPAD_31	G13	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD<31> 14
AGPST_0	14 AGP_ST<0> DELAY_RULE=:::130% NET_SPACING_TYPE=AGP2	E10	AGPSBA_0	C7	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_SBA<0> 14
AGPST_1	14 AGP_ST<1> DELAY_RULE=:::130% NET_SPACING_TYPE=AGP2	C8	AGPSBA_1	B6	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_SBA<1> 14
AGPST_2	14 AGP_ST<2> DELAY_RULE=:::130% NET_SPACING_TYPE=AGP2	B8	AGPSBA_2	C6	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_SBA<2> 14
			AGPSBA_3	B5	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_SBA<3> 14
AGPPIPE	14 AGP_PIPE* DELAY_RULE=:::1.5N NET_SPACING_TYPE=AGP2	B2	AGPSBA_4	A4	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_SBA<4> 14
AGPRBF	14 AGP_RBF* DELAY_RULE=:::1.5N NET_SPACING_TYPE=AGP2	E6	AGPSBA_5	C5	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_SBA<5> 14
AGPWBF	14 AGP_WBF* DELAY_RULE=:::1.5N NET_SPACING_TYPE=AGP2	B3	AGPSBA_6	F8	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_SBA<6> 14
			AGPSBA_7	B4	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP	NET_PHYSICAL_TYPE=AGP_DATA	AGP_SBA<7> 14
AGPPME	AGP_PME	A7						
AGPTYPEDET		A3						

AGP INTERFACE

R36
1K
5%
1/16W
MF
603
14 AGP_TYPEDET*

AGPSB_STB	AGPSB_STB	F9	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP_STB	NET_PHYSICAL_TYPE=AGP_DATA	AGP_SB_STB 14
AGPSB_STB*	AGPSB_STB*	G9	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP_STB	NET_PHYSICAL_TYPE=AGP_DATA	AGP_SB_STB* 14
AGPAD_STB0	AGPAD_STB0	F16	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP_STB	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD_STB0 14
AGPAD_STB0*	AGPAD_STB0*	F15	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP_STB	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD_STB0* 14
AGPAD_STB1	AGPAD_STB1	F12	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP_STB	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD_STB1 14
AGPAD_STB1*	AGPAD_STB1*	E12	DELAY_RULE=::3000:4000	NET_SPACING_TYPE=AGP_STB	NET_PHYSICAL_TYPE=AGP_DATA	AGP_AD_STB1* 14

LENGTH OF STROBES MUST BE LONGEST IN RESPECTIVE GROUPS

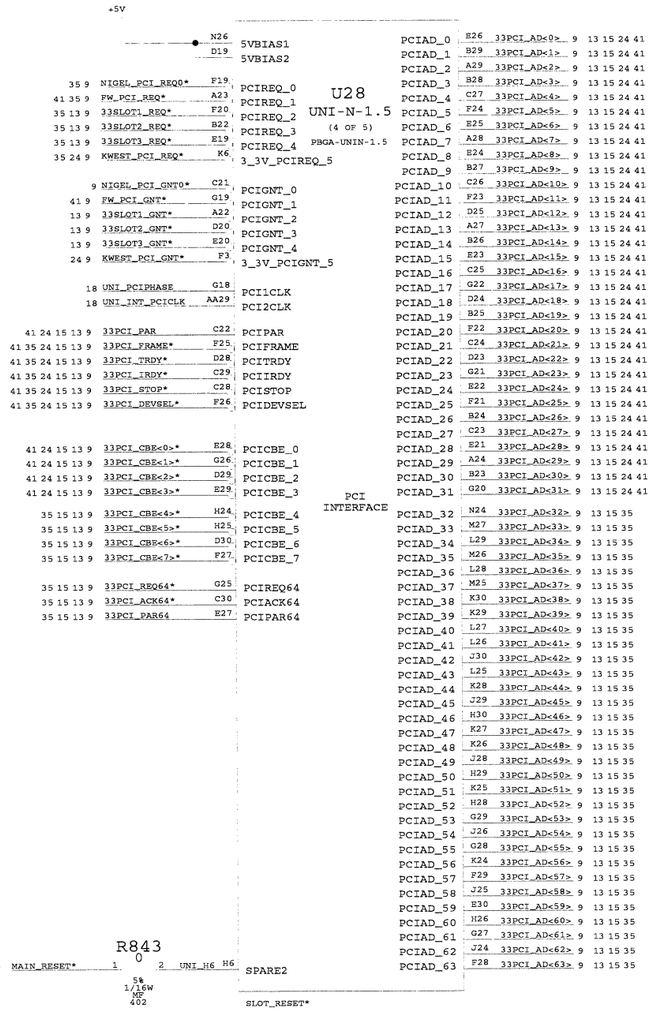
AGP_VREF F11 AGP_VREF_GC 14
AGBU4RTAP G10 AGP_AGBU4RTAP

R840
475
1%
1/16W
MF
603

AGPPLLAVS AGPPLLDVS
E7 G8

AGP CONTROLLER (UNI-N/3)

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-0997	REV. 01
	SCALE NONE	SHT 11 OF 47	



PCI HOST CONTROLLER (UNI-N/4)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-0997 | REV. 01

SCALE NONE | SHT 12 OF 47

SLOT B

J12 TH

+3.3V +5V +3.3V +12V -12V +5V +3.3V

NO STUFF
R42 10K 5% 1/16W MF 402

	B1	A1	33PCI_TRST* 13 35
35 13 33PCI_TCK	B2	A2	
	B3	A3	33PCI_TMS 13 35
TDO 33PCI_TDO	B4	A4	TDI
END OF PCI SCAN CHAIN	B5	A5	
	B6	A6	33SLOT1_INT* 13 27 35
35 27 13 33SLOT1_INT*	B7	A7	
	B8	A8	
PRSNT1	B9	A9	RESERVED
RESERVED	B10	A10	
PRSNT2	B11	A11	RESERVED
	B12	A12	
	B13	A13	
RESERVED	B14	A14	3_3V_SLEEP 3 6 7 8 10 11 13 14 19 20 24 27 31 35 36 37 39 41
	B15	A15	MAIN_RESET* 9 12 13 14 33 36 41
18 33SLOT1_CLK	B16	A16	
	B17	A17	33SLOT1_GNT* 9 12
35 12 9 33SLOT1_REQ*	B18	A18	
	B19	A19	PME* 9 13 14 19 20 27 36 38
41 24 31 15 13 12 9 33PCI_AD<31>	B20	A20	41 24 15 13 12 9 33PCI_AD<30> 30
29 33PCI_AD<29>	B21	A21	
	B22	A22	41 24 15 13 12 9 33PCI_AD<28> 28
41 24 27 15 13 12 9 33PCI_AD<27>	B23	A23	41 24 15 13 12 9 33PCI_AD<26> 26
25 33PCI_AD<25>	B24	A24	
	B25	A25	41 24 15 13 12 9 33PCI_AD<24> 24
15 13 12 9 33PCI_CBE<3>*	B26	A26	33SLOT1_IDSEL
41 24 23 33PCI_AD<23>	B27	A27	
	B28	A28	41 24 15 13 12 9 33PCI_AD<22> 22
41 24 21 15 13 12 9 33PCI_AD<21>	B29	A29	41 24 15 13 12 9 33PCI_AD<20> 20
19 33PCI_AD<19>	B30	A30	
	B31	A31	41 24 15 13 12 9 33PCI_AD<18> 18
41 24 17 15 13 12 9 33PCI_AD<17>	B32	A32	41 24 15 13 12 9 33PCI_AD<16> 16
15 13 12 9 33PCI_CBE<2>*	B33	A33	
41 24	B34	A34	33PCI_FRAME* 9 12 13 15 24 35 41
24 15 13 12 9 33PCI_IRDY* 41 35	B35	A35	
24 15 13 12 9 33PCI_DEVSEL* 41 35	B36	A36	33PCI_TRDY* 9 12 13 15 24 35 41
	B37	A37	
	B38	A38	33PCI_STOP* 9 12 13 15 24 35 41
35 15 13 33PCI_LOCK*	B39	A39	
41 35 15 13 33PCI_PERR*	B40	A40	33PCI_SDONE 13 35
	B41	A41	33PCI_SBO* 13 35
41 35 15 13 33PCI_SERR*	B42	A42	
	B43	A43	33PCI_PAR 9 12 13 15 24 41
15 13 12 9 33PCI_CBE<1>*	B44	A44	41 24 15 13 12 9 33PCI_AD<15> 15
14 41 24 33PCI_AD<14>	B45	A45	
	B46	A46	41 24 15 13 12 9 33PCI_AD<13> 13
41 24 12 15 13 12 9 33PCI_AD<12>	B47	A47	41 24 15 13 12 9 33PCI_AD<11> 11
10 33PCI_AD<10>	B48	A48	
	B49	A49	41 24 15 13 12 9 33PCI_AD<9> 9
41 24 8 15 13 12 9 33PCI_AD<8>	B52	A52	33PCI_CBE<0>* 9 12 13 15 24 41
7 33PCI_AD<7>	B53	A53	
	B54	A54	41 24 15 13 12 9 33PCI_AD<6> 6
41 24 5 15 13 12 9 33PCI_AD<5>	B55	A55	41 24 15 13 12 9 33PCI_AD<4> 4
3 33PCI_AD<3>	B56	A56	
	B57	A57	41 24 15 13 12 9 33PCI_AD<2> 2
41 24 1 15 13 12 9 33PCI_AD<1>	B58	A58	41 24 15 13 12 9 33PCI_AD<0> 0
	B59	A59	
35 15 13 12 9 33PCI_ACK64*	B60	A60	33PCI_REQ64* 9 12 13 15 35
	B61	A61	
	B62	A62	
RESERVED	B63	A63	
	B64	A64	33PCI_CBE<7>* 9 35 12 13 15
15 13 12 9 33PCI_CBE<6>*	B65	A65	33PCI_CBE<5>* 9 35 12 13 15
15 13 12 9 33PCI_CBE<4>* 35	B66	A66	
	B67	A67	33PCI_PAR64 9 35 12 13 15
63 35 15 13 12 9 33PCI_AD<63>	B68	A68	35 15 13 12 9 33PCI_AD<62> 62
61 35 15 13 12 9 33PCI_AD<61>	B69	A69	
	B70	A70	35 15 13 12 9 33PCI_AD<60> 60
59 35 15 13 12 9 33PCI_AD<59>	B71	A71	35 15 13 12 9 33PCI_AD<58> 58
57 35 15 13 12 9 33PCI_AD<57>	B72	A72	
	B73	A73	35 15 13 12 9 33PCI_AD<56> 56
55 35 15 13 12 9 33PCI_AD<55>	B74	A74	35 15 13 12 9 33PCI_AD<54> 54
53 35 15 13 12 9 33PCI_AD<53>	B75	A75	
	B76	A76	35 15 13 12 9 33PCI_AD<52> 52
51 35 15 13 12 9 33PCI_AD<51>	B77	A77	35 15 13 12 9 33PCI_AD<50> 50
49 35 15 13 12 9 33PCI_AD<49>	B78	A78	
	B79	A79	35 15 13 12 9 33PCI_AD<48> 48
47 35 15 13 12 9 33PCI_AD<47>	B80	A80	35 15 13 12 9 33PCI_AD<46> 46
45 35 15 13 12 9 33PCI_AD<45>	B81	A81	
	B82	A82	35 15 13 12 9 33PCI_AD<44> 44
43 35 15 13 12 9 33PCI_AD<43>	B83	A83	35 15 13 12 9 33PCI_AD<42> 42
41 35 15 13 12 9 33PCI_AD<41>	B84	A84	
	B85	A85	35 15 13 12 9 33PCI_AD<40> 40
39 35 15 13 12 9 33PCI_AD<39>	B86	A86	35 15 13 12 9 33PCI_AD<38> 38
37 35 15 13 12 9 33PCI_AD<37>	B87	A87	
	B88	A88	35 15 13 12 9 33PCI_AD<36> 36
35 35 15 13 12 9 33PCI_AD<35>	B89	A89	35 15 13 12 9 33PCI_AD<34> 34
33 35 15 13 12 9 33PCI_AD<33>	B90	A90	
	B91	A91	35 15 13 12 9 33PCI_AD<32> 32
RESERVED	B92	A92	RESERVED
RESERVED	B93	A93	
	B94	A94	RESERVED

R83 22 5% 1/16W MF 402

SLOT C

J11 TH

+3.3V +5V +3.3V +12V -12V +5V +3.3V

NO STUFF
R43 10K 5% 1/16W MF 402

	B1	A1	33PCI_TRST* 13 35
35 13 33PCI_TCK	B2	A2	
	B3	A3	33PCI_TMS 13 35
TDO 33PCI_TDO_2	B4	A4	TDI
	B5	A5	
	B6	A6	33SLOT2_INT* 13 27 35
35 27 13 33SLOT2_INT*	B7	A7	
	B8	A8	
PRSNT1	B9	A9	RESERVED
RESERVED	B10	A10	
PRSNT2	B11	A11	RESERVED
	B12	A12	
	B13	A13	
RESERVED	B14	A14	3_3V_SLEEP 3 6 7 8 10 11 13 14 19 20 24 27 31 35 36 37 39 41
	B15	A15	MAIN_RESET* 9 12 13 14 33 36 41
18 33SLOT2_CLK	B16	A16	
	B17	A17	33SLOT2_GNT* 9 12
35 12 9 33SLOT2_REQ*	B18	A18	
	B19	A19	PME* 9 13 14 19 20 27 36 38
41 31 24 15 13 12 9 33PCI_AD<31>	B20	A20	41 24 15 13 12 9 33PCI_AD<30> 30
29 33PCI_AD<29>	B21	A21	
	B22	A22	41 24 15 13 12 9 33PCI_AD<28> 28
41 27 24 15 13 12 9 33PCI_AD<27>	B23	A23	41 24 15 13 12 9 33PCI_AD<26> 26
25 33PCI_AD<25>	B24	A24	
	B25	A25	41 24 15 13 12 9 33PCI_AD<24> 24
24 15 13 12 9 33PCI_CBE<3>*	B26	A26	33SLOT2_IDSEL
41 23 33PCI_AD<23>	B27	A27	
	B28	A28	41 24 15 13 12 9 33PCI_AD<22> 22
41 21 24 15 13 12 9 33PCI_AD<21>	B29	A29	41 24 15 13 12 9 33PCI_AD<20> 20
19 33PCI_AD<19>	B30	A30	
	B31	A31	41 24 15 13 12 9 33PCI_AD<18> 18
41 17 24 15 13 12 9 33PCI_AD<17>	B32	A32	41 24 15 13 12 9 33PCI_AD<16> 16
24 15 13 12 9 33PCI_CBE<2>* 41	B33	A33	
	B34	A34	33PCI_FRAME* 9 12 13 15 24 35 41
35 24 15 13 12 9 33PCI_IRDY* 41	B35	A35	
35 24 15 13 12 9 33PCI_DEVSEL* 41	B36	A36	33PCI_TRDY* 9 12 13 15 24 35 41
	B37	A37	
	B38	A38	33PCI_STOP* 9 12 13 15 24 35 41
35 15 13 33PCI_LOCK*	B39	A39	
41 35 15 13 33PCI_PERR*	B40	A40	33PCI_SDONE 13 35
	B41	A41	33PCI_SBO* 13 35
41 35 15 13 33PCI_SERR*	B42	A42	
	B43	A43	33PCI_PAR 9 12 13 15 24 41
24 15 13 12 9 33PCI_CBE<1>* 41	B44	A44	41 24 15 13 12 9 33PCI_AD<15> 15
14 33PCI_AD<14>	B45	A45	
	B46	A46	41 24 15 13 12 9 33PCI_AD<13> 13
12 41 24 15 13 12 9 33PCI_AD<12>	B47	A47	41 24 15 13 12 9 33PCI_AD<11> 11
10 33PCI_AD<10>	B48	A48	
	B49	A49	41 24 15 13 12 9 33PCI_AD<9> 9
8 41 24 15 13 12 9 33PCI_AD<8>	B52	A52	33PCI_CBE<0>* 9 41 12 13 15 24
7 41 24 15 13 12 9 33PCI_AD<7>	B53	A53	
	B54	A54	41 24 15 13 12 9 33PCI_AD<6> 6
5 41 24 15 13 12 9 33PCI_AD<5>	B55	A55	41 24 15 13 12 9 33PCI_AD<4> 4
3 41 24 15 13 12 9 33PCI_AD<3>	B56	A56	
	B57	A57	41 24 15 13 12 9 33PCI_AD<2> 2
1 41 24 15 13 12 9 33PCI_AD<1>	B58	A58	41 24 15 13 12 9 33PCI_AD<0> 0
	B59	A59	
35 15 13 12 9 33PCI_ACK64*	B60	A60	33PCI_REQ64* 9 12 13 15 35
	B61	A61	
	B62	A62	
RESERVED	B63	A63	
	B64	A64	33PCI_CBE<7>* 9 12 13 15 35
35 15 13 12 9 33PCI_CBE<6>*	B65	A65	33PCI_CBE<5>* 9 12 13 15 35
35 15 13 12 9 33PCI_CBE<4>*	B66	A66	
	B67	A67	33PCI_PAR64 9 12 13 15 35
63 35 15 13 12 9 33PCI_AD<63>	B68	A68	35 15 13 12 9 33PCI_AD<62> 62
61 35 15 13 12 9 33PCI_AD<61>	B69	A69	
	B70	A70	35 15 13 12 9 33PCI_AD<60> 60
59 35 15 13 12 9 33PCI_AD<59>	B71	A71	35 15 13 12 9 33PCI_AD<58> 58
57 35 15 13 12 9 33PCI_AD<57>	B72	A72	
	B73	A73	35 15 13 12 9 33PCI_AD<56> 56
55 35 15 13 12 9 33PCI_AD<55>	B74	A74	35 15 13 12 9 33PCI_AD<54> 54
53 35 15 13 12 9 33PCI_AD<53>	B75	A75	
	B76	A76	35 15 13 12 9 33PCI_AD<52> 52
51 35 15 13 12 9 33PCI_AD<51>	B77	A77	35 15 13 12 9 33PCI_AD<50> 50
49 35 15 13 12 9 33PCI_AD<49>	B78	A78	
	B79	A79	35 15 13 12 9 33PCI_AD<48> 48
47 35 15 13 12 9 33PCI_AD<47>	B80	A80	35 15 13 12 9 33PCI_AD<46> 46
45 35 15 13 12 9 33PCI_AD<45>	B81	A81	
	B82	A82	35 15 13 12 9 33PCI_AD<44> 44
43 35 15 13 12 9 33PCI_AD<43>	B83	A83	35 15 13 12 9 33PCI_AD<42> 42
41 35 15 13 12 9 33PCI_AD<41>	B84	A84	
	B85	A85	35 15 13 12 9 33PCI_AD<40> 40
39 35 15 13 12 9 33PCI_AD<39>	B86	A86	35 15 13 12 9 33PCI_AD<38> 38
37 35 15 13 12 9 33PCI_AD<37>	B87	A87	
	B88	A88	35 15 13 12 9 33PCI_AD<36> 36
35 35 15 13 12 9 33PCI_AD<35>	B89	A89	35 15 13 12 9 33PCI_AD<34> 34
33 35 15 13 12 9 33PCI_AD<33>	B90	A90	
	B91	A91	35 15 13 12 9 33PCI_AD<32> 32
RESERVED	B92	A92	RESERVED
RESERVED	B93	A93	
	B94	A94	RESERVED

R82 22 5% 1/16W MF 402

SLOT D

J10 TH

+3.3V +5V +3.3V +12V -12V +5V +3.3V

NO STUFF
R41 10K 5% 1/16W MF 402

	B1	A1	33PCI_TRST* 13 35
35 13 33PCI_TCK	B2	A2	
	B3	A3	33PCI_TMS 13 35
TDO 33PCI_TDO_3	B4	A4	START OF PCI SCAN CHAIN 33PCI_TDI
	B5	A5	
	B6	A6	33SLOT3_INT* 13 27 35
35 27 13 33SLOT3_INT*	B7	A7	
	B8	A8	
PRSNT1	B9	A9	RESERVED
RESERVED	B10	A10	
PRSNT2	B11	A11	RESERVED
	B12	A12	
	B13	A13	
RESERVED	B14	A14	3_3V_SLEEP 3 6 7 8 10 11 13 14 19 20 24 27 31 35 36 37 39 41
	B15	A15	MAIN_RESET* 9 12 13 14 33 36 41
18 33SLOT3_CLK	B16	A16	
	B17	A17	33SLOT3_GNT* 9 12
35 12 9 33SLOT3_REQ*	B18	A18	
	B19	A19	PME* 9 13 14 19 20 27 36 38
41 31 24 15 13 12 9 33PCI_AD<31>	B20	A20	41 24 15 13 12 9 33PCI_AD<30> 30
29 33PCI_AD<29>	B21	A21	
	B22	A22	41 24 15 13 12 9 33PCI_AD<28> 28
41 27 24 15 13 12 9 33PCI_AD<27>	B23	A23	41 24 15 13 12 9 33PCI_AD<26> 26
25 33PCI_AD<25>	B24	A24	
	B25	A25	41 24 15 13 12 9 33PCI_AD<24> 24
24 15 13 12 9 33PCI_CBE<3>*	B26	A26	33SLOT3_IDSEL
41 23 33PCI_AD<23>	B27	A27	
	B28	A28	41 24 15 13 12 9 33PCI_AD<22> 22
41 21 24 15 13 12 9 33PCI_AD<21>	B29	A29	41 24 15 13 12 9 33PCI_AD<20> 20
19 33PCI_AD<19>	B30	A30	
	B31	A31	41 24 15 13 12 9 33PCI_AD<18> 18
41 17 24 15 13 12 9 33PCI_AD<17>	B32	A32	41 24 15 13 12 9 33PCI_AD<16> 16
24 15 13 12 9 33PCI_CBE<2>* 41	B33	A33	
	B34	A34	33PCI_FRAME* 9 12 13 15 24 35 41
35 24 15 13 12 9 33PCI_IRDY* 41	B35	A35	
35 24 15 13 12 9 33PCI_DEVSEL* 41	B36	A36	33PCI_TRDY* 9 12 13 15 24 35 41
	B37	A37	
	B38	A38	33PCI_STOP* 9 12 13 15 24 35 41
35 15 13 33PCI_LOCK*	B39	A39	
41 35 15 13 33PCI_PERR*	B40	A40	33PCI_SDONE 13 35
	B41	A41	33PCI_SBO* 13 35
41 35 15 13 33PCI_SERR*	B42	A42	
	B43	A43	33PCI_PAR 9 12 13 15 24 41
24 15 13 12 9 33PCI_CBE<1>* 41	B44	A44	41 24 15 13 12 9 33PCI_AD<15> 15
14 33PCI_AD<14>	B45	A45	
	B46	A46	41 24 15 13 12 9 33PCI_AD<13> 13
12 41 24 15 13 12 9 33PCI_AD<12>	B47	A47	41 24 15 13 12 9 33PCI_AD<11> 11
10 33PCI_AD<10>	B48	A48	
	B49	A49	41 24 15 13 12 9 33PCI_AD<9> 9
8 41 24 15 13 12 9 33PCI_AD<8>	B52	A52	33PCI_CBE<0>* 9 12 13 15 24 41
7 41 24 15 13 12 9 33PCI_AD<7>	B53	A53	
	B54	A54	41 24 15 13 12 9 33PCI_AD<6> 6
5 41 24 15 13 12 9 33PCI_AD<5>	B55	A55	41 24 15 13 12 9 33PCI_AD<4> 4
3 41 24 15 13 12 9 33PCI_AD<3>	B56	A56	
	B57	A57	41 24 15 13 12 9 33PCI_AD<2> 2
1 41 24 15 13 12 9 33PCI_AD<1>	B58	A58	41 24 15 13 12 9 33PCI_AD<0> 0
	B59	A59	
35 15 13 12 9 33PCI_ACK64*	B60	A60	33PCI_REQ64* 9 12 13 15 35
	B61	A61	
	B62	A62	
RESERVED	B63	A63	
	B64	A64	33PCI_CBE<7>* 9 12 13 15 35
35 15 13 12 9 33PCI_CBE<6>*	B65	A65	33PCI_CBE<5>* 9 12 13 15 35
35 15 13 12 9 33PCI_CBE<4>*	B66	A66	
	B67	A67	33PCI_PAR64 9 12 13 15 35
63 35 15 13 12 9 33PCI_AD<63>	B68	A68	35 15 13 12 9 33PCI_AD<62> 62
61 35 15 13 12 9 33PCI_AD<61>	B69	A69	
	B70	A70	35 15 13 12 9 33PCI_AD<60> 60
59 35 15 13 12 9 33PCI_AD<59>	B71	A71	35 15 13 12 9 33PCI_AD<58> 58
57 35 15 13 12 9 33PCI_AD<57>	B72	A72	
	B73	A73	35 15 13 12 9 33PCI_AD<56> 56
55 35 15 13 12 9 33PCI_AD<55>	B74	A74	35 15 13 12 9 33PCI_AD<54> 54
53 35 15 13 12 9 33PCI_AD<53>	B75	A75	
	B76	A76	35 15 13 12 9 33PCI_AD<52> 52
51 35 15 13 12 9 33PCI_AD<51>	B77	A77	35 15 13 12 9 33PCI_AD<50> 50
49 35 15 13 12 9 33PCI_AD<49>	B78	A78	
	B79	A79	35 15 13 12 9 33PCI_AD<48> 48
47 35 15 13 12 9 33PCI_AD<47>	B80	A80	35 15 13 12 9 33PCI_AD<46> 46
45 35 15 13 12 9 33PCI_AD<45>	B81	A81	
	B82	A82	35 15 13 12 9 33PCI_AD<44> 44
43 35 15 13 12 9 33PCI_AD<43>	B83	A83	35 15 13 12 9 33PCI_AD<42> 42
41 35 15 13 12 9 33PCI_AD<41>	B84	A84	
	B85	A85	35 15 13 12 9 33PCI_AD<40> 40
39 35 15 13 12 9 33PCI_AD<39>	B86	A86	35 15 13 12 9 33PCI_AD<38> 38
37 35 15 13 12 9 33PCI_AD<37>	B87	A87	
	B88	A88	35 15 13 12 9 33PCI_AD<36> 36
35 35 15 13 12 9 33PCI_AD<35>	B89	A89	35 15 13 12 9 33PCI_AD<34> 34
33 35 15 13 12 9 33PCI_AD<33>	B90	A90	
	B91	A91	35 15 13 12 9 33PCI_AD<32> 32
RESERVED	B92	A92	RESERVED
RESERVED	B93	A93	
	B94	A94	RESERVED

R81 22 5% 1/16W MF 402

33 MHZ PCI SLOTS

CR-14

SLOT A

28V_TRICKLE

R175 2.7K 5% 1/2W FS 2010

DS1 GREEN SM

28V_GC

L15 63-OHM SM

J9 7H

28V_GND

P-ST-ES00306

C42 100UF 20% 6.3V ELEC SM

C43 100UF 20% 6.3V ELEC SM NO STUFF

PLACE NEAR AGP SLOT

J16 TH-145376

ALL POWER BELOW THIS LINE = VDDQ (I/O RAIL)

OUTPUT FROM RESISTOR DIVIDER

INPUT TO UNI-N

R148 470 5% 1/16W MF 603 — PWR_SWITCH* 29 36 39

R149 0 5% 1/16W MF 402 — DISPLAY_LED 39

AGP_IO_RAIL SUPPLY

Q3 MTD15N06V SM

R14 10K 5% 1/16W MF 402

AGP_IO_RAIL 10 14 19 MIN_LINE_WIDTH=25

C69 150UF 20% 6.3V TANT SMD NEAR UNI-N

C70 150UF 20% 6.3V TANT SMD NEAR AGP SLOT

U4 TLV431A SOT

C59 0.01UF 20% 50V CERM 402 NO STUFF

R15 1.07K 1% 1/16W MF 603

R16 4.99K 1% 1/16W MF 603

Q11 2N7002 SM

FLOAT/HIGH = 3.3V VDDQ
LOW = 1.5V VDDQ

AGP2X CAN BE AT 3.3V OR 1.5V
AGP4X HAS TO BE AT 1.5V

VREF GENERATION

C71 470PF 10% 50V CERM 603

R141 4.99K 1% 1/16W MF 603 — AGP 2X UNI-N VREF

R142 3.32K 1% 1/16W MF 603

Q23 2N7002 SM

C100 0.01UF 402

R17 4.99K 1% 1/16W MF 603

R30 4.99K 1% 1/16W MF 603

R32 82.5 1% 1/16W MF 603 — AGP 4X AGP CARD VREF

R34 82.5 1% 1/16W MF 603

C72 470PF 10% 50V CERM 603

AGP_VREF_CG

C347 0.01UF 402

C359 0.01UF 402

C368 0.01UF 402

SPACE OUT EVENLY UNDER CONNECTOR

FOR IMAGE CURRENT RETURN

C346 0.01UF 402

C360 0.01UF 402

C369 0.01UF 402

R226 4.7K 5% 1/16W MF 603 — AGP_INT*

R228 4.7K 5% 1/16W MF 603 — AGP_TYPEDET*

RP114 4.7K 5% 1/16W SM — AGP_REQ*, AGP_RBF*, AGP_PIPE*, AGP_WBF*

RP39 4.7K 5% 1/16W SM — AGP_SB_STB, AGP_SB_STB*

RP38 4.7K 5% 1/16W SM — AGP_IRDY*, AGP_FRAME*, AGP_DEVSEL*, AGP_TRDY*

RP65 4.7K 5% 1/16W SM — AGP_STOP*, AGP_PERR*, AGP_SERR*

R407 4.99K 1% 1/16W MF 603 — AGP_GNT*

R134 470 1% 1/16W MF 603 — AGP_AD_STB0

TERMINATION TO REDUCE CROSSTALK
INDUCED BY RINGING DATA LINES

R133 56.2 1% 1/16W MF 402 NO STUFF — AGP_TERM0

C87 33PF 10% 50V CERM 603 NO STUFF

R106 470 1% 1/16W MF 603 NO STUFF — AGP_AD_STB1

R107 56.2 1% 1/16W MF 402 — AGP_TERM1

C67 33PF 10% 50V CERM 603 NO STUFF

R119 470 1% 1/16W MF 603 — AGP_AD_STB0*

R120 470 1% 1/16W MF 603 — AGP_AD_STB1*

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-0997	01
SCALE: NONE	SHT 14 OF 47	

AGP SLOT / VREF / IO SUPPLY

CR-15

33PCI_FRAME*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 35 41
33PCI_TRDY*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 35 41
33PCI_IRDY*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 35 41
33PCI_STOP*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 35 41
33PCI_LOCK*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	13 35
33PCI_DEVSEL*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 35 41
33PCI_REQ64*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_ACK64*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<0>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<1>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<2>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<3>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<4>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<5>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<6>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<7>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<8>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<9>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<10>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<11>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<12>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<13>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<14>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<15>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
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33PCI_AD<18>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<19>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<20>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<21>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<22>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
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33PCI_AD<25>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<26>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<27>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<28>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<29>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<30>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_AD<31>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_PAR	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_CBE<0>*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_CBE<1>*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_CBE<2>*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_CBE<3>*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 24 41
33PCI_PERR*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	13 35 41
33PCI_SERR*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	13 35 41
33PCI_AD<32>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<33>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
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33PCI_AD<38>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
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33PCI_AD<41>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<42>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<43>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<44>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<45>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<46>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<47>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<48>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<49>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<50>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<51>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<52>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<53>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<54>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<55>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<56>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<57>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<58>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<59>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<60>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<61>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<62>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_AD<63>	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_PAR64	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_CBE<4>*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_CBE<5>*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_CBE<6>*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35
33PCI_CBE<7>*	RATSNEST_SCHEDULE=MIN_DAISY_CHAIN	STUB_LENGTH=1500	DELAY_RULE=:::130%	9 12 13 35

APPLE COMPUTER INC.

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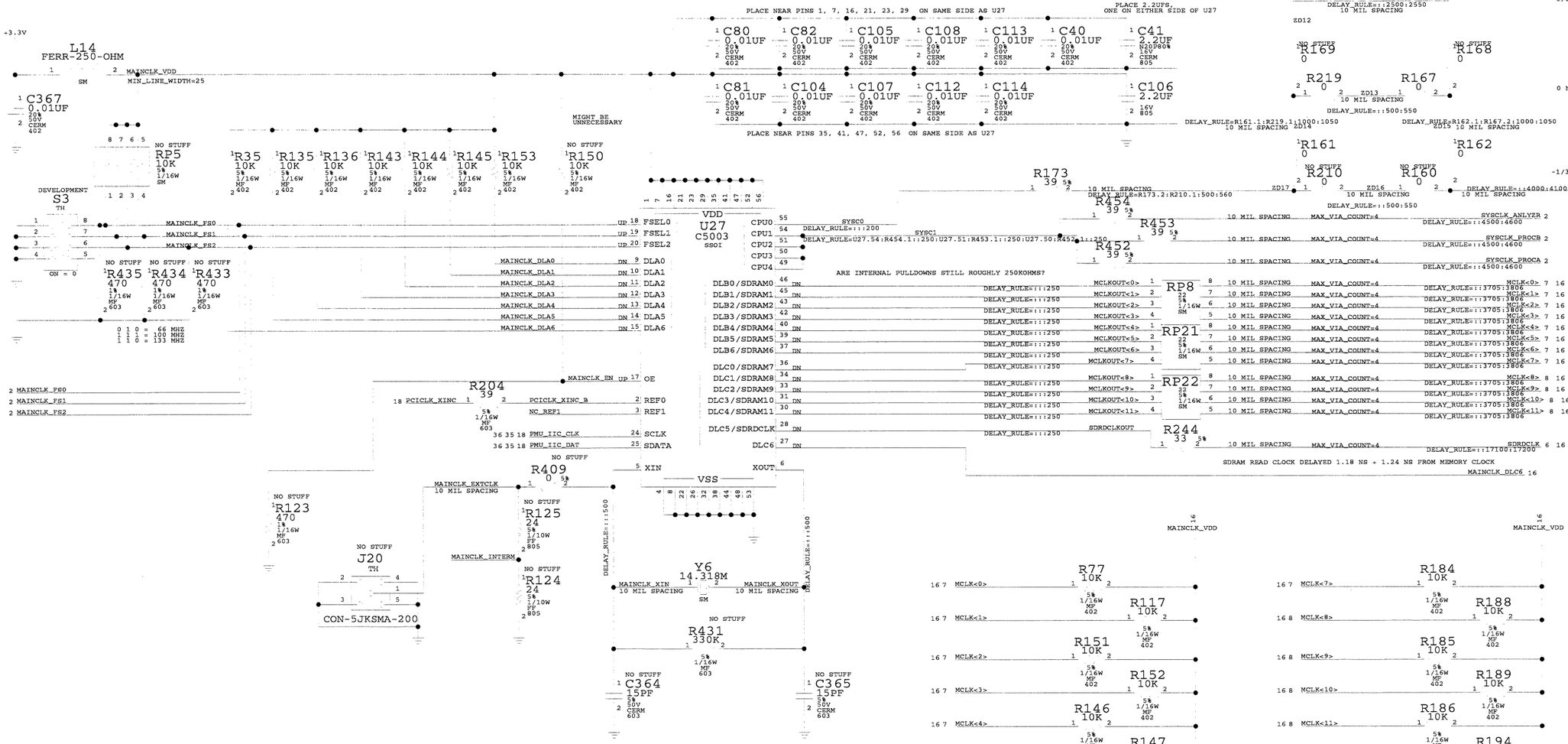
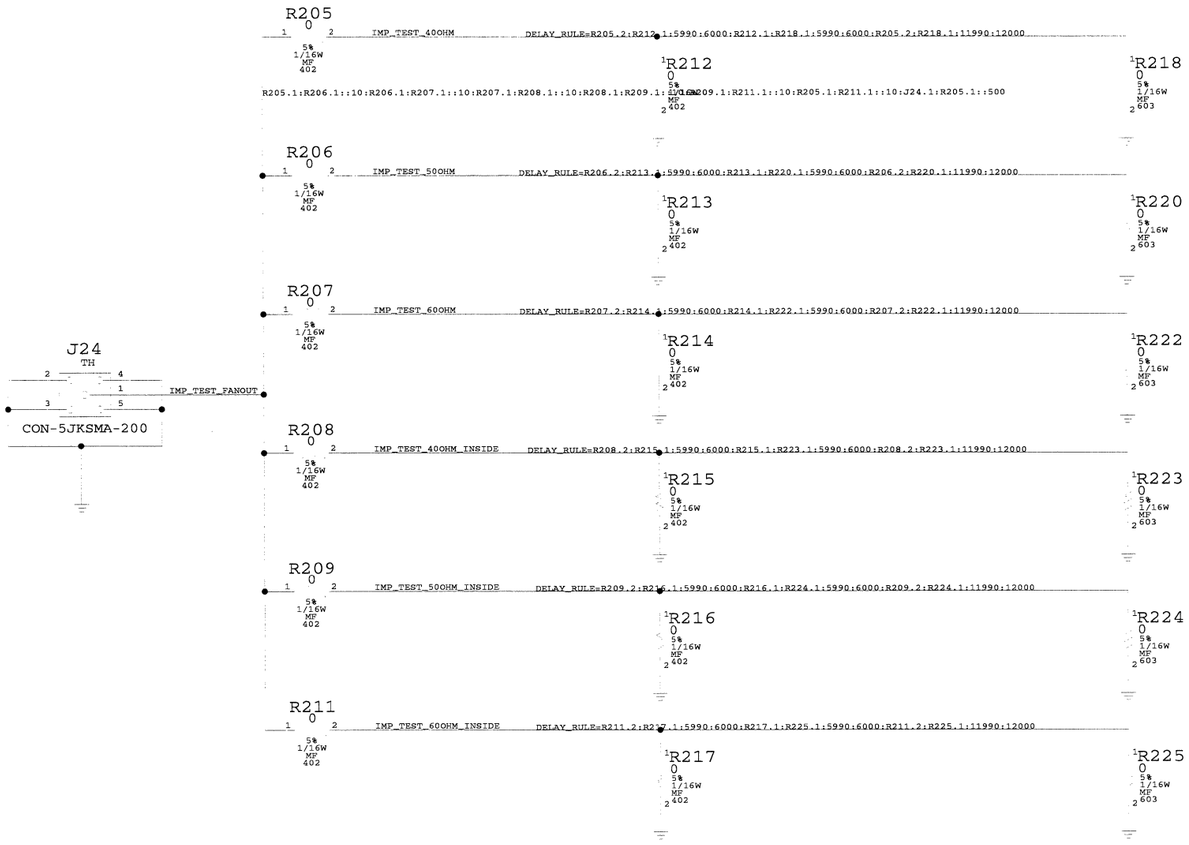
SCALE: NONE	SHT 15 OF 47	

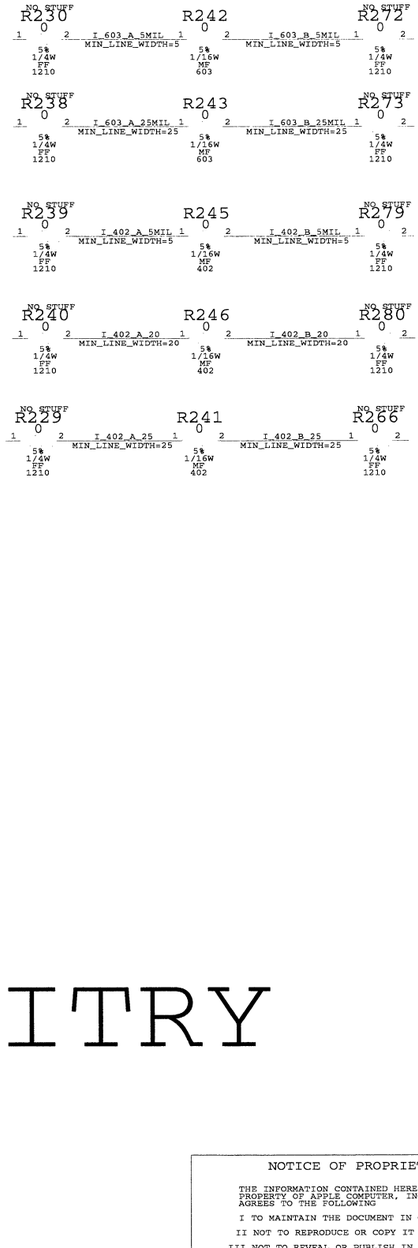
PULLUP/PULLDOWN PHILOSOPHY: OPPOSITE OF INTERNAL



MASTER CLOCK GENERATION

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-0997	01
	SCALE: NONE	SHT 16 OF 47	

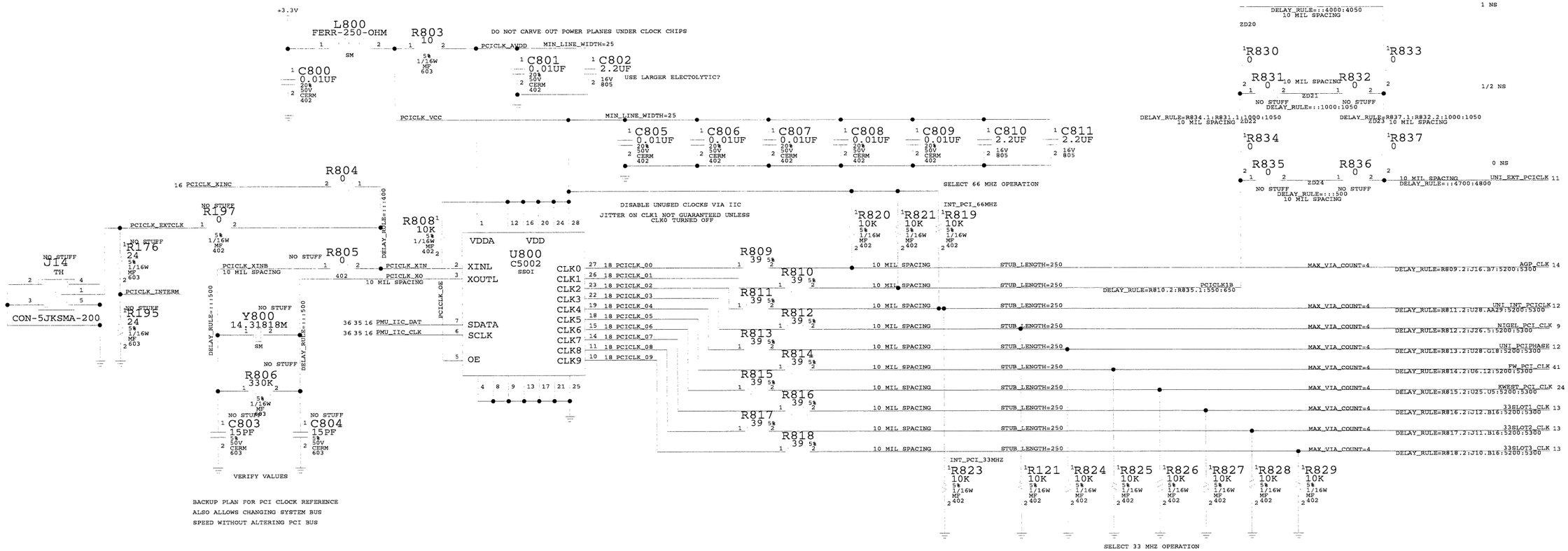




IMPEDANCE TEST CIRCUITRY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-0997	01
SCALE NONE	SHT 17 OF 47	

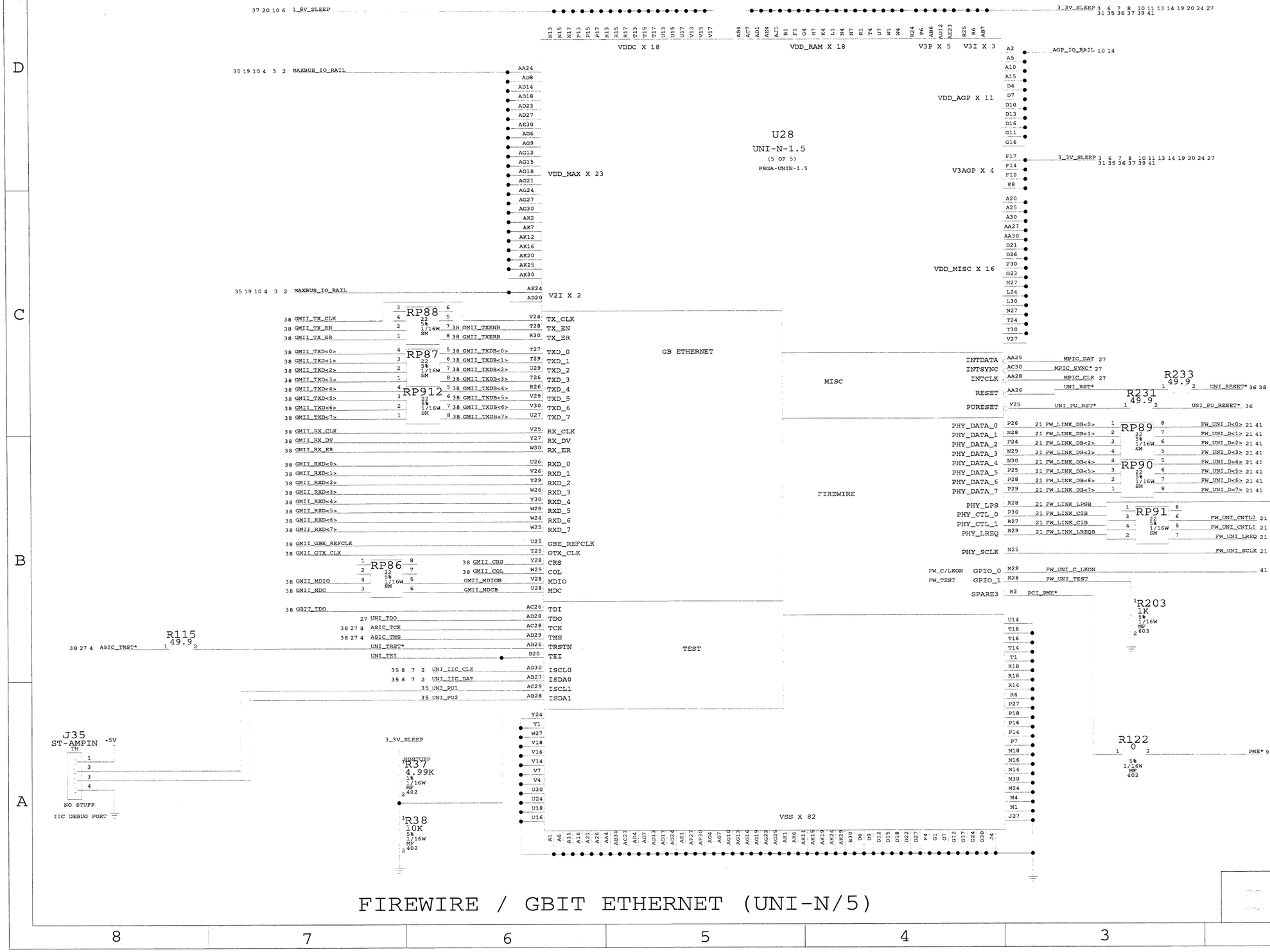


PCICLK_00	10 MIL SPACING	DELAY_RULE=::250	18
PCICLK_01	10 MIL SPACING	DELAY_RULE=::250	18
PCICLK_02	10 MIL SPACING	DELAY_RULE=::250	18
PCICLK_03	10 MIL SPACING	DELAY_RULE=::250	18
PCICLK_04	10 MIL SPACING	DELAY_RULE=::250	18
PCICLK_05	10 MIL SPACING	DELAY_RULE=::250	18
PCICLK_06	10 MIL SPACING	DELAY_RULE=::250	18
PCICLK_07	10 MIL SPACING	DELAY_RULE=::250	18
PCICLK_08	10 MIL SPACING	DELAY_RULE=::250	18
PCICLK_09	10 MIL SPACING	DELAY_RULE=::250	18

66 MHZ PCI CLOCKS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-0997	01
SCALE: NONE	SHT 18	OF 47



FIREWIRE / GBIT ETHERNET (UNI-N/5)

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-0997	01
	SCALE NONE	SHT 19 OF 47	

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MODE	Iovdd (mA)	Idvdd (mA)	Iavdd (mA)	Ilvdd (mA)	ITotl (mA)	PTotl (mW)
1000BaseT (rx/tx)	64.3	577.5	756.8	282.3	1681	4258
100BaseTx (rx/tx)	29.5	470.4	366.2	64.6	931	2420
10BaseT (rx/tx)	18.6	279.5	184.9	24.2	507	1329
10BaseT WOL (rx)	18.4	10.8	108.6	2.5	140	382

20 GBIT_1_8V

PLACE THESE CAPS AS CLOSE AS POSSIBLE TO THE L_VDD PINS.

EN_GBIT C920 0.001UF 20% 50V CERM 603
EN_GBIT C922 0.001UF 20% 50V CERM 603
EN_GBIT C924 0.001UF 20% 50V CERM 603
EN_GBIT C926 0.001UF 20% 50V CERM 603
EN_GBIT C921 0.01UF 20% 50V CERM 402
EN_GBIT C923 0.01UF 20% 50V CERM 402
EN_GBIT C925 0.01UF 20% 50V CERM 402
EN_GBIT C927 0.01UF 20% 50V CERM 402
EN_GBIT C120 0.1UF N20P80% 16V CERM 603
EN_GBIT C121 0.1UF N20P80% 16V CERM 603
EN_GBIT C149 10UF N20P80% 16V CERM 1210

20 GBIT_2_5V

PLACE THESE CAPS AS CLOSE AS POSSIBLE TO THE D_VDD PINS.

EN_GBIT C900 0.001UF 20% 50V CERM 603
EN_GBIT C901 0.001UF 20% 50V CERM 603
EN_GBIT C902 0.001UF 20% 50V CERM 603
EN_GBIT C903 0.001UF 20% 50V CERM 603
EN_GBIT C904 0.001UF 20% 50V CERM 603
EN_GBIT C905 0.001UF 20% 50V CERM 603
EN_GBIT C906 0.01UF 20% 50V CERM 402
EN_GBIT C907 0.01UF 20% 50V CERM 402
EN_GBIT C908 0.01UF 20% 50V CERM 402
EN_GBIT C909 0.01UF 20% 50V CERM 402
EN_GBIT C916 0.01UF 20% 50V CERM 402
EN_GBIT C917 0.01UF 20% 50V CERM 402
EN_GBIT C918 0.01UF 20% 50V CERM 402
EN_GBIT C919 0.01UF 20% 50V CERM 402
EN_GBIT C932 0.1UF N20P80% 16V CERM 603
EN_GBIT C933 0.1UF N20P80% 16V CERM 603
EN_GBIT C152 10UF N20P80% 16V CERM 1210

20 38 40 GBIT_3_3V

PLACE THESE CAPS AS CLOSE AS POSSIBLE TO THE O_VDD/ADC_VDD PINS.

EN_GBIT C910 0.001UF 20% 50V CERM 603
EN_GBIT C911 0.001UF 20% 50V CERM 603
EN_GBIT C912 0.001UF 20% 50V CERM 603
EN_GBIT C913 0.001UF 20% 50V CERM 603
EN_GBIT C914 0.01UF 20% 50V CERM 402
EN_GBIT C915 0.01UF 20% 50V CERM 402
EN_GBIT C934 0.1UF N20P80% 16V CERM 603
EN_GBIT C935 0.1UF N20P80% 16V CERM 603
EN_GBIT C134 10UF N20P80% 16V CERM 1210

20 GBIT_2_5V
20 38 40 GBIT_3_3V
EN_GBIT U900 BCM5401 (1 OF 2) PBGA

A4	O_VDD	L_VDD	A12
A10	O_VDD	L_VDD	A14
A17	O_VDD	L_VDD	A16
D18	O_VDD	L_VDD	B12
E18	O_VDD	L_VDD	B14
F18	O_VDD	L_VDD	B16
G18	O_VDD	L_VDD	C12
H18	O_VDD	L_VDD	C14
J18	O_VDD	L_VDD	D14
K18	O_VDD	L_VDD	U14
M18	O_VDD	L_VDD	V12
P18	O_VDD	L_VDD	V14
U18	O_VDD	L_VDD	W12
V20	O_VDD	L_VDD	W14
Y4	O_VDD	L_VDD	W16
Y17	O_VDD	L_VDD	Y12
		L_VDD	Y14
A18	O_GND	L_VDD	Y16
B5	O_GND		
B11	O_GND	ADC_VDD	B6
C18	O_GND	ADC_VDD	E2
E17	O_GND	ADC_VDD	E3
F17	O_GND	ADC_VDD	E4
G17	O_GND	ADC_VDD	G4
H17	O_GND	ADC_VDD	J3
J17	O_GND	ADC_VDD	J4
K17	O_GND	ADC_VDD	M3
M17	O_GND	ADC_VDD	M4
P17	O_GND	ADC_VDD	P4
V18	O_GND	ADC_VDD	T2
W5	O_GND	ADC_VDD	T3
Y18	O_GND	ADC_VDD	T4
A9	D_VDD		
B9	D_VDD	ADC_GND	B7
D8	D_VDD	ADC_GND	C2
F19	D_VDD	ADC_GND	C3
L17	D_VDD	ADC_GND	D2
N18	D_VDD	ADC_GND	D3
W7	D_VDD	ADC_GND	D4
W8	D_VDD	ADC_GND	D7
W9	D_VDD	ADC_GND	F2
W10	D_VDD	ADC_GND	F3
Y7	D_VDD	ADC_GND	F4
Y8	D_VDD	ADC_GND	G2
Y10	D_VDD	ADC_GND	G3
		ADC_GND	H2
A13	D_GND	ADC_GND	H3
A15	D_GND	ADC_GND	H4
B13	D_GND	ADC_GND	K2
B15	D_GND	ADC_GND	K3
C9	D_GND	ADC_GND	K4
C13	D_GND	ADC_GND	L2
C15	D_GND	ADC_GND	L3
D9	D_GND	ADC_GND	L4
D12	D_GND	ADC_GND	N2
D13	D_GND	ADC_GND	N3
D15	D_GND	ADC_GND	N4
F20	D_GND	ADC_GND	P2
N17	D_GND	ADC_GND	P3
U7	D_GND	ADC_GND	R2
U8	D_GND	ADC_GND	R3
U9	D_GND	ADC_GND	R4
U12	D_GND	ADC_GND	U2
U13	D_GND	ADC_GND	U3
U15	D_GND	ADC_GND	U4
V7	D_GND	ADC_GND	V2
V8	D_GND	ADC_GND	V3
V9	D_GND		
V13	D_GND	RDAC	L1
V15	D_GND	VREF	K1 NC
W13	D_GND		
Y13	D_GND	BIAS_VDD	J2
W15	D_GND	BIAS_VDD	M2
Y15	D_GND	DLL_VDD	A7

BCM5401_RDAC
EN_GBIT R952 1.24K 1% 1/16W MF 402
MIN_LINE_WIDTH=25
EN_GBIT R951 4.7 5% 1/16W MF 603
EN_GBIT C928 0.001UF 20% 50V CERM 603
GBIT_BIASVDD
GBIT_DLLVDD

PLACE ALL COMPONENTS ON GBIT_BIASVDD AT PIN J2/M2

PLACE ALL COMPONENTS ON GBIT_DLLVDD AT PIN A7

20 GBIT_2_5V
EN_GBIT L902 FERR-EMI-600-OHM SM
EN_GBIT C930 0.1UF N20P80% 16V CERM 603
EN_GBIT R196 2 5% 1/16W MF 603
EN_GBIT C61 1UF 10% 10V CERM 805

NEED 20HM ESR ACCORDING TO BROADCOM

3_3V_SLEEP
20 38 40 GBIT_3_3V
EN_GBIT R924 0 5% 1/16W
EN_GBIT R925 0 5% 1/16W
MIN_LINE_WIDTH=25

1_8V_SLEEP
6 10 19 37
20 GBIT_1_8V
EN_GBIT R926 0 5% 1/16W
EN_GBIT R927 0 5% 1/16W
MIN_LINE_WIDTH=25

20 38 40 GBIT_3_3V
5V_SLEEP
24 27 29 30 31 37
EN_GBIT R930 10 5% 1/16W MF 603
1 EN_GBIT
SENSE
VR900
CS5253
SM
VPWR VOUT
VCTRL VOUT
ADJ TAB
GBIT_5V
MIN_LINE_WIDTH=25
EN_GBIT R932 124 1% 1/16W MF 603
GBIT_REG_ADJ
MIN_LINE_WIDTH=25
GBIT_2_5V 20
MIN_LINE_WIDTH=25
2.51 - 2.63V
(REQUIREMENT IS 2.47 - 2.73)

300UF NEEDED FOR STABILITY

EN_GBIT C937 100UF 20% 6.3V ELEC SM
EN_GBIT C938 10UF N20P80% 16V CERM 1210
EN_GBIT C939 0.1UF N20P80% 16V CERM 603
EN_GBIT R933 130 1% 1/16W MF 603
EN_GBIT C940 330UF 20% 16V ELEC SM

20 38 40 GBIT_3_3V

DEVELOPMENT R941 124 1% 1/16W MF 603	DEVELOPMENT R942 124 1% 1/16W MF 603	DEVELOPMENT R943 124 1% 1/16W MF 603	DEVELOPMENT R944 124 1% 1/16W MF 603	DEVELOPMENT R945 124 1% 1/16W MF 603	DEVELOPMENT R946 124 1% 1/16W MF 603	NO STUFF R947 124 1% 1/16W MF 603	DEVELOPMENT R948 124 1% 1/16W MF 603	DEVELOPMENT R949 124 1% 1/16W MF 603
GBIT_LED1	GBIT_LED2	GBIT_LED3	GBIT_LED4	GBIT_LED5	GBIT_LED6	GBIT_LED7	GBIT_LED8	GBIT_LED9
DEVELOPMENT DS900 GREEN SM	DEVELOPMENT DS901 GREEN SM	DEVELOPMENT DS902 GREEN SM	DEVELOPMENT DS903 GREEN SM	DEVELOPMENT DS904 RED SM	DEVELOPMENT DS905 GREEN SM	DEVELOPMENT DS906 GREEN SM	DEVELOPMENT DS907 GREEN SM	DEVELOPMENT DS908 GREEN SM

38 GBIT_LINK10*
38 GBIT_LINK100*
38 GBIT_LINK1000*
38 GBIT_FDXLED*
38 GBIT_XMTLED*
38 GBIT_RCVLED*
38 GBIT_PHY_INT*
38 GBIT_SLAVE*
38 GBIT_QUALITY

EN_GBIT R950 0 5% 1/16W MF 402
PME*9 13 14 19 27 36 38

PLACE SILKSCREEN NEAR THE LEDS -SEE RICK

10/100/GBIT ETHERNET PHY POWER, DECOUPLING AND PULLUPS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-0997	01
SCALE: NONE	SHT 20 OF 47	

CR=21

41 21 FW_LINK_D<0> — RP11 22 (1–8) — FW_PHY_D<0> 21 22

41 21 FW_LINK_D<1> — RP11 22 (2–7) — FW_PHY_D<1> 21 22

41 21 FW_LINK_D<2> — RP11 22 (3–6) — FW_PHY_D<2> 21 22

41 21 FW_LINK_D<3> — RP11 22 (4–5) — FW_PHY_D<3> 21 22

41 21 FW_LINK_D<4> — RP12 22 (1–8) — FW_PHY_D<4> 21 22

41 21 FW_LINK_D<5> — RP12 22 (2–7) — FW_PHY_D<5> 21 22

41 21 FW_LINK_D<6> — RP12 22 (3–6) — FW_PHY_D<6> 21 22

41 21 FW_LINK_D<7> — RP12 22 (4–5) — FW_PHY_D<7> 21 22

41 21 FW_LINK_CNTL0 — R366 22 (1–2) — FW_PHY_CNTL0 21 22

41 21 FW_LINK_CNTL1 — R365 22 (1–2) — FW_PHY_CNTL1 21 22

41 21 FW_LINK_LREQ — R367 22 (1–2) — FW_PHY_LREQ 21 22

41 21 FW_LINK_SCLK — R371 22 (1–2) — FW_PHY_SCLK 21 22

All resistors: 5% 1/16W

SIMULATE LUCENT PHY
TO SEE IF THESE REQUIRED

27 FW_LINK_PD — R198 0 (1–2) — FW_PHY_PD 22

5% 1/16W MF 402

FW_PHY_RST* 22

41 FW_LINK_RST — R373 4.99K (1–2) — FW_PHY_RST — Q17 2N3904 SM (1=3, 2)

PROVIDE INVERSION AND ISOLATION FOR WHEN LINK UNPOWERED

FW_LINK_DB<0>	DELAY_RULE=::500:700	19
FW_LINK_DB<1>	DELAY_RULE=::500:700	19
FW_LINK_DB<2>	DELAY_RULE=::500:700	19
FW_LINK_DB<3>	DELAY_RULE=::400:600	19
FW_LINK_DB<4>	DELAY_RULE=::150:350	19
FW_LINK_DB<5>	DELAY_RULE=::150:350	19
FW_LINK_DB<6>	DELAY_RULE=::150:350	19
FW_LINK_DB<7>	DELAY_RULE=::150:350	19
FW_LINK_C0B	DELAY_RULE=::300:500	19
FW_LINK_C1B	DELAY_RULE=::300:500	19
FW_LINK_LREQB	DELAY_RULE=::300:500	19
FW_LINK_LPSB	DELAY_RULE=:::500	19
FW_LINK_I00	DELAY_RULE=:::500	

FW_UNI_D<0>	DELAY_RULE=::2100:3000	19 41
FW_UNI_D<1>	DELAY_RULE=::2100:3000	19 41
FW_UNI_D<2>	DELAY_RULE=::2100:3000	19 41
FW_UNI_D<3>	DELAY_RULE=::2100:3100	19 41
FW_UNI_D<4>	DELAY_RULE=::2250:3350	19 41
FW_UNI_D<5>	DELAY_RULE=::2250:3350	19 41
FW_UNI_D<6>	DELAY_RULE=::2250:3350	19 41
FW_UNI_D<7>	DELAY_RULE=::2250:3350	19 41
FW_UNI_CNTL0	DELAY_RULE=::2100:3300	19 41
FW_UNI_CNTL1	DELAY_RULE=::2100:3300	19 41
FW_UNI_LREQ	DELAY_RULE=::2100:3300	19 41
FW_UNI_SCLK	DELAY_RULE=U28.N25:RP116.2:2300:2500	19 41

FW_LINK_D<0>	STUB_LENGTH=1500	DELAY_RULE=::5600:6000	21 41
FW_LINK_D<1>	STUB_LENGTH=1500	DELAY_RULE=::5600:6000	21 41
FW_LINK_D<2>	STUB_LENGTH=1500	DELAY_RULE=::5600:6000	21 41
FW_LINK_D<3>	STUB_LENGTH=1500	DELAY_RULE=::5600:6000	21 41
FW_LINK_D<4>	STUB_LENGTH=1500	DELAY_RULE=::5700:6100	21 41
FW_LINK_D<5>	STUB_LENGTH=1500	DELAY_RULE=::5700:6100	21 41
FW_LINK_D<6>	STUB_LENGTH=1500	DELAY_RULE=::5700:6100	21 41
FW_LINK_D<7>	STUB_LENGTH=1500	DELAY_RULE=::5700:6100	21 41
FW_LINK_CNTL0	STUB_LENGTH=1500	DELAY_RULE=::5650:6150	21 41
FW_LINK_CNTL1	STUB_LENGTH=1500	DELAY_RULE=::5700:6200	21 41
FW_LINK_LREQ	STUB_LENGTH=1500	DELAY_RULE=::5650:6150	21 41
FW_LINK_SCLK	STUB_LENGTH=1500	DELAY_RULE=::5200:5500	21 41

RESTRICT MAJORITY OF TRACE TO INNER LAYERS

FW_PHY_D<0>	DELAY_RULE=::200:400	21 22
FW_PHY_D<1>	DELAY_RULE=::200:400	21 22
FW_PHY_D<2>	DELAY_RULE=::200:400	21 22
FW_PHY_D<3>	DELAY_RULE=::200:400	21 22
FW_PHY_D<4>	DELAY_RULE=::100:300	21 22
FW_PHY_D<5>	DELAY_RULE=::100:300	21 22
FW_PHY_D<6>	DELAY_RULE=::100:300	21 22
FW_PHY_D<7>	DELAY_RULE=::100:300	21 22
FW_PHY_CNTL0	DELAY_RULE=::150:250	21 22
FW_PHY_CNTL1	DELAY_RULE=::100:200	21 22
FW_PHY_LREQ	DELAY_RULE=::150:250	21 22
FW_PHY_SCLK	DELAY_RULE=::100:200	21 22

WHEN UNI-N USED:
DATA LINES: 8.2 TO 10.1 INCHES
SCLK: 7.7 - 8.2 INCHES

WHEN LYNX USED:
DATA LINES: 5.8 TO 6.65 INCHES
SCLK: 5.3 - 5.8 INCHES

FIREWIRE LINK TO PHY CONNECTION

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-0997 | REV. 01

SCALE NONE | SHT 21 OF 47

FIREWIRE PHY

F2 0.9AMP-33V
F1 0.9AMP-33V
L30 FERR-250-OHM
L31 FERR-250-OHM
R372 330K 5% 1/16W MF 603
R289 0 5% 1/16W MF 402
C226 0.1UF N20P80% 16V CERM 603
C227 0.001UF 20% 50V CERM 603
C232 0.1UF N20P80% 16V CERM 603
C233 0.001UF 20% 50V CERM 603
C234 0.1UF N20P80% 16V CERM 603
C235 0.001UF 20% 50V CERM 603
C230 2.2UF N20P80% 16V CERM 805
C299 2.2UF N20P80% 16V CERM 805
C301 0.1UF N20P80% 16V CERM 603
C300 0.001UF 20% 50V CERM 603
C229 0.1UF N20P80% 16V CERM 603
C228 0.001UF 20% 50V CERM 603
C298 0.01UF 20% 50V CERM 402
C296 0.01UF 20% 50V CERM 402
C231 2.2UF N20P80% 16V CERM 805
R39 10K 5% 1/16W MF 402 (NOSTUFF)
R306 499K 1% 1/16W MF 603
C236 27PF 5% 50V CERM 805
C237 27PF 5% 50V CERM 805
Y4 24.576M SM
U3 FW802 FLAS-1
R40 10K 5% 1/16W MF 402
R298 56.2 1% 1/16W MF 603
R300 56.2 1% 1/16W MF 603
R294 56.2 1% 1/16W MF 603
R296 56.2 1% 1/16W MF 603
R297 56.2 1% 1/16W MF 603
R299 56.2 1% 1/16W MF 603
R291 56.2 1% 1/16W MF 603
R293 56.2 1% 1/16W MF 603
R305 2.49K 1% 1/16W MF 603
R78 10K 5% 1/16W MF 402 (NO STUFF)
C30 220PF 5% 50V CERM 805
R301 4.99K 1% 1/16W MF 603
C29 0.33UF 20% 16V CERM 805
C224 220PF 5% 50V CERM 805
R295 4.99K 1% 1/16W MF 603
C225 0.33UF 20% 16V CERM 805
R369 1K 5% 1/16W MF 603
C302 0.1UF N20P80% 16V CERM 603
R292 10K 5% 1/16W MF 402
R290 1K 5% 1/16W MF 603
R79 10K 5% 1/16W MF 402
L29 FERR-250-OHM
L28 FERR-250-OHM
T3 (J6: TPO, TPO#, TPI, TPI#, VP, VGND) — PORT 1
T2 (J5: TPO, TPO#, TPI, TPI#, VP, VGND) — PORT 2
C212 0.01UF 20% 50V CERM 402
C213 0.01UF 20% 50V CERM 402
C214 0.01UF 20% 50V CERM 402
C31 0.01UF 20% 50V CERM 402
C223 0.01UF 20% 50V CERM 402
ZH5 MLB MOUNTING SCREW 235R156
ZH1 235R156

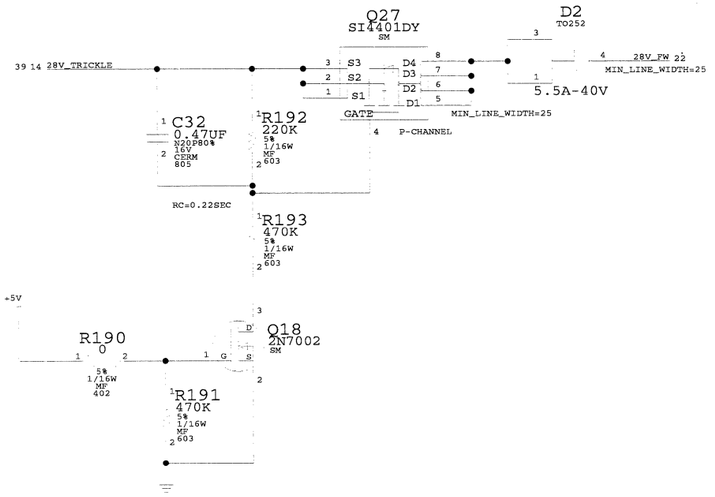
CAPACITOR IN CONJUCTION WITH INTERNAL PULLUP PROVIDES RESET PULSE WHEN PHY FIRST RECEIVES POWER

CLEAR OUT ALL PLANES UNDER TRANSFORMERS

IO FENCE MOUNTING SCREWS

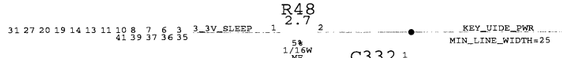
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-0997	01
SCALE: NONE	SHT 22 OF 47	



SOFT START FOR FIREWIRE BUS POWER

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-0997	01
	SCALE	SHT	OF
	NONE	23	47



STAR3

C4

UIDE_PLL_AVDD

U25

KEYLARGO
(1 OF 2)

BGA-1

41 15 13 12 9	33PCI_AD<0>	W18	PCIAD0	EIDE_DD0	L19	31 25 24 IOBUSDT<0>	DELAY_RULE=:::130% 0
41 15 13 12 9	33PCI_AD<1>	V17	PCIAD1	EIDE_DD1	M20	31 25 24 IOBUSDT<1>	DELAY_RULE=:::130% 1
41 15 13 12 9	33PCI_AD<2>	U16	PCIAD2	EIDE_DD2	M19	31 25 24 IOBUSDT<2>	DELAY_RULE=:::130% 2
41 15 13 12 9	33PCI_AD<3>	V18	PCIAD3	EIDE_DD3	M18	31 25 24 IOBUSDT<3>	DELAY_RULE=:::130% 3
41 15 13 12 9	33PCI_AD<4>	W17	PCIAD4	EIDE_DD4	M17	31 25 24 IOBUSDT<4>	DELAY_RULE=:::130% 4
41 15 13 12 9	33PCI_AD<5>	V16	PCIAD5	EIDE_DD5	N20	31 25 24 IOBUSDT<5>	DELAY_RULE=:::130% 5
41 15 13 12 9	33PCI_AD<6>	Y17	PCIAD6	EIDE_DD6	N19	31 25 24 IOBUSDT<6>	DELAY_RULE=:::130% 6
41 15 13 12 9	33PCI_AD<7>	W16	PCIAD7	EIDE_DD7	N18	31 25 24 IOBUSDT<7>	DELAY_RULE=:::130% 7
41 15 13 12 9	33PCI_AD<8>	U14	PCIAD8	EIDE_DD8	P20	31 25 24 IOBUSDT<8>	DELAY_RULE=:::130% 8
41 15 13 12 9	33PCI_AD<9>	Y16	PCIAD9	EIDE_DD9	P19	31 25 24 IOBUSDT<9>	DELAY_RULE=:::130% 9
41 15 13 12 9	33PCI_AD<10>	W15	PCIAD10	EIDE_DD10	P18	31 25 24 IOBUSDT<10>	DELAY_RULE=:::130% 10
41 15 13 12 9	33PCI_AD<11>	V14	PCIAD11	EIDE_DD11	R20	31 25 24 IOBUSDT<11>	DELAY_RULE=:::130% 11
41 15 13 12 9	33PCI_AD<12>	W14	PCIAD12	EIDE_DD12	R19	31 25 24 IOBUSDT<12>	DELAY_RULE=:::130% 12
41 15 13 12 9	33PCI_AD<13>	Y14	PCIAD13	EIDE_DD13	P17	31 25 24 IOBUSDT<13>	DELAY_RULE=:::130% 13
41 15 13 12 9	33PCI_AD<14>	V13	PCIAD14	EIDE_DD14	R18	31 25 24 IOBUSDT<14>	DELAY_RULE=:::130% 14
41 15 13 12 9	33PCI_AD<15>	W13	PCIAD15	EIDE_DD15	T20	31 25 24 IOBUSDT<15>	DELAY_RULE=:::130% 15
41 15 13 12 9	33PCI_AD<16>	Y11	PCIAD16	EIDE_DA0	H20	31 25 24 ATADA<0>	DELAY_RULE=:::130% 0
41 15 13 12 9	33PCI_AD<17>	Y10	PCIAD17	EIDE_DA1	J17	31 25 24 ATADA<1>	DELAY_RULE=:::130% 1
41 15 13 12 9	33PCI_AD<18>	V10	PCIAD18	EIDE_DA2	J18	31 25 24 ATADA<2>	DELAY_RULE=:::130% 2
41 15 13 12 9	33PCI_AD<19>	W10	PCIAD19	IOA3	J19	31 24 ATADA<3>	3
41 15 13 12 9	33PCI_AD<20>	Y9	PCIAD20	IOA4	J20	31 24 ATADA<4>	4
41 15 13 12 9	33PCI_AD<21>	W9	PCIAD21	EIDE_IOCHRDY	H19	ATAIOCHRDY	DELAY_RULE=:::130% 25
41 15 13 12 9	33PCI_AD<22>	V9	PCIAD22	EIDE_CS1FX	H18	ATA0CS1*	DELAY_RULE=:::130% 25 31
41 24 15 13 12 9	33PCI_AD<23>	U9	PCIAD23	EIDE_CS3FX	G20	ATA0CS3*	DELAY_RULE=:::130% 25 31
41 24 15 13 12 9	33PCI_AD<24>	W7	PCIAD24	EIDE0_RST	L18	ATA0RESET*	DELAY_RULE=:::130% 25
41 24 15 13 12 9	33PCI_AD<25>	V7	PCIAD25	EIDE0_WR	K20	ATAWR*	DELAY_RULE=:::130% 25
41 15 13 12 9	33PCI_AD<26>	Y6	PCIAD26	EIDE0_RD	K19	ATARD*	DELAY_RULE=:::130% 25
41 15 13 12 9	33PCI_AD<27>	W6	PCIAD27	EIDE0_DMAACK	G19	ATA0DMAACK*	DELAY_RULE=:::130% 25
41 15 13 12 9	33PCI_AD<28>	U7	PCIAD28	EIDE0_DMAREQ	F19	ATA0DMAREQ	DELAY_RULE=:::130% 25
41 15 13 12 9	33PCI_AD<29>	V6	PCIAD29	EIDE0_INT	G17	ATA0IRQ	DELAY_RULE=:::130% 25
41 15 13 12 9	33PCI_AD<30>	W5	PCIAD30	EIDE1_RST	L20	NC_ATA1RST*	
41 15 13 12 9	33PCI_AD<31>	V5	PCIAD31	EIDE1_WR	K18	NC_ATA1WR*	
41 15 13 12 9	33PCI_CBE<0>*	V15	PCIC_BE0	EIDE1_RD	K17	NC_ATA1RD*	
41 15 13 12 9	33PCI_CBE<1>*	Y13	PCIC_BE1	EIDE1_DMAACK	F20	NC_ATA1ACK*	
41 15 13 12 9	33PCI_CBE<2>*	W11	PCIC_BE2	EIDE1_DMAREQ	G18	PD_ATA1REQ	
41 15 13 12 9	33PCI_CBE<3>*	Y7	PCIC_BE3	EIDE1_INT	E20	PD_ATA1INT	
41 15 13 12 9	33PCI_PAR	U12	PCIPAR	DEVCS2	E19	CRDSLT_CE2*	31
41 35 15 13 12 9	33PCI_FRAME*	V11	PCIFRAME	DEVCS3	D20	NC_DEVCS3*	
41 35 15 13 12 9	33PCI_TRDY*	Y12	PCITRDY	DEVCS4	E18	NC_DEVCS4*	
41 35 15 13 12 9	33PCI_IRDY*	U11	PCIIRDY	PRAMCS	D19	CRDSLT_CE1*	31
41 35 15 13 12 9	33PCI_STOP*	V12	PCISTOP	DIR_245	C20	NC_DIR245	
41 35 15 13 12 9	33PCI_DEVSEL*	W12	PCIDEVSEL	UIDE_DD0	A13	26 24 UDSD<0>	DELAY_RULE=::4700:5200 0
KW_IDSEL		V8	PCIIDSEL	UIDE_DD1	C12	26 24 UDSD<1>	DELAY_RULE=::4700:5200 1
KW_IDSEL_USB0		W8	PCIIDESEL_USB0	UIDE_DD2	D12	26 24 UDSD<2>	DELAY_RULE=::4700:5200 2
KW_IDSEL_USB1		Y8	PCIIDESEL_USB1	UIDE_DD3	A12	26 24 UDSD<3>	DELAY_RULE=::4700:5200 3
35 12 9	KWEST_PCI_REQ*	Y4	PCIREQ	UIDE_DD4	B12	26 24 UDSD<4>	DELAY_RULE=::4700:5200 4
12 9	KWEST_PCI_GNT*	Y3	PCIGNT	UIDE_DD5	A10	26 24 UDSD<5>	DELAY_RULE=::4700:5200 5
31	MODEM_SDOWN	U3	ARBCRITICAL	UIDE_DD6	A11	26 24 UDSD<6>	DELAY_RULE=::4700:5200 6
36	IO_RESET*	V4	PCIRST	UIDE_DD7	C10	26 24 UDSD<7>	DELAY_RULE=U25.C10:RP13.3:4700:5200 7
18	KWEST_PCI_CLK	U5	PCICLK	UIDE_DD8	B10	26 24 UDSD<8>	DELAY_RULE=::4700:5200 8
37 31 30 29 27 20	5V_SLEEP	W4	PCI_IO_RAIL	UIDE_DD9	B9	26 24 UDSD<9>	DELAY_RULE=::4700:5200 9
				UIDE_DD10	C9	26 24 UDSD<10>	DELAY_RULE=::4700:5200 10
				UIDE_DD11	A8	26 24 UDSD<11>	DELAY_RULE=::4700:5200 11
				UIDE_DD12	D9	26 24 UDSD<12>	DELAY_RULE=::4700:5200 12
				UIDE_DD13	B8	26 24 UDSD<13>	DELAY_RULE=::4700:5200 13
				UIDE_DD14	A7	26 24 UDSD<14>	DELAY_RULE=::4700:5200 14
				UIDE_DD15	C8	26 24 UDSD<15>	DELAY_RULE=::4700:5200 15
				UIDE_DA0	D14	26 24 UDSA<0>	DELAY_RULE=::4700:5200 0
				UIDE_DA1	B15	26 24 UDSA<1>	DELAY_RULE=::4700:5200 1
				UIDE_DA2	A15	26 24 UDSA<2>	DELAY_RULE=::4700:5200 2
				UIDE_IOCHRDY	D10	UDSTB0/DRDY0*	DELAY_RULE=::4700:5200 26
				UIDE_CS1FX	B14	UATA_CS1*	DELAY_RULE=::4700:5200 26
				UIDE_CS3FX	C14	UATA_CS3*	DELAY_RULE=::4700:5200 26
				UIDE_RST	B7	UATARESET*	
				UIDE_WR	A16	USTOP0	DELAY_RULE=::125:325
				UIDE_RD	C15	UHSTB0/RDY0*	DELAY_RULE=::125:325
				UIDE_DMAACK	B13	UDMACK0*	DELAY_RULE=::125:325
				UIDE_DMAREQ	C11	UDMARQ0	DELAY_RULE=::4700:5200 26
				UIDE_INT	C13	UINTA0*	DELAY_RULE=::4700:5200 26

IOBUSDT<15..0> 24 25 31

ATADA<4..0> 24 25 31

UDSD<15..0> 24 26

UDSA<2..0> 24 26

41 24 15 13 12 9 33PCI_AD<23>
41 24 15 13 12 9 33PCI_AD<24>
41 24 15 13 12 9 33PCI_AD<25>

R87 22 5% 1/16W MF 402
R89 22 5% 1/16W MF 402
R88 22 5% 1/16W MF 402

R112 4.99K 1% 1/16W MF 603
R110 4.99K 1% 1/16W MF 603

RP18 22 5% 1/16W SM

4	5	RUATARESET*	DELAY_RULE=RP18.5:J15.1:4700:5200 26
1	8	RU0STOP	DELAY_RULE=::4700:5200 26
2	7	UHSTB/RDY*	DELAY_RULE=::4700:5200 26
3	6	UATA0DMACK*	DELAY_RULE=RP18.6:J15.29:4700:5200 26

KEYWEST/1

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-0997	01
SCALE: NONE	SHT 24 OF 47	

31 25 24 IOBUSDT<15..0>

RP101 33 5% 1/16W SM
RP102 33 5% 1/16W SM
RP103 33 5% 1/16W SM
RP100 33 5% 1/16W SM

31 25 24	0 IOBUSDT<0>	4	5	25 IDE0D<0> DELAY_RULE=:::500 0
31 25 24	1 IOBUSDT<1>	3	6	25 IDE0D<1> DELAY_RULE=:::500 1
31 25 24	2 IOBUSDT<2>	2	7	25 IDE0D<2> DELAY_RULE=:::500 2
31 25 24	3 IOBUSDT<3>	1	8	25 IDE0D<3> DELAY_RULE=:::500 3
31 25 24 IOBUSDT<7> 7	4 IOBUSDT<4>	4	5	25 IDE0D<4> DELAY_RULE=:::500 4
31 25 24	5 IOBUSDT<5>	3	6	25 IDE0D<5> DELAY_RULE=:::500 5
31 25 24	6 IOBUSDT<6>	2	7	25 IDE0D<6> DELAY_RULE=:::500 6
31 25 24	7 IOBUSDT<7>	1	8	25 IDE0D<7> DELAY_RULE=:::500 7
31 25 24	8 IOBUSDT<8>	1	8	25 IDE0D<8> DELAY_RULE=:::500 8
31 25 24	9 IOBUSDT<9>	2	7	25 IDE0D<9> DELAY_RULE=:::500 9
31 25 24	10 IOBUSDT<10>	3	6	25 IDE0D<10> DELAY_RULE=:::500 10
31 25 24	11 IOBUSDT<11>	4	5	25 IDE0D<11> DELAY_RULE=:::500 11
31 25 24	12 IOBUSDT<12>	1	8	25 IDE0D<12> DELAY_RULE=:::500 12
31 25 24	13 IOBUSDT<13>	2	7	25 IDE0D<13> DELAY_RULE=:::500 13
31 25 24	14 IOBUSDT<14>	3	6	25 IDE0D<14> DELAY_RULE=:::500 14
31 25 24	15 IOBUSDT<15>	4	5	25 IDE0D<15> DELAY_RULE=:::500 15

[1]R263 10K 5% 1/16W MF 402 — PULLDOWN RESISTOR ALLOWS HOST TO DETECT THE ABSENSE OF AN IDE DEVICE

+5V

R265 10K 5% 1/16W MF 402

24 ATA0RESET* — R264 33 5% 1/16W MF 603 — DELAY_RULE=:::500 — IDERST0*

+5V +5V

[1]R258 1K 5% 1/16W MF 603

[1]R520 10K 5% 1/16W MF 402

24 ATA0DMAREQ	R262 82 5% 1/16W MF 603	DELAY_RULE=:::500	IDE0DMAREQ
24 ATA0DMAACK*	R256 22 5% 1/16W MF 603	DELAY_RULE=:::500	IDEWR*
		DELAY_RULE=:::500	IDERD*
		DELAY_RULE=:::500	IORDY
		DELAY_RULE=:::500	IDEDMAACK*
		DELAY_RULE=:::500	IDE0IRQ
24 ATA0IRQ	R255 82 5% 1/16W MF 603	DELAY_RULE=:::500	IDEA<1>
		DELAY_RULE=:::500	IDEA<0>
		DELAY_RULE=:::500	IDE0CS1*
24 ATAWR*	R260 22 5% 1/16W MF 402		
24 ATARD*	R259 22 5% 1/16W MF 402		
31 24 ATADA<1>	R253 33 5% 1/16W MF 402		
31 24 ATADA<0>	R252 33 5% 1/16W MF 603		
31 24 ATA0CS1*	R251 22 5% 1/16W MF 603		
31 24 ATA0CS3*	R523 22 5% 1/16W MF 402	DELAY_RULE=:::500	
31 24 ATADA<2>	R522 33 5% 1/16W MF 603	DELAY_RULE=:::500	
24 ATA0IOCHRDY	R257 82 5% 1/16W MF 603		

C204 47PF 5% 50V CERM 805 — 33 PF OK?

[1]R261 4.99K 1% 1/16W MF 603

[1]R254 4.99K 1% 1/16W MF 603

ATA(3) CONNECTOR

DEVELOPMENT
DS7
IDE0_INUSE* 2 — 1 IDE0_INUSE1*
GREEN SM
ATA(3) ACTIVE

DEVELOPMENT
[1]R250 330 5% 1/16W MF 603

NO STUFF
1 C418 0.01UF 20% 50V CERM 402

NO STUFF
1 C419 0.01UF 20% 50V CERM 402

LOWER_CHASSIS 39

IDE0D<15..0>

J33 TH

7	25 IDE0D<7>	3	4	25 IDE0D<8> 8
6	25 IDE0D<6>	5	6	25 IDE0D<9> 9
5	25 IDE0D<5>	7	8	25 IDE0D<10> 10
4	25 IDE0D<4>	9	10	25 IDE0D<11> 11
3	25 IDE0D<3>	11	12	25 IDE0D<12> 12
2	25 IDE0D<2>	13	14	25 IDE0D<13> 13
1	25 IDE0D<1>	15	16	25 IDE0D<14> 14
0	25 IDE0D<0>	17	18	25 IDE0D<15> 15
		19		
		21	22	
		23	24	IDEDETECT* 27
		25	26	
		27	28	IDE0DCSELP*
		29	30	
		31	32	IDE0IOCS16
		33	34	N.C. (PDIAG)
		35	36	IDEA<2>
		37	38	IDE0CS3*
		39	40	+5V

+3.3V

[1]R518 10K 5% 1/16W MF 402

[1]R521 1K 5% 1/16W MF 603

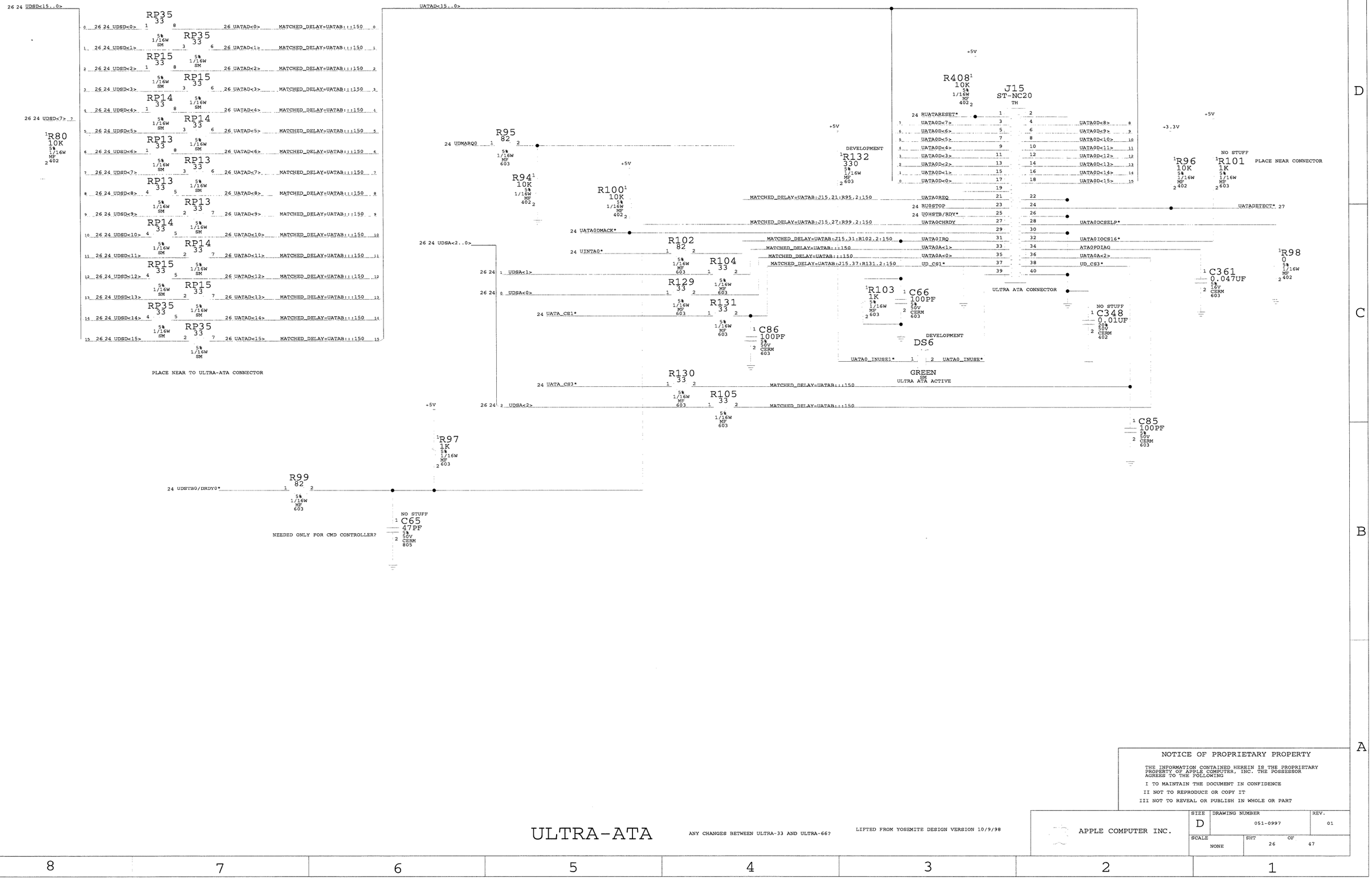
[1]R519 0 5% 1/16W MF 402 — CABLE SELECT = 0 (CABLE HARNESS MUST ISOLATE THIS LINE FROM SECOND DRIVE)

LIFTED FROM YOSEMITE DESIGN VERSION 6/2/98

IDE TERMINATION/CONNECTORS, NVRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-0997	01
SCALE: NONE	SHT 25 OF 47	



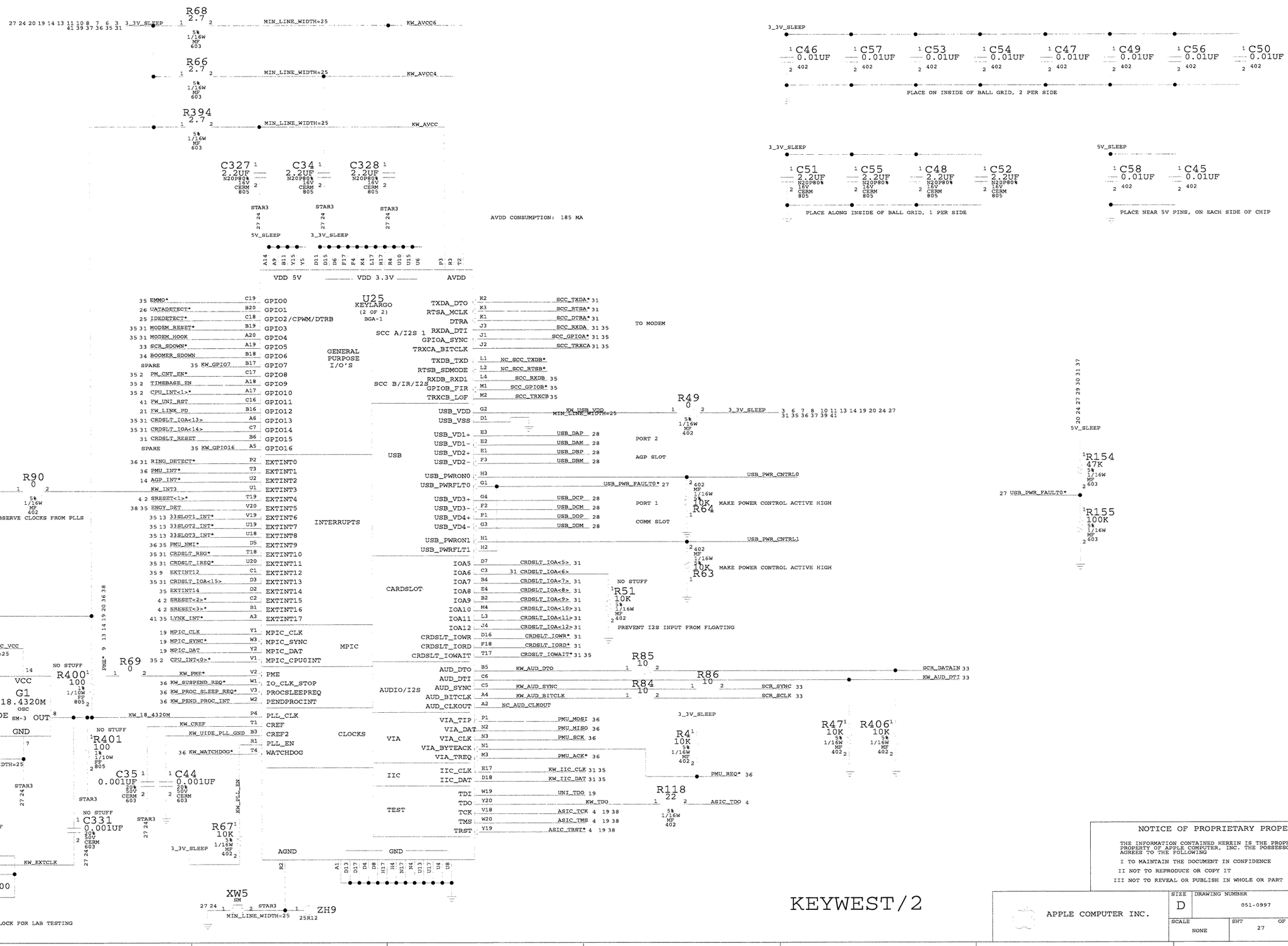
ULTRA-ATA

ANY CHANGES BETWEEN ULTRA-33 AND ULTRA-66?

LIFTED FROM YOSEMITE DESIGN VERSION 10/9/98

APPLE COMPUTER INC.

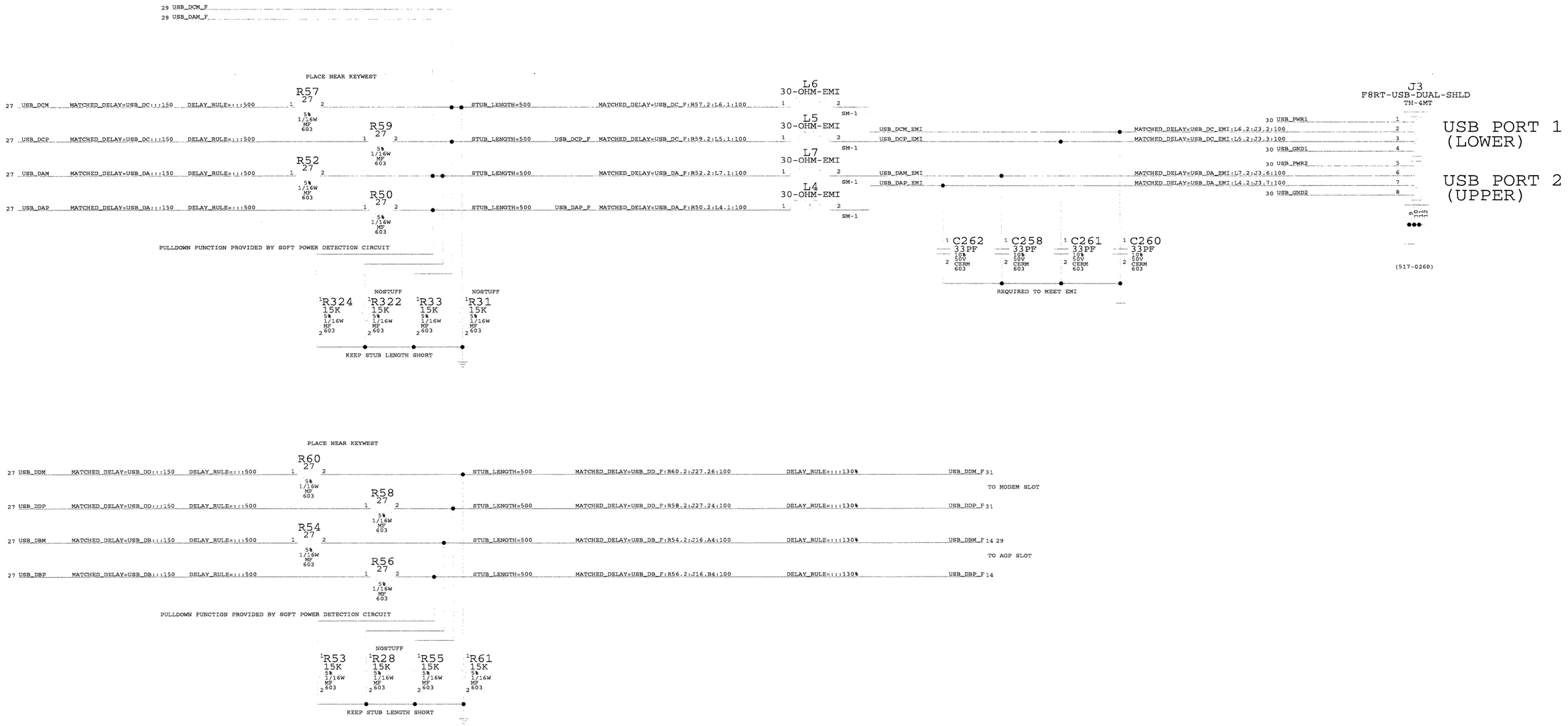
SIZE	DRAWING NUMBER	REV.
D	051-0997	01
SCALE: NONE	SHT 26 OF 47	



KEYWEST/2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-0997	01
SCALE: NONE	SHT 27 OF 47	



USB PORTS

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-0997	01
	SCALE	SHT	OF
	NONE	28	47

39 37 36 33 5V_TRICKLE

R385 1K 5% 1/16W MF 603

TURN OFF CURRENT SOURCE WHEN POWER ON

SFT_PWR1

5V_SLEEP

Q2 2N7002 SM

R386 15K 5% 1/16W MF 603

R29 15K 5% 1/16W MF 603

R27 15K 5% 1/16W MF 603

RP10 100K 5% 1/16W SM

RP10 100K 5% 1/16W SM

2.67V SFT_PWR4

RP10 100K 5% 1/16W SM

RP10 100K 5% 1/16W SM

C321 0.1UF N20P80% 16V CERM 603

100K GIVES LONGER POWER ON KEY TIME CONSTANT

SFT_PWR5

LM339A SOI

U16

28 USB_DAM_F

R387 47.0K 1% 1/16W MF 603

SFT_PWR2

C322 0.047UF 5% 16V CERM 603

THRESHOLD = .24V

AGP_SFT_PWR_NOT

R170 10K 5% 1/16W MF 402

28 14 USB_DBM_F

AGP_SFT_PWR

R71 47.0K 1% 1/16W MF 603

SFT_PWR3

AGP_SFT_PWR

C37 0.047UF 5% 16V CERM 603

LM339A SOI

U16

R72 47.0K 1% 1/16W MF 603

SFT_PWR6

SFT_PWR7

1.6 VOLTS WHEN LOW

SFT_PWR8

LM339A SOI

U16

PWR_SWITCH* 14 36 39

5V_SLEEP

Q1 2N7002 SM

IGNORE COMPARATOR OUTPUT WHEN POWER ON

28 USB_DCM_F

R26 47.0K 1% 1/16W MF 603

SFT_PWR9

C23 0.047UF 5% 16V CERM 603

R25 10K 5% 1/16W MF 402

LM339A SOI

U16

LOW SPEED USB PULLS-UP D- WITH 1.5K OHM RESISTOR, V = 430 MV

HIGH SPEED USB VOLTAGE GENERALLY LIMITED BY FORWARD BIASED PROTECTION DIODE (~700 MV)

USB SOFT POWER DETECT

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-0997 | REV. 01

SCALE NONE | SHT 29 OF 47

DCR = 0.008 OHMS MAX

MIN_LINE_WIDTH=25

C977
0.1UF
N20P80%
16V
CERM
603

L2
63-OHM
SM
155S0045

MIN_LINE_WIDTH=50

28 USB_PWR2

C978
150UF
20%
6.3V
TANT
SMD
POSCAP

NO STUFF
C24
10UF
N20P80%
16V
CERM
1210

USB SPEC = 4.75 V MIN

MIN_LINE_WIDTH=50 USB_GND2 28

LOW ESR REQUIRED TO MEET HOTPLUG DROOP SPEC

C264
0.01UF
20%
50V
CERM
402

C256
0.01UF
20%
50V
CERM
402

37 31 29 27 24 20 5V_SLEEP

DCR = 0.008 OHMS MAX

MIN_LINE_WIDTH=25

C981
0.1UF
N20P80%
16V
CERM
603

L3
63-OHM
SM
155S0045

MIN_LINE_WIDTH=50 USB_PWR1 28

C982
150UF
20%
6.3V
TANT
SMD
POSCAP

NO STUFF
C255
10UF
N20P80%
16V
CERM
1210

USB SPEC = 4.75 V MIN

MIN_LINE_WIDTH=50 USB_GND1 28

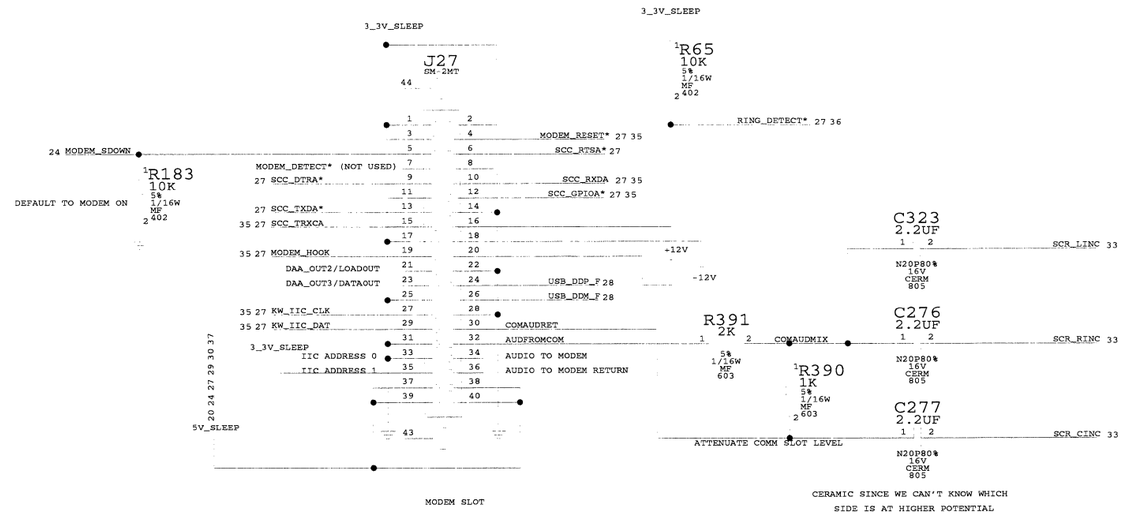
LOW ESR REQUIRED TO MEET HOTPLUG DROOP SPEC

C263
0.01UF
20%
50V
CERM
402

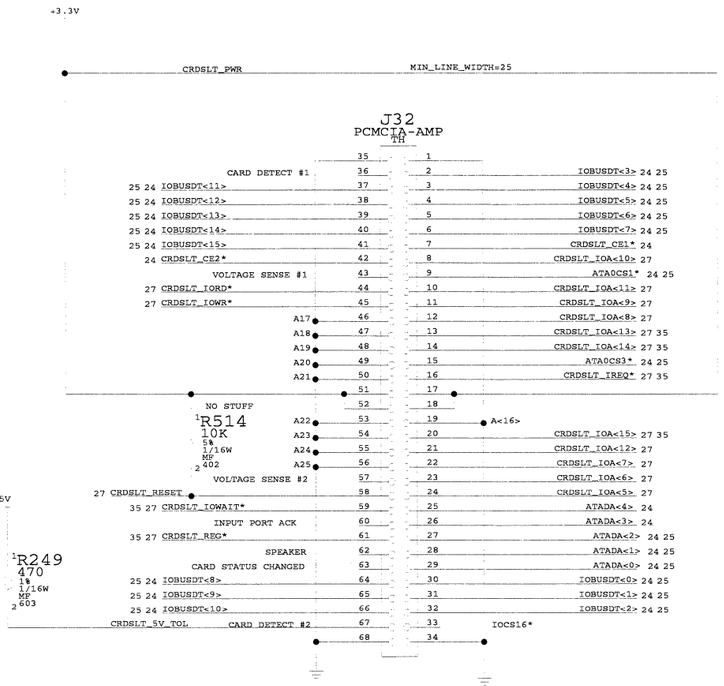
C257
0.01UF
20%
50V
CERM
402

USB PORT POWER

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-0997	01
	SCALE	SHT OF	
	NONE	30 47	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
460-3108	2	SCREW, M3.0X0.5X4.0MM	X7,X8	
805-2264	2	8MM,2X SCREW STANDOFF	X10,X11	
815-3221	1	STANDOFF	X13	

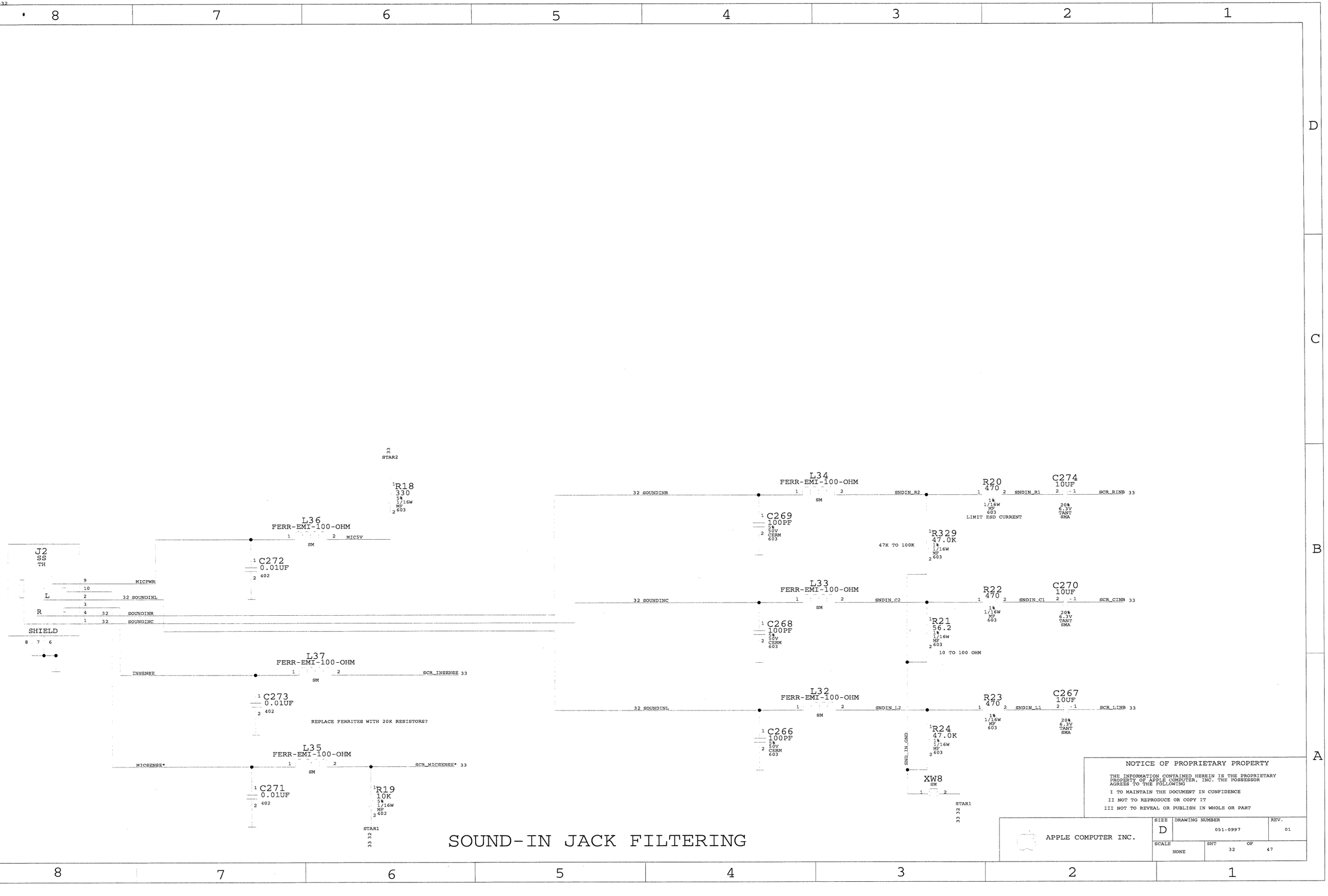


MODEM SLOT, CARDBUS CONNECTOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-0997	01
SCALE: NONE	SHT 31 OF 47	

CR-32



SOUND-IN JACK FILTERING

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-0997	01

SCALE	SHT	OF
NONE	32	47

ANALOG STAR POWER

ZH6 1 32 STAR2
25R12

+12V

L1
FERR-250-OHM
SM
WAS 1550070

MAX CURRENT = 200 MA BEFORE VOLTAGE SAGS TO 8.5V
WOULD ONE RESISTOR BE CHEAPER?

MIN_LINE_WIDTH=25
AUD12V

R330 33 5% 1/2W FF 2010
R389 33 5% 1/2W FF 2010

VR1 78M05 SM $0.24
IN OUT GND

MIN_LINE_WIDTH=25 AUDREGIN
MIN_LINE_WIDTH=25 AUDIO5V
MIN_LINE_WIDTH=25 AUD_REG_GND
CHANGE TO 7805 FOR HIGHER CURRENT?
CURRENT ~95 MA. POWER DISSIPATION ~.67W (.5W WITH RESISTOR)

C22 3.3UF 10% 16V TANT SMA
C275 0.01UF 402
C324 0.01UF 402
C36 3.3UF 10% 16V TANT SMA

XW12 SM
XW13 SM
XW2 SM
XW3 SM

SCR_AVDD2 DELAY_RULE=:::300
SCR_AVDD1 DELAY_RULE=:::300

XW9 SM
MIN_LINE_WIDTH=25

STAR1
33 32

RP3 100K 5% 1/16W SM
8 7 6 5
1 2 3 4

SOUND-IN JACK
COMM SLOT

KEEP CAP CLOSE TO SCREAMER PINS 2 AND 3
SCR_DVDD
MIN_LINE_WIDTH=25
C325 3.3UF 10% 16V TANT SMA
C329 0.01UF 402
SCR_DGND

NATIONAL: 60 MA
CRYSTAL: 15 MA

C283 0.01UF 402
C284 0.01UF 402
AVDD1 AVDD2 DVDD

U1
SCREAMER
PLC

NC_SCR_9	9	L_IN_A	L_OUT_A	27	HPL
NC_SCR_7	7	R_IN_A	R_OUT_A	25	HPR
NC_SCR_8	8	COM_IN_A	COM_OUT_A	28	HPCOM
32 SCR_LINB	15	L_IN_B	L_OUT_B	34	N.C.
32 SCR_RINB	13	R_IN_B	R_OUT_B	32	N.C.
32 SCR_CINB	14	COM_IN_B	COM_OUT_B	33	N.C.
31 SCR_LINC	10	L_IN_C	L_OUT_C	29	SCR_LOUTC 34
31 SCR_RINC	12	R_IN_C	R_OUT_C	31	SCR_ROUTC 34
31 SCR_CINC	11	COM_IN_C	COM_OUT_C	30	SCR_REF 34
		P_IN_0	P_OUT_0	41	SOUND_OUT_EN
		P_IN_1	P_OUT_1	40	N.C.
		P_IN_2			
		P_IN_3			
	42	SCLK			
	43	SYNC			
	44	SD_IN	SD_OUT	1	SCR_DATAOUT
	5	SEL_0	L_IN_AA	16	SCR_ALIASL
	4	SEL_1	R_IN_AA	17	SCR_ALIASR
	35	RESET	VREF_BYP	19	SCR_VREF
	6	TEST	REF_BUF	18	
	24	PWD			
	26	PCMCIA_SPKRO			
		AGND1 AGND2 DGND			
		20 23 2			

1 = SOUND OUT PORT ENABLED

CONNECT THIS TO COMM SLOT?
TO SPEAKER AMP

32 SCR_MICSENSE* 4
33 REARHPDET 3
32 SCR_INSENSE 2
NC_PIN3 1
RP4 100K 5% 1/16W SM
5 6 7 8
P_IN<0> P_IN<1> P_IN<2> P_IN<3>

27 SCR_SCLK
27 SCR_SYNC
27 SCR_DATAIN
SCR_SEL0
SCR_SEL1
41 36 14 13 12 9 MAIN_RESET*
SCR_TEST
27 SCR_SDOWN*
SCR_PCM_AUD

R396 10 SCR_DATAOUT KW_AUD_DTI 27

C278 3.3UF 10% 16V TANT SMA
C280 3.3UF 10% 16V TANT SMA
C20 0.001UF 10% 50V CERM 603
C21 0.001UF 10% 50V CERM 603

C281 0.1UF N20P80% 16V CERM 603
SCR_AGND2 DELAY_RULE=:::300
SCR_DGND

R340 10K 5% 1/16W MF 402
RP9 470 5% 1/16W SM
7 8 6 5
2 1 3 4
DEFAULT SCREAMER TO POWERED DOWN

R393 4.7 5% 1/16W MF 603
FOR NATIONAL PART
XW14 SM
MIN_LINE_WIDTH=25

33 32 STAR1
MIN_LINE_WIDTH=25
DELAY_RULE=ZH7.1:U1.20::300 VERY, VERY SHORT

R331 1 5% 1/4W PF 1210
L42 1000-OHM-EMI SM
HPRETB
CURRENT RETURN FOR HEADPHONE OUTPUT

XW10 SM
ZH7 1 25R12
LOCATE AS CLOSE AS POSSIBLE TO HEADPHONE JACK
C219 330PF 10% 50V CERM 603

ANALOG STAR GROUND

HOT GROUND COLD GROUND

KEEP SHORT
0 OHM STAR GROUND
2
20
SCREAMER
23

COLD ISOLATED GROUND PLANE UNDER AUDIO CIRCUITRY
ALL OTHER PLANES CLEARED OUT

20-30 MIL ALL-LAYER CUT

CAN BRING IN FINGER OF GROUND PLANE TO CAPTURE DIGITAL INTERFACE SIGNALS ON SCREAMER

R342 0 5% 1/16W MF 402
NO STUFF
BYPASS ANTI-POP CIRCUIT

Q16 TP0610 SM
Q14 TP0610 SM

C15 100UF 20% 6.3V ELEC SM
HPL0 HPL4 HPL1

R343 10K 5% 1/16W MF 402
C286 0.1UF N20P80% 16V CERM 603

LIMIT ESD CURRENT
C13 1UF 10% 16V TANT
HPC1
R345 470 1% 1/16W MF 603
HPC2
SMA

C19 0.01UF CERM
KEEP SCREAMER STABLE IF EXCESSIVE INDUCTANCE

XW4 SM
AUD_OUT_GND
STAR1
33 32

R333 10K 5% 1/16W MF 402
ANTI_POP
Q12 TP0610 SM
Q13 TP0610 SM

C16 100UF 20% 6.3V ELEC SM
HPR0 HPR4 HPR1

R336 0 5% 1/16W MF 402
BYPASS ANTI-POP CIRCUIT NO STUFF

5V_TRICKLE
Q15 TP0610 SM
R346 10K 5% 1/16W MF 402
SCR_SNDOUTEN
R344 100K 5% 1/16W MF 603
-12V

LOCATE EMI FILTERS NEAR AUDIO JACK

R335 100 5% 1/16W MF 603
L39 1000-OHM-EMI SM
L24 1000-OHM-EMI SM
HPL2 HPL3

C17 0.01UF CERM
2 FOR NATIONAL PART
C218 330PF 10% 50V CERM 603

L38 1000-OHM-EMI SM
L23 1000-OHM-EMI SM
HPC3

C217 330PF 10% 50V CERM 603

C18 0.01UF CERM
2 FOR NATIONAL PART

R332 47.0K 1% 1/16W MF 603
DC DRAW FOR HP DETECT DURING ANTI-POP OPERATION
R334 100 5% 1/16W MF 603
L40 1000-OHM-EMI SM
L27 1000-OHM-EMI SM
HPR2 HPR3

ALL EMI INDUCTORS MUST OF SAME VALUE

C221 330PF 10% 50V CERM 603

R341 100K 5% 1/16W MF 603

L41 1000-OHM-EMI SM
L26 1000-OHM-EMI SM
33 REARHPDET HPDET

C220 0.01UF 20% 50V CERM 402

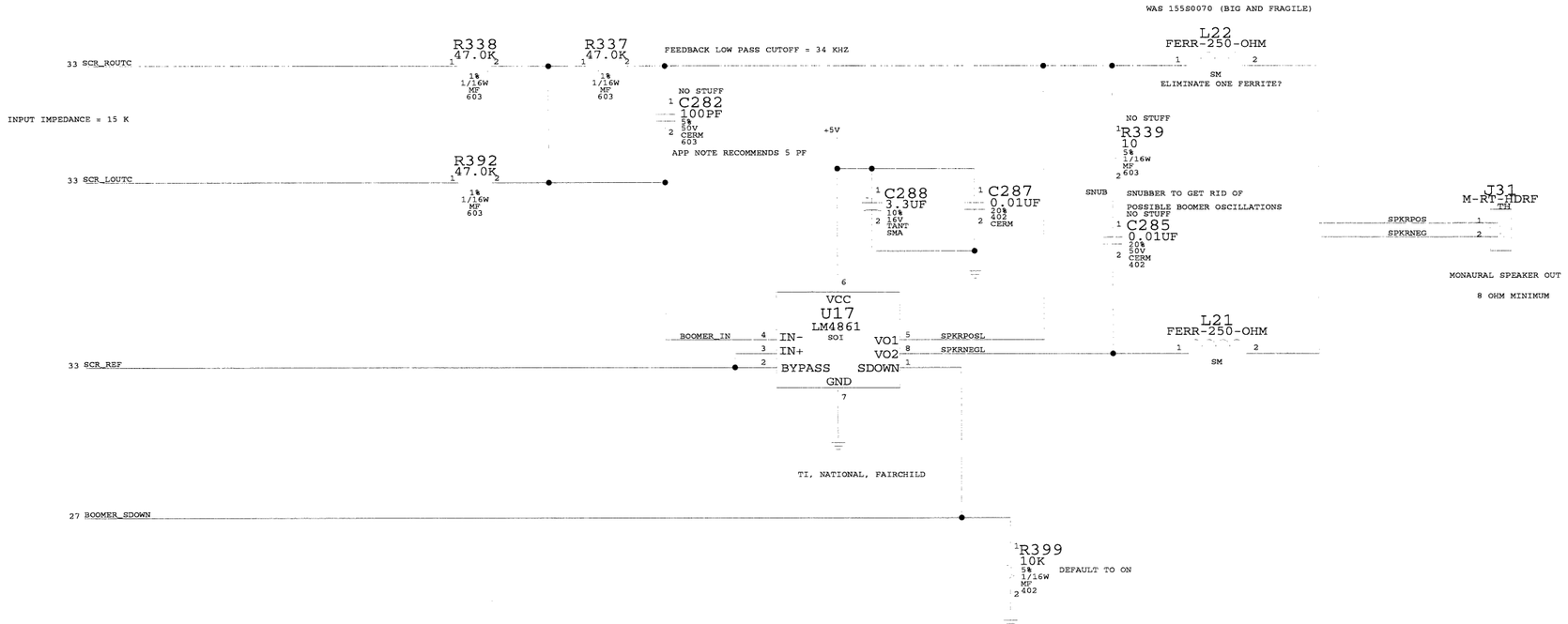
J1 SS TH-1
HEADPHONE_L 5 L
HP_DETECT 3
HEADPHONE_R 4 R
WRHP_RETURN 1
SHIELD 6 7 8

L25 1000-OHM-EMI SM
HPRET

SCREAMER PARALLEL INPUT PORT ASSIGNMENTS:

PORT 0: LOW WHEN PLAINTALK MIC INSERTED
PORT 1: HIGH WHEN PLUG IN SOUND OUT PORT
PORT 2: HIGH WHEN PLUG IN SOUND IN PORT

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-0997	01
	SCALE	SHT	OF
	NONE	33	47



APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-0997	01
	SCALE	SHT OF	
	NONE	34 47	

MAXBUS PULLUPS

PULLUPS NEEDED WITH KEEPERS?

MAXBUS_IO_RAIL

3 2 BR<0>* — RP95 — 5
3 2 HIT<0>* — 2 — 7
3 2 BR<1>* — 1 — 8
3 2 DRDY<0>* — 3 — 6
4
10K 5% 1/16W SM

3 2 DRDY<1>* — RP94 — 5
5 3 2 ARTRY* — 1 — 8
3 2 HIT<1>* — 2 — 7
5 3 2 TS* — 3 — 6
4
10K 5% 1/16W SM

5 3 2 TA* — RP93 — 6
5 3 2 TEA* — 2 — 7
3 2 2.5V_1.8V* — 1 — 8
4 — 5
10K 5% 1/16W SM

27 2 CPU_INT<0>* — R227 2K — 5% 1/16W MF 603
27 2 CPU_INT<1>* — R221 2K — 5% 1/16W MF 603

36 2 SMI<0>* — R485 2K — 5% 1/16W MF 603
36 2 SMI<1>* — R471 2K — 5% 1/16W MF 603 NO STUFF
36 2 SMI<2>* — R490 2K — 5% 1/16W MF 603 NO STUFF
36 2 SMI<3>* — R473 2K — 5% 1/16W MF 603

27 2 TIMEBASE_EN — R482 2K — 5% 1/16W MF 603
27 2 PM_CNT_EN* — R483 2K — 5% 1/16W MF 603

IS THERE A BETTER WAY TO DO LEVEL CONVERSION?

33 MHZ PCI PULLUPS

+3.3V

41 24 15 13 12 9 33PCI_FRAME* — RP20 — 4.7K 5% 1/16W SM
41 24 15 13 12 9 33PCI_TRDY*
41 24 15 13 12 9 33PCI_IRDY*
41 24 15 13 12 9 33PCI_STOP*
15 13 33PCI_LOCK* — RP37 — 4.7K 5% 1/16W SM
41 24 15 13 12 9 33PCI_DEVSEL*
15 13 12 9 33PCI_REQ64*
15 13 12 9 33PCI_ACK64*
41 15 13 33PCI_PERR* — RP36 — 4.7K 5% 1/16W SM
41 15 13 33PCI_SERR*
13 33PCI_SDONE
13 33PCI_SBO*
12 9 NIGEL_PCI_REQ0* — RP32 — 4.7K 5% 1/16W SM
24 12 9 KWEST_PCI_REQ*
41 12 9 FW_PCI_REQ*
13 12 9 33SLOT1_REQ* — RP55 — 4.7K 5% 1/16W SM
13 12 9 33SLOT2_REQ*
13 12 9 33SLOT3_REQ*
15 13 12 9 33PCI_PAR64

PCI PULLUPS 4.7K SO IX MICRO VIDEO CARD WORKS

+3.3V

13 33PCI_TMS — R45 10K — 5% 1/16W MF 402
13 33PCI_TCK — R46 10K — 5% 1/16W MF 402
13 33PCI_TRST* — R44 1K — 5% 1/16W MF 603

+3.3V

15 13 12 9 33PCI_AD<32> — RP85 — 10K 5% 1/16W SM
15 13 12 9 33PCI_AD<33>
15 13 12 9 33PCI_AD<34>
15 13 12 9 33PCI_AD<35>
15 13 12 9 33PCI_AD<36> — RP84 — 10K 5% 1/16W SM
15 13 12 9 33PCI_AD<37>
15 13 12 9 33PCI_AD<38>
15 13 12 9 33PCI_AD<39>
15 13 12 9 33PCI_AD<40> — RP83 — 10K 5% 1/16W SM
15 13 12 9 33PCI_AD<41>
15 13 12 9 33PCI_AD<42>
15 13 12 9 33PCI_AD<43>
15 13 12 9 33PCI_AD<44> — RP42 — 10K 5% 1/16W SM
15 13 12 9 33PCI_AD<45>
15 13 12 9 33PCI_AD<46>
15 13 12 9 33PCI_AD<47>
15 13 12 9 33PCI_AD<48> — RP64 — 10K 5% 1/16W SM
15 13 12 9 33PCI_AD<49>
15 13 12 9 33PCI_AD<50>
15 13 12 9 33PCI_AD<51>
15 13 12 9 33PCI_AD<52> — RP63 — 10K 5% 1/16W SM
15 13 12 9 33PCI_AD<53>
15 13 12 9 33PCI_AD<54>
15 13 12 9 33PCI_AD<55>
15 13 12 9 33PCI_AD<56> — RP62 — 10K 5% 1/16W SM
15 13 12 9 33PCI_AD<57>
15 13 12 9 33PCI_AD<58>
15 13 12 9 33PCI_AD<59>
15 13 12 9 33PCI_AD<60> — RP61 — 10K 5% 1/16W SM
15 13 12 9 33PCI_AD<61>
15 13 12 9 33PCI_AD<62>
15 13 12 9 33PCI_AD<63>

15 13 12 9 33PCI_CBE<4>* — RP60 — 10K 5% 1/16W SM
15 13 12 9 33PCI_CBE<5>*
15 13 12 9 33PCI_CBE<6>*
15 13 12 9 33PCI_CBE<7>*

KEYWEST PULLUPS

+3.3V

27 EMMO* — RP40 — 10K 5% 1/16W SM — 3_3V_SLEEP
31 27 MODEM_RESET*
31 27 MODEM_HOOK
27 KW_GPIO7
31 27 CRDSLT_IOA<13> — RP112 — 10K 5% 1/16W SM
31 27 CRDSLT_IOA<14>
27 KW_GPIO16
31 27 CRDSLT_IOWAIT* — RP43 — 10K 5% 1/16W SM
38 27 ENGY_DET
27 13 33SLOT1_INT*
27 13 33SLOT2_INT*
27 13 33SLOT3_INT* — RP41 — 10K 5% 1/16W SM
36 27 PMU_NMI*
31 27 CRDSLT_REG*
31 27 CRDSLT_IREQ*
27 9 EXTINT12 — RP16 — 10K 5% 1/16W SM
31 27 CRDSLT_IOA<15>
27 EXTINT14
27 SCC_RXDB — RP17 — 10K 5% 1/16W SM
41 27 LYNX_INT*
27 SCC_GPIOB*
27 SCC_TRXCB

31 27 SCC_RXDA — RP19 — 10K 5% 1/16W SM
31 27 SCC_GPIOA*
31 27 SCC_TRXCA

IIC BUS PULLUPS

MAIN RAIL, TO PREVENT LEAKAGE INTO UNPOWERED DEVICES

+3.3V

19 UNI_PU1 — R235 1K — 5% 1/16W MF 603
19 UNI_PU2 — R232 1K — 5% 1/16W MF 603
31 27 KW_IIC_CLK — R181 1K — 5% 1/16W MF 603
31 27 KW_IIC_DAT — R182 1K — 5% 1/16W MF 603
36 18 16 PMU_IIC_CLK — R354 4.99K — 1% 1/16W MF 603
PMU NOT RATED STRONG ENOUGH FOR 1K
36 18 16 PMU_IIC_DAT — R353 4.99K — 1% 1/16W MF 603

19 8 7 2 UNI_IIC_CLK — R236 1K — 5% 1/16W MF 603
19 8 7 2 UNI_IIC_DAT — R234 1K — 5% 1/16W MF 603
NO STUFF R248 1K 41 39 37 36 35 31 27 11 10 8 7 6 5 3 24 20 19 14 13 3_3V_SLEEP 5% 1/16W MF 603
NO STUFF R247 1K 5% 1/16W MF 603

IF UNPOWERED IIC BUS MESSES UP SDRAM ROMS, SWITCH TO 3.3V_SLEEP RAIL

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-0997 | REV. 01

SCALE NONE | SHT 35 OF 47

UNI_PU_RESET*: ASSERTED UNTIL SLEEP POWER AVAILABLE
UNI_RESET*: AS ABOVE, PLUS AT RESTART
MAIN_RESET*: ASSERTED UNTIL MAIN POWER AVAILABLE, PLUS AT RESTART
(ALSO USED FOR PCI DEVICES WHICH ARE NOT POWERED DURING SLEEP)
CPU_HRESET*: ASSERTED WHEN ALL PROCESSORS STOPPED
IO/RESET*: FOR KEYLARGO
(ALSO USED FOR PCI DEVICES WHICH REMAIN POWERED DURING SLEEP)

PMU SPEC: OPERATING: 2.2 TO 3.6 VOLTS
PROGRAMMING: 2.7 TO 3.6 VOLTS

39 37 33 29 5V_TRICKLE — D9 1N914 SOT23 — PMU_SCAP — MIN_LINE_WIDTH=25
4.5 TO 5.5V

VR3 SM
IN — VOLTAGE REGULATOR MC78LC33NTR — OUT
GND

MIN_LINE_WIDTH=25

R10 4.7 5% 1/16W MF 603 — PMU_AVCC 36

C162 2.2UF N20P80% 16V CERM 805 — PLACE NEAR REGULATOR
C2 0.1UF N20P80% 16V CERM 603 — PLACE NEAR PMU
C1 0.1UF N20P80% 16V CERM 603
C3 0.1UF N20P80% 16V CERM 603

D10 SM — MBR0540 — MIN_LINE_WIDTH=25
C295 0.1UF N20P80% 16V CERM 603
2 DIODES USED FOR DOUBLE ISOLATION BATTERY CHARGE PROTECTION U.L. REQUIREMENT
SCHOTTKY DIODES USED FOR LOW FORWARD DROP
D1 SM — MBR0540 — BATT — MIN_LINE_WIDTH=25

BT1 3.6V-850MAH — BATT — MIN_LINE_WIDTH=25 — TH

R363 10K 5% 1/16W MF 402
VCC
U903 SOT23-2.32V MAX6328
RESET
GND — VDET_3PIN

PMU_POWER 36 39

14 60 — VCC
97 — AVCC

PROTECT SWITCH FROM PITTING
R288 33 5% 1/16W MF 603 — PMU_RST_BUT — PMU_RSTDLY
S1 SM — SILKSCREEN "PMU RESET"
C222 0.047UF 5% 16V CERM 603

VDET_5PIN
VCC
U22 SM — DELAY — RESET
VOLTAGE DETECTOR MC33465N_22ATR
GND

R362 0 VDET_3PIN
IF 5 PIN VOLTAGE DETECTOR NOT PRESENT

3_3V_SLEEP
MAIN POWER DETECT
VCC — NO STUFF
U21 SM — PD_DLY — DELAY — RESET — PWR_FAIL* 36
R360 2.49K 1% 1/16W MF 603 — 2.49K/10K DROPS VOLTAGE TO 2.6V NOMINAL IF VOLTAGE DETECTOR NOT USED
C294 0.001UF 20% 50V CERM 603 — NO STUFF
VOLTAGE DETECTOR MC33465N_22ATR
R361 3.32K 1% 1/16W MF 603
GND
STUFF VOLTAGE DETECTOR IF PRECISE DETECTION NEEDED
CHOOSE APPROPRIATE TRIGGER VOLTAGE

R2 0 — 37 SLEEP — PMU_SLEEP
REMOVE TO DISABLE SLEEP MODE

R1 4.99K 1% 1/16W MF 603

SERIAL DOWNLOAD CONNECTOR
36 39 PMU_POWER
RP1 10K 5% 1/16W SM
DEVELOPMENT J7 SM

36 PMU_CNVSS	1	2	PMU_P64 36 39	(BUSY)
36 (CE*) PMU_AP	3	4	DOOR_AJAR 36	(SCLK)
	5	6	RESET_BUTTON* 36 39	(RXD)
36 PMU_RST*	7	8	NMI_BUTTON* 36 39	(TXD)
36 PMU_EPM* LOW FOR LOADING CODE	9	10		
	11	12		

RP1 10K 5% 1/16W SM

N.C. 86 P00_D0
N.C. 85 P01_D1
N.C. 84 P02_D2
N.C. 83 P03_D3
N.C. 82 P04_D4
N.C. 81 P05_D5
N.C. 80 P06_D6
N.C. 79 P07_D7
N.C. 78 P10_D8
N.C. 77 P11_D9
39 RUN_LED* 76 P12_D10
39 37 POWER_ON* 75 P13_D11
(BACKUP SELECT?) 74 P14_D12
39 29 14 PWR_SWITCH* 73 P15_D13_INT3
31 27 RING_DETECT* 72 P16_D14_INT4
27 KW_WATCHDOG* 71 P17_D15_INT5
N.C. 70 P20_A0_D0
N.C. 69 P21_A1_D1_D0
N.C. 68 P22_A2_D2_D1
N.C. 67 P23_A3_D3_D2
35 2 SMI<2>* 66 P24_A4_D4_D3
35 2 SMI<3>* 65 P25_A5_D5_D4
N.C. 64 P26_A6_D6_D5
N.C. 63 P27_A7_D7_D6
PORTABLE_DESKTOP* 61 P30_A8_D7
LOW INDICATES DESKTOP SYSTEM
N.C. 59 P31_A9
24 IO_RESET* 58 P32_A10
N.C. 57 P33_A11
N.C. 56 P34_A12
N.C. 55 P35_A13
N.C. 54 P36_A14
N.C. 53 P37_A15
27 PMU_INT* 52 P40_A16
51 P41_A17
2 CPU0_PLL_STOP 50 P42_A18
2 CPU1_PLL_STOP 49 P43_A19
48 P44_CS0
27 KW_SUSPEND_REQ* 47 P45_CS1
3 UNI_SUSPEND_ACK* 46 P46_CS2
3 UNI_SUSPEND_REQ* 45 P47_CS3

R287 1K 5% 1/16W MF 603 — R
DRIVEN OPEN COLLECTOR
NO NEED TO VOLTAGE CONVERT

PMU_BYTE 6 — BYTE
PMU_XO1 11 — XOUT
PMU_XI1 13 — XIN
36 PMU_RST* 10 — RESET
36 PMU_AVCC 96 — VREP
36 PMU_CNVSS 7 — CNVSS
6 12 62 — VSS
94 — AVSS

R359 33 5% 1/16W MF 603
R355 1K 5% 1/16W MF 603
RP2 10K 5% 1/16W SM
PMU_XO1B
R358 5.1M 5% 1/16W MF 603
Y1 10.0000M
C292 33PF 10% 50V CERM 603
C293 15PF 5% 50V CERM 603

OMIT
U20 M16C62 FLAS-1

P50_WRL_WR	44	PMU_AP 36 ALSO CE* FOR LOADING CODE
P51_WRH_BHE	43	UNI_RESET* 19 38
P52_RD	42	MAIN_RESET* 9 12 13 14 33 41
P53_BCLK	41	SMI<1>* 2 35
P54_HLDA	40	PMU_NMI* 27 35
P55_HOLD	39	PMU_EPM* 36
P56_ALE	38	UNI_PU_RESET* 19
P57_RDY_CLKOUT	37	CPU_HRESET* 2 4
P60_CTS0_RTS0	36	PMU_ACK* 27
P61_CLK0	35	PMU_SCK 27
P62_RXD0	34	PMU_MISO 27
P63_TXD0	33	PMU_MOSI 27
P64_CTS1_RTS1_CTS0_CLKS1	32	36 PMU_P64 ALSO "BUSY" FOR LOADING CODE
P65_CLK1	31	DOOR_AJAR 36 39 ALSO SCLK FOR LOADING CODE
P66_RXD1	30	RESET_BUTTON* 36 39 ALSO "RXD" FOR LOADING CODE
P67_TXD1	29	NMI_BUTTON* 36 39 ALSO "TXD" FOR LOADING CODE
P70_TXD2_SDA_TA0OUT	28	N.C.
P71_RXD2_SCL_TA0IN_TB5IN	27	N.C.
P72_CLK2_TA1OUT_V	26	UNI_CLK_EN
P73_CTS2_RTS2_TA1IN_V	25	CPU CLOCK OE (NOT USED)
P74_TA2OUT_W	24	N.C.
P75_TA2IN_W	23	N.C.
P76_TA3OUT	22	N.C.
P77_TA3IN	21	N.C.
P80_TA4OUT_U	20	SLEEP_LED* 39
P81_TA4IN_U	19	SMI<0>* 2 35
P82_INT0	18	PWR_FAIL* 36
P83_INT1	17	
P84_INT2	16	KW_PEND_PROC_INT 27
P85_NMI	15	PMU_PU
P86_XCOUT	9	PMU_XO2
P87_XCIN	8	PMU_XI2
P90_TB0IN_CLK3	5	
P91_TB1IN_SIN3	4	
P92_TB2IN_SOUT3	3	N.C.
P93_DA0_TB3IN	2	N.C.
P94_DA1_TB4IN	1	KW_PROC_SLEEP_REQ* 27
P95_ANEX0_CLK4	100	
P96_ANEX1_SOUT4	99	N.C.
P97_ADTRG_SIN4	98	PMU_PD1
P100_AN0	95	(THERMISTOR)
P101_AN1	93	TRICKLE_DETECT
P102_AN2	92	
P103_AN3	91	N.C.
P104_AN4_KI0	90	PMU_IIC_CLK 16 18 35
P105_AN5_KI1	89	PMU_IIC_DAT 16 18 35
P106_AN6_KI2	88	PMU_SMB_SCK
P107_AN7_KI3	87	PMU_SMB_SDA

J8 TH — DEVELOPMENT — UNRELEASED — PMU_REQ* 27
PROVIDE ISOLATION WHEN LOADING CODE

3_3V_SLEEP
R3 0
RP2 10K 5% 1/16W SM

S2 SM — PME* 9 13 14 19 20 27 38
DEVELOPMENT
FORCE POWER MANAGEMENT EVENT

OK TO POWER UP SIGNAL — POWERUP_OK 2

3_3V_TRICKLE
R5 2.49K 1% 1/16W MF 603
R9 3.32K 1% 1/16W MF 603
R8 1K 5% 1/16W MF 603
R6 10K 5% 1/16W MF 402
R7 10K 5% 1/16W MF 402

R357 160K 5% 1/16W MF 603
NO STUFF
R356 5.1M 5% 1/16W MF 603
PMU_XO2B
Y2 SM — 32.768K
C290 10PF 5% 50V CERM 603
C291 22PF 5% 50V CERM 603

R11 10K 5% 1/16W MF 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
820-1173	1	BARE PCB	X0	
525-0057	1	BATTERY HOLDER	BT1	
341S0591	1	IC, PWR MGR 99, 64K FLSH	U20	
613-3290	0	GEN DWG, MLB		
825-2029	1	LABEL, SERIAL	X14	
725-0144	1	MYLAR BATTERY INSULATOR	BT1	

POWER MANAGEMENT UNIT

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-0997	01
	SCALE: NONE	SHT 36 OF 47	

CR-37

SYSTEM MODE	POWER_ON*	SLEEP
RUN	0	0
SLEEP	X	1
SHUTDOWN	1	0

D.C. TERMINATION POWER SUPPLY

VERIFY POWER RAILS

+3.3V
R275 1.27K 1% 1/16W MF 603 — TERM3
R277 2.49K 1% 1/16W MF 603 — TERM1
C207 100PF 5% 50V CERM 603 — TERM4
R276 3.01K 1% 1/16W MF 603 — TERM2
R270 2.49K 1% 1/16W MF 603
R278 3.01K 1% 1/16W MF 603
R268 1K 1% 1/16W MF 603 — TERM8
R267 49.9 1% 1/16W MF 603
U12 TS922ID SOI
Q7 SI9426DY SOI
OVERKILL
R497 0.1 1% 1W WW 2512 — 1_8V_TERM 8 — MIN_LINE_WIDTH=25
Q6 SM SI4467DY
5V_TRICKLE

+5V
R166 100K 5% 1/16W MF 603 — RC=1MSEC SLOW TURNON
C163 0.01UF 20% 50V CERM 402

Q9 SI2302DS SM — FET OFF WHEN 5V RAIL OFF
1_8V_TO_PROC 2 — MIN_LINE_WIDTH=25
N-CHANNEL

PUT CURRENT LIMIT RESISTOR?
Q21 MTD15N06V SM
R500 10K 5% 1/16W MF 402
5V_TRICKLE 3_3V_SLEEP
MIN_LINE_WIDTH=25
1.82 - 1.90 VOLTS
1_8V_SLEEP 6 10 19 20 — MIN_LINE_WIDTH=25 — WIDER YET?
C409 150UF 20% 6.3V TANT SMD POSCAP — MOVE CLOSER TO UNI_N CORE? IF NEEDED FOR STABILITY
R274 2.49K 1% 1/16W MF 603
NO STUFF
C410 0.01UF 20% 50V CERM 402 — PRC17
PULLUP TO ENGURE TURN-ON OF 1.8V POWER SUPPLY
PRC15
U13 TLV431A SOT
NO STUFF
R499 4.99K 1% 1/16W MF 603
R70 100K 5% 1/16W MF 603 — STUFF TO GET 1.89V NOMINAL

+3.3V
Q22 SI4467DY SM — FET ON IN RUN
5V_TRICKLE
R503 470 1% 1/16W MF 603
3_3V_TRICKLE
RP132 100K 5%
VB1
LM339A SOI
U33 GND
39 37 36 POWER_ON*
37 36 SLEEP
PRC1
PRC20
R502 1K 5% 1/16W MF 603
LM339A SOI
U33 GND
PRC2
R504 47.0K 1% 1/16W MF 603

MIN_LINE_WIDTH=25
3_3V_SLEEP 3 6 7 8 10 11 13 14 19 20 24 27 31 35 36 37 39 41
C413 150UF 20% 6.3V TANT SMD — POSCAPS
NO STUFF
C412 150UF 20% 6.3V TANT SMD
NEED LOW ESR TO KEEP VOLTAGE DROOP LOW WHEN SWITCHING BETWEEN RAILS

TERM7
U12 TS922ID SOI
37 TERM2

FET ON IN SLEEP
Q900 SI4467DY
POWER DISSIPATION 2.4W AT 1.4A
POUR COPPER FOR HEAT SINK
MIN_LINE_WIDTH=25
1.5 AMP CURRENT RATING
P-CHANNEL
R(ON) = 11 MOHMS
5V_TRICKLE
SENSE VR901 CS5253 SM
VPWR VOUT
VCTRL VOUT
ADJ TAB
R985 124 1% 1/16W MF 603
3.30 - 3.46 VOLTS
3_3V_TRICKLE 2 22 36 37 39
3_3V_ADJ
C983 100UF 20% 6.3V ELEC SM
C984 0.1UF N20P80% 16V CERM 603
R986 210 1% 1/16W MF 603
C985 150UF 20% 6.3V TANT SMD POSCAP

3_3V_TRICKLE
RP105 100K 5% 1/16W SM
R269 47.0K 1% 1/16W MF 603
37 36 SLEEP
PRC13
R271 47.0K 1% 1/16W MF 603
39 37 36 POWER_ON*
PRC14
RP105 100K 5% 1/16W SM
RUN -> LOW
SLEEP -> LOW
SHUTDOWN -> FLOAT
LM339A SOI
U33 GND
R164 100K 5% 1/16W MF 603
FET ON DURING SHUTDOWN
Q24 SI2302DS SM
C33 0.01UF 20% 50V CERM 402
R498 10 5% 1/16W MF 603

3_3V_TRICKLE
RP104 100K 5%
37 36 SLEEP
39 37 36 POWER_ON*
PRC4
PRC5
PRC6
LM339A SOI
V- U33 GND
PRC18
RP105 100K 5% 1/16W SM
R501 1K 5% 1/16W MF 603
R165 100K 5% 1/16W MF 603 — RC=1MSEC SLOW TURNON
FET OFF IN SHUTDOWN
Q8 SI4467DY SM
C153 0.01UF 20% 50V CERM 402
5V_SLEEP 20 24 27 29 30 31
MIN_LINE_WIDTH=25
P-CHANNEL

3_3V_SLEEP GROUND_CIRCUITRY

PREVENT POWER RAIL PUMP-UP BY ROGUE SELF-POWERED USB DEVICES

POWER RAIL CONTROL

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-0997	REV. 01
	SCALE NONE	SHT 37 OF 47	

10/100/GBIT ETHERNET PHY

U900
BCM5401
(2 OF 2)
PBGA

U2
BCM5201
FLAS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
805-2266	1	HEAT SINK, GBIT PHY	U900	EN_GBIT

NETS WITH SERIES RESISTOR AT UNI-N = 4500-5000
NETS WITH SERIES RESISTOR AT PHY = 4600-5100

PLACE SPARKS UNDER U900

VALUE CHANGED FROM 10K TO BE SIMILAR TO P1 SCHEMATIC

ASSUMES ALL DRIVERS WHICH WISH TO INDICATE INTERRUPT DURING SLEEP MODE DRIVE TO GROUND RAIL

PLACE THESE CAPS AS CLOSE AS POSSIBLE TO THE A_VDD PINS.

PLACE THESE CAPS AS CLOSE AS POSSIBLE TO THE D_VDD PINS.

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CR-39

NOTCH THIS SIDE

PIN 4: +5V, USED TO BE POWERGOOD SIGNAL
POWERGOOD DRIVEN LOW BY SERVER POWER SUPPLY
IF RUNNING IN REDUNDANT MODE
OUTPUT IS SHORT-CIRCUIT PROTECTED FOR YOSEMITE COMPATIBILITY

POWER SUPPLY CONNECTOR

3_3V_TRICKLE

R128 4.99K 1% 1/16W MF 603

R126 10K 5% 1/16W MF 402

R127 47.0K 1% 1/16W MF 603

POWER SUPPLY REQUIRES 5 MA SINK CAPABILITY, PMU ONLY RATED FOR 1 MA.

PWR_UP

Q19 2N3904 SM

Q20 2N3904 SM

POWER_UP_F*

-12V

+5V

+3.3V

MIN_LINE_WIDTH=25

C84 47UF 20% 16V ELEC SM

CON_M22ST_HTEMP (517-0883)

J25 TH

C109 150UF 20% 6.3V TANT SMD POSCAP

C110 100UF 20% 6.3V ELEC SM

C11 100UF 20% 25V ELEC SM

C370 0.01UF 20% 50V CERM 402

J19 TH

28V_TRICKLE

MIN_LINE_WIDTH=100

12VUNPROT

C191 47UF 20% 16V ELEC SM

F5 2AMP-15V

+12V

XW7 SM

XW6 SM

PLACE NEAR POWER CONNECTOR

FAN_PWR 2

FAN_GND 2

R517 240 5% 1W FF 2512

R494 240 5% 1W FF 2512 0.6W EACH

R493 240 5% 1W FF 2512

PMU_POWER

39 37 36 22 2 3_3V_TRICKLE

RP97 10K 5% 1/16W SM

12V LOAD TO KEEP POWER SUPPLY WITHIN REGULATION
SPREAD RESISTORS OUT TO ISOLATE THERMALLY

PROVIDE ISOLATION FOR SERIAL DATA WHEN CODE DOWNLOADED

RP96 470 5% 1/16W SM

36 NMI_BUTTON* — NMI_BUT*
36 RESET_BUTTON* — RESET_BUT*
36 29 14 PWR_SWITCH* — PWR_BUT*
36 DOOR_AJAR — DOOR_SWITCH

FRONT PANEL BOARD CONNECTOR

J30 M-ST-HDRF TH (515-1380)

PRI_LED

N.C.

29 33 36 37 39 5V_TRICKLE

27 24 20 19 14 13 11 10 8 7 6 3 41 37 36 35 31 3_3V_SLEEP

OLD_FPB Q4 2N3906 SM

OLD_FPB R495 4.99K 1% 1/16W MF 603

36 RUN_LED* GREEN LED (ON)

PRI_LED_B

CURRENT LIMIT FOR LEDS ON FPB

OLD_FPB Q5 2N3906 SM

OLD_FPB R496 4.99K 1% 1/16W MF 603

36 SLEEP_LED* YELLOW LED (SLEEP)

SEC_LED_B

SEC_LED

NO STUFF C405 0.01UF 20% 50V CERM 402

NO STUFF C407 0.01UF 20% 50V CERM 402

NO STUFF C408 0.001UF 20% 50V CERM 603

NO STUFF C417 0.001UF 20% 50V CERM 603

LIMIT VALUE OF CAPS ON RESET AND NMI SIGNALS TO PREVENT INTERFERENCE WITH DOWNLOADING CODE

LOWER_CHASSIS

39 25

NO STUFF C406 0.01UF 20% 50V CERM 402

NO STUFF C404 0.01UF 20% 50V CERM 402

NO STUFF C164 0.01UF 20% 50V CERM 402

LOWER_CHASSIS

39 25

37 36 33 29 5V_TRICKLE

NEW_FPB R172 10K 5% 1/16W MF 402

14 DISPLAY_LED

NEW_FPB Q25 2N7002 SM

39 37 36 33 29 5V_TRICKLE

NEW_FPB R178 10K 5% 1/16W MF 402

NEW_FPB Q26 2N7002 SM

14 23 39 28V_TRICKLE

R156 1K 1% 1/16W MF 603

5V_TRKL_FB

5V_TRKL_BST

FB

VR4 LM2679 SM

VIN

BST

SFTSTART

S_OUT

ADJ GND GND1

5V_TRKL_SS

5V_TRKL_SOUT

5V_TRKL_ADJ

C27 1UF 20% 50V CERM 1812

C28 1UF 20% 50V CERM 1812

C115 1UF 20% 50V CERM 1812

C116 1UF 20% 50V CERM 1812

C117 0.01UF 20% 50V CERM 402

R159 240K 5% 1/16W MF 603

R163 3.32K 1% 1/16W MF 603

L16 10UH SM-5

VOUT=5.15V

5V_TRICKLE 29 33 36 37 39

NO STUFF

C118 330UF 20% 6.3V TANT SMD POSCAP

C119 330UF 20% 6.3V TANT SMD POSCAP

NO STUFF

R157 47K 5% 1/16W MF 603

R158 6.19K 1% 1/16W MF 603

D4 TO252 5.5A-40V

POWER SUPPLY CONNECTOR / FRONT PANEL INTERFACE / 28V TO 5V TRICKLE P/S

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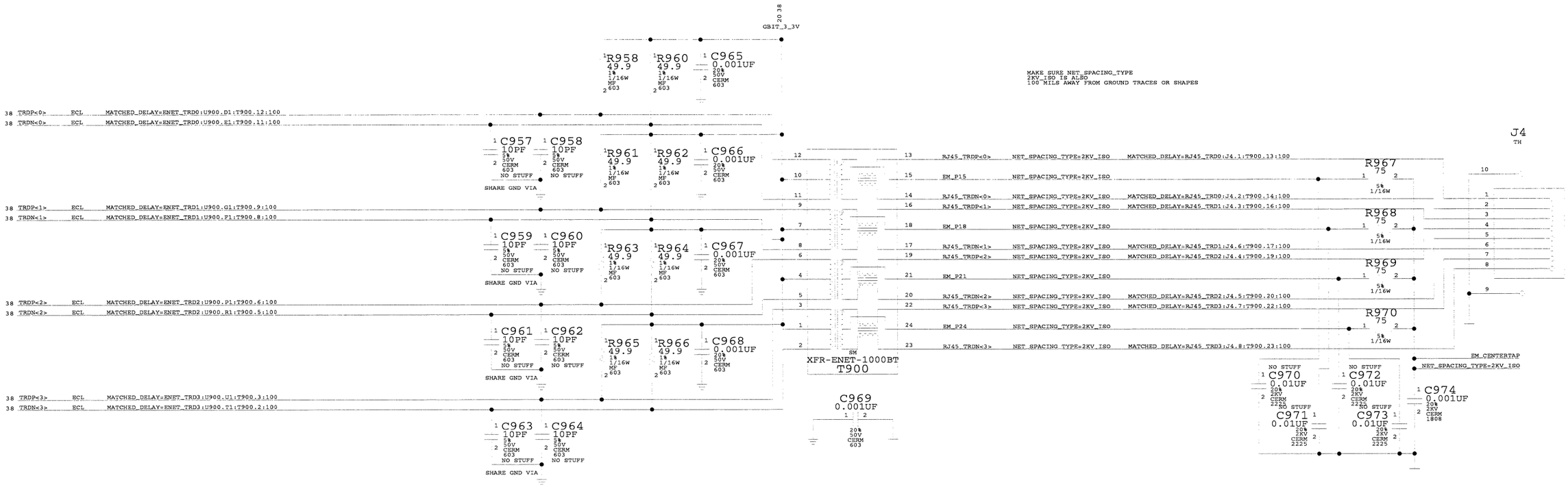
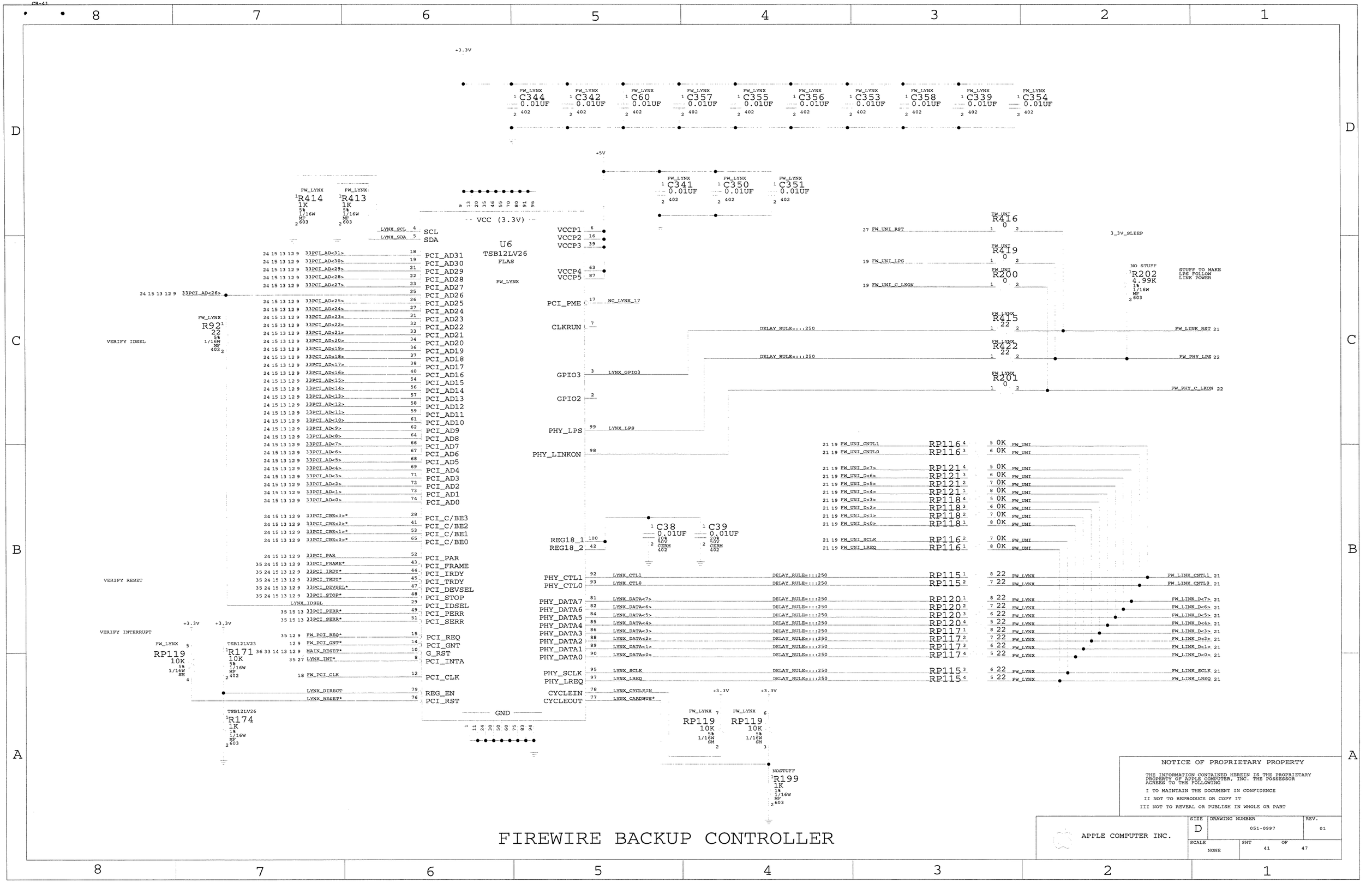


38 TRDP<0> ECL MATCHED_DELAY=ENET_TRD0:U900.D1:T900.12:100
38 TRDN<0> ECL MATCHED_DELAY=ENET_TRD0:U900.E1:T900.11:100
38 TRDP<1> ECL MATCHED_DELAY=ENET_TRD1:U900.G1:T900.9:100
38 TRDN<1> ECL MATCHED_DELAY=ENET_TRD1:U900.F1:T900.8:100
38 TRDP<2> ECL MATCHED_DELAY=ENET_TRD2:U900.P1:T900.6:100
38 TRDN<2> ECL MATCHED_DELAY=ENET_TRD2:U900.R1:T900.5:100
38 TRDP<3> ECL MATCHED_DELAY=ENET_TRD3:U900.U1:T900.3:100
38 TRDN<3> ECL MATCHED_DELAY=ENET_TRD3:U900.T1:T900.2:100

13 RJ45_TRDP<0> NET_SPACING_TYPE=2KV_ISO MATCHED_DELAY=RJ45_TRD0:J4.1:T900.13:100
15 EM_P15 NET_SPACING_TYPE=2KV_ISO
14 RJ45_TRDN<0> NET_SPACING_TYPE=2KV_ISO MATCHED_DELAY=RJ45_TRD0:J4.2:T900.14:100
16 RJ45_TRDP<1> NET_SPACING_TYPE=2KV_ISO MATCHED_DELAY=RJ45_TRD1:J4.3:T900.16:100
18 EM_P18 NET_SPACING_TYPE=2KV_ISO
17 RJ45_TRDN<1> NET_SPACING_TYPE=2KV_ISO MATCHED_DELAY=RJ45_TRD1:J4.6:T900.17:100
19 RJ45_TRDP<2> NET_SPACING_TYPE=2KV_ISO MATCHED_DELAY=RJ45_TRD2:J4.4:T900.19:100
21 EM_P21 NET_SPACING_TYPE=2KV_ISO
20 RJ45_TRDN<2> NET_SPACING_TYPE=2KV_ISO MATCHED_DELAY=RJ45_TRD2:J4.5:T900.20:100
22 RJ45_TRDP<3> NET_SPACING_TYPE=2KV_ISO MATCHED_DELAY=RJ45_TRD3:J4.7:T900.22:100
24 EM_P24 NET_SPACING_TYPE=2KV_ISO
23 RJ45_TRDN<3> NET_SPACING_TYPE=2KV_ISO MATCHED_DELAY=RJ45_TRD3:J4.8:T900.23:100

10/100/GBIT ETHERNET MAGNETICS AND CONNECTOR

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-0997	01
	SCALE	SHT	OF
	NONE	40	47



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FIREWIRE BACKUP CONTROLLER

UATA0A<2..0>	26
UATA0CHRDY	26
UATA0D<15..0>	26
UATA0DCSELP*	26
UATA0DMACK*	24 26
UATA0IOCS16*	26
UATA0IRQ	26
UATA0REQ	26
UATA0_INUSE*	26
UATA0_INUSE1*	26
UATAD<15..0>	26
UATADETECT*	26 27
UATARESET*	24
UATA_CS1*	24 26
UATA_CS3*	24 26
UDMACK0*	24
UDMARQ0	24 26
UDSA<2..0>	24 26
UDSD<15..0>	24 26
UDSTB0/DRDY0*	24 26
UD_CS1*	26
UD_CS3*	26
UHSTB0/RDY0*	24
UINTA0*	24 26
UNI_AB6	3
UNI_AGP_AVDD	11
UNI_CLK_EN	36
UNI_EXT_PCICLK	11 18
UNI_H6	12
UNI_IIC_CLK	2 7 8 19 35
UNI_IIC_DAT	2 7 8 19 35
UNI_INT_PCICLK	12 18
UNI_MAX_AVDD	3
UNI_MAX_DVDD	3
UNI_PCIPHASE	12 18
UNI_PU1	19 35
UNI_PU2	19 35
UNI_PU_RESET*	19 36
UNI_PU_RST*	19
UNI_RESET*	19 36 38
UNI_ROMCS*	6
UNI_ROMOE*	6
UNI_ROMWE*	6
UNI_RST*	19
UNI_SUSPEND_ACK*	3 36
UNI_SUSPEND_REQ*	3 36
UNI_TDO	19 27
UNI_TEI	19
UNI_TRST*	19
USB_DAM	27 28
USB_DAM_EMI	28
USB_DAM_F	28 29
USB_DAP	27 28
USB_DAP_EMI	28
USB_DAP_F	28
USB_DBM	27 28
USB_DBM_F	14 28 29
USB_DBP	27 28
USB_DBP_F	14 28
USB_DCM	27 28
USB_DCM_EMI	28
USB_DCM_F	28 29
USB_DCP	27 28
USB_DCP_EMI	28
USB_DCP_F	28
USB_DDM	27 28
USB_DDM_F	28 31
USB_DDP	27 28
USB_DDP_F	28 31
USB_GND1	28 30
USB_GND2	28 30
USB_PWR1	28 30
USB_PWR2	28 30
USB_PWR_CNTRL0	27
USB_PWR_CNTRL1	27
USB_PWR_FAULT0*	27
USTOP0	24
VB1	37
WE_A*	6 7 8
WRHP_RETURN	33
WT*	2 3 5
ZD12	16
ZD13	16
ZD14	16
ZD15	16
ZD16	16
ZD17	16
ZD20	18
ZD21	18
ZD22	18
ZD23	18
ZD24	18

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SIZE	DRAWING NUMBER	REV.
D	?	?
SCALE NONE	SHT 48 OF ?	

*** Unit Cross-Reference ***
--- for the entire design --

BT1	BATTERY	36
C1	CAP	36
C2	CAP	36
C3	CAP	36
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C985	CAP_P	37
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D2	DIODE_3P_C	23
D4	DIODE_3P_C	39
D9	DIODE	36
D10	DIODE_SCHOT	36
D900	DIODE	38
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F5	FUSE	39
G1	OSC	27
J1	CON_STEREO3	33
J2	CON_STEREO4_X5	32
J3	CON_F8RT_USB_DUAL_SHLD	28
J4	CON_RJ45_SHORT	40
J5	CON_FWVERT_SKT	22
J6	CON_FWVERT_SKT	22
J7	CON_M12ST_SM	36
J8	CON_M2ST_100P	36
J9	CON_F6ST_HTEMP	14
J10	CON_64_5V_ST	13
J11	CON_64_5V_ST	13
J12	CON_64_5V_ST	13
J13	CON_5JKSMA_200	27
J14	CON_5JKSMA_200	18
J15	CON_M40ST_NC20	26
J16	CON_132ST_AGP	14
J17	CON_F80ST_D2MT_SM	9
J18	CON_F20SM_KX	4
J19	CON_F48T_D_TH	39
J20	CON_5JKSMA_200	16
J21	CON_168ST_UDRM	7
J22	CON_168ST_UDRM	7
J23	CON_168ST_UDRM	8
J24	CON_5JKSMA_200	17
J25	CON_M22ST_HTEMP	39
J26	CON_F80ST_D2MT_SM	9
J27	CON_M40SM_635	31
J29	CON_F10X30_07_11_00	2
J30	CON_M10ST_HDRF	39
J31	CON_M2RT_HDRF	34
J32	CON_68_PCMCIA	31
J33	CON_M40RT_NC20	25
J35	CON_4ST_AMPIN	19
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Q2	TRA_2N7002	29
Q3	TRA_MTD15N06V	14
Q4	TRA_2N3906	39
Q5	TRA_2N3906	39
Q6	TRA_SI4467DY	37
Q7	TRA_SI9426DY	37
Q8	TRA_SI4467DY	37
Q9	TRA_SI2302DS	37
Q11	TRA_2N7002	14
Q12	TRA_TP0610	33
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Q27	TRA_SI4401DY	23
Q900	TRA_SI4467DY	37
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R11	RES	36

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER ?	REV. ?
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RP909	RPAK4P	38
RP912	RPAK4P	19
S1	SWI_TACT_4SM	36
S2	SWI_TACT_4SM	36
S3	SWI_4_LOPRO	16
T2	FILTER_CHOKE_DUAL	22
T3	FILTER_CHOKE_DUAL	22
T900	XFR_ENET_1000BT	40
U1	SCREAMER	33
U2	TRANSCEIVER_ENET_BCM5201	38
U3	PW802	22
U4	SHNTREG_TLV431A	14
U6	TSB12LV26	41
U7	FEPR_1MX8	9
U12	OPAMP_TS922ID	37
U13	SHNTREG_TLV431A	37
U16	COMPARATOR_LM339A	29
U17	AUDIO_LM4861	34
U20	M16C62	36
U21	VDET_MC33465N_22ATR	36
U22	VDET_MC33465N_22ATR	36
U25	KEYLARGO	24 27
U27	CLK_GEN_IMIC5003	16
U28	UNI_N_658P	3 6 11 12 19
U33	COMPARATOR_LM339A	37
U800	CLK_GEN_IMIC5002	18
U900	TRANSCEIVER_ENET_BCM5401	20 38
U903	MAX6328	36
VR1	VREG_78M05	33
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VR4	VREG_LM2679	39
VR900	VREG_CS5253_ADJ	20
VR901	VREG_CS5253_ADJ	37
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Y3	CRYSTAL	38
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ZH11	MTGHOLE	2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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R77	RES	16
R78	RES	22
R79	RES	22
R80	RES	26
R81	RES	13
R82	RES	13
R83	RES	13
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R85	RES	27
R86	RES	27
R87	RES	24
R88	RES	24
R89	RES	24
R90	RES	27
R91	RES	11
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R105	RES	26
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R118	RES	27
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R139	RES	6
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R149	RES	14
R150	RES	16
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R152	RES	16
R153	RES	16
R154	RES	30
R155	RES	30
R156	RES	39
R157	RES	39
R158	RES	39
R159	RES	39
R160	RES	16
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R164	RES	37
R165	RES	37
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R167	RES	16
R168	RES	16
R169	RES	16
R170	RES	29
R171	RES	39
R172	RES	39
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R175	RES	19
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R182	RES	35
R183	RES	31
R184	RES	16
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R187	RES	16
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R189	RES	16
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R472	RES	4
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R814	RES	18
R815	RES	18
R816	RES	18
R817	RES	18
R818	RES	18
R819	RES	18
R820	RES	18
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R824	RES	18
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R843	RES	12
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R970	RES	40
R971	RES	38
R972	RES	38
R985	RES	37
R986	RES	37
R987	RES	19
RP1	RPAK4P	36
RP2	RPAK4P	36
RP3	RPAK4P	33
RP4	RPAK4P	33
RP5	RPAK4P	16
RP8	RPAK4P	16
RP9	RPAK4P	33
RP10	RPAK4P	29
RP11	RPAK4P	21
RP12	RPAK4P	21
RP13	RPAK4P	26
RP14	RPAK4P	26
RP15	RPAK4P	26
RP16	RPAK4P	35
RP17	RPAK4P	35
RP18	RPAK4P	24
RP19	RPAK4P	35
RP20	RPAK4P	35
RP21	RPAK4P	16
RP22	RPAK4P	16
RP32	RPAK4P	35
RP35	RPAK4P	26
RP36	RPAK4P	35
RP37	RPAK4P	35
RP38	RPAK4P	14
RP39	RPAK4P	14
RP40	RPAK4P	35
RP41	RPAK4P	35
RP42	RPAK4P	35
RP43	RPAK4P	35
RP55	RPAK4P	35
RP60	RPAK4P	35
RP61	RPAK4P	35
RP62	RPAK4P	35
RP63	RPAK4P	35
RP64	RPAK4P	35
RP65	RPAK4P	14
RP83	RPAK4P	35
RP84	RPAK4P	35
RP85	RPAK4P	35
RP86	RPAK4P	19
RP87	RPAK4P	19
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RP89	RPAK4P	19
RP90	RPAK4P	19
RP91	RPAK4P	19
RP93	RPAK4P	35
RP94	RPAK4P	35
RP95	RPAK4P	35
RP96	RPAK4P	39
RP97	RPAK4P	39
RP100	RPAK4P	25
RP101	RPAK4P	25
RP102	RPAK4P	25
RP103	RPAK4P	25
RP104	RPAK4P	37
RP105	RPAK4P	37
RP112	RPAK4P	35
RP114	RPAK4P	14
RP115	RPAK4P	41
RP116	RPAK4P	41
RP117	RPAK4P	41
RP118	RPAK4P	41
RP119	RPAK4P	41
RP120	RPAK4P	41
RP121	RPAK4P	41
RP123	RPAK4P	35
RP132	RPAK4P	37
RP900	RPAK4P	38
RP901	RPAK4P	38
RP902	RPAK4P	38
RP905	RPAK4P	38
RP906	RPAK4P	38
RP907	RPAK4P	38
RP908	RPAK4P	38
RP909	RPAK4P	38
RP911	RPAK4P	20
RP912	RPAK4P	19
S1	SWI_TACT_4SM	36
S2	SWI_TACT_4SM	36
S3	SWI_4_LOPRO	16
T2	FILTER_CHOKE_DUAL	22
T3	FILTER_CHOKE_DUAL	22
T900	XFR_ENET_1000BT	40
U1	SCREAMER	33
U2	TRANSCEIVER_ENET_BCM5201	38
U3	FW803	22
U4	SHNTREG_TLV431A	14
U6	TSB12LV26	41
U7	FEPR_1MX8	9
U12	OPAMP_TS922ID	37
U13	SHNTREG_TLV431A	37
U16	COMPARATOR_LM339A	29
U17	AUDIO_LM4861	34
U20	M16C62	36
U21	VDET_MC33465N_22ATR	36
U22	VDET_MC33465N_22ATR	36
U25	KEYLARGO	24 27
U27	CLK_GEN_IMIC5003	16
U28	UNI_N_658P	3 6 11 12 19
U33	COMPARATOR_LM339A	37
U800	CLK_GEN_IMIC5002	18

U900	TRANSCEIVER_ENET_BCM5401	20 38
U903	MAX6328	36
VR1	VREG_78M05	33
VR2	VREG_MIC2951	27
VR3	VREG_MC78LC33NTR	36
VR4	VREG_LM2679	39
VR900	VREG_CS5253_ADJ	20
VR901	VREG_CS5253_ADJ	37
XW2	SHORT	33
XW3	SHORT	33
XW4	SHORT	33
XW5	SHORT	27
XW6	SHORT	39
XW7	SHORT	39
XW8	SHORT	32
XW9	SHORT	33
XW10	SHORT	33
XW12	SHORT	33
XW13	SHORT	33
XW14	SHORT	33
Y1	CRYSTAL	36
Y2	CRYSTAL_4PIN	36
Y3	CRYSTAL	38
Y4	CRYSTAL	22
Y6	CRYSTAL	16
Y800	CRYSTAL	18
Y900	CRYSTAL	38
ZH1	MTGHOLE	22
ZH5	MTGHOLE	22
ZH6	MTGHOLE	33
ZH7	MTGHOLE	33
ZH9	MTGHOLE	27
ZH10	MTGHOLE	2
ZH11	MTGHOLE	2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	?	?
SCALE	SHT	OF
NONE	251	?

REVISION HISTORY

P21 DESIGN BASED ON P10 DESIGN, 820-????

8/29/99
CHANGE REFERENCE DESIGNATORS ON UNI-N PLL FILTER SERIES ELEMENTS FROM L TO R

9/17/99
REPLACED 10/100 ETHERNET LAYOUT WITH 05 EVT+ GBIT LAYOUT ON PAGES 19, 20, 38, & 40.
CHANGED ALL REF NUMBERS OF NEW PARTS TO START AT 900 ON THE GGIT PAGES ADDED ABOVE.
USB SLEEP MODE CURRENT LIMIT ISSUE (RFA 110509) ON PAGE 30:
CHANGED RP5 FROM 100K TO 4.7K
CHANGED R328 FROM 4.99K TO 470
CHANGED R32 FROM 1 TO 0.200

9/28/99
ADDED ADDITIONAL I/O FENCE MOUNTING HOLE
CORRECT GBIT BOM OPTIONS
DELETE R423 AND R424 (21143 SERIES RESISTORS)
CHANGE INDUCTORS ON BCM5201 TRANSMIT PAIR TO 0 OHM RESISTORS

10/6/99
FIX CONSTRAINTS ON TRACES GOING TO GBIT TRANSFORMER
FIX CONSTRAINT ON STAR1 NET
CHANGE GBIT LINK-PHY CONSTRAINTS TO EASE ROUTING

10/7/99
REMOVE CD ANALOG INPUT AND DVD HARDWARE TO MAKE ROOM FOR PROCESSOR MOUNTING HOLE

10/13/99
REPLACE USB POWER CIRCUITRY TO USE 5V_TRICKLE ALWAYS, AND TPS2031 CURRENT LIMITERS
ADD BOM OPTIONS FOR UNI 1.0.7 VERSUS 1.0.8 MEMORY TIMING
ELIMINATE KEYWEST/KEYLARGO BOM OPTIONS

10/15/99
CHANGE 10 MHZ PMU XTAL FROM 197S0604 TO 197S0154 (HIGHER PROFILE)
ADD BOM OPTIONS TO PULLUP/PULLDOWN ON UNI-N F/W PHY RESET SIGNAL
ELIMINATE DUPLICATE FILTERING FOR USB POWER SWITCH INPUTS

10/20/99
ADD GBIT_DEV BOM OPTION TO ALLOW STUFFING OF GBIT LEDS WITHOUT OTHER DEV STUFF

10/22/99
ADD HEAT SINK FOR GBIT PHY

10/28/99 REV 01
UPDATE SCHEMATIC AND RFA NUMBERS
BUMP GBIT CORE VOLTAGE FROM 2.5 TO 2.6 VOLTS
UPDATE PARTNUMBER OF BOOT ROOM

11/3/99
ADD STUFFING OPTION TO ALLOW 48 MHZ UNI-N INTERNAL PCI BUS OPERATION
REMOVE EXTRA I/O FENCE MOUNTING HOLE AGAIN

11/17/99
CHANGE 32 KHZ PMU XTAL CIRCUIT TO INCREASE CAPACITIVE LOADING

11/18/99
CORRECT SIGNAL NAME FROM ETHERNET_PHY_RST* TO UNI_RESET*
ADD MISSING PULLUP BACK IN TO KEYLARGO GPIO16
BEEF UP 3.3V TRICKLE REGULATOR (CHANGE LT1117 TO CS5253)
BEEF UP 3.3V SLEEP FET (CHANGE SI2301 TO SI4467)

11/19/99
ADD STUFFING OPTION FOR ALTERNATE PMU VOLTAGE DETECTOR
ADD BOM OPTION FOR SYNCHRONIZING UNI-N INTERNAL PCI TO FIREWIRE PHY

12/15/99
CORRECT PART NUMBER ON THREE TERMINAL VOLTAGE DETECTOR FOR PMU POWER
ADD MYLAR INSULATOR TO KEEP PMU UNPOWERED DURING ASSEMBLY

1/4/00
CHANGE UNI-N PART NUMBER TO 1.09
CHANGE REVISION TO A

1/7/00
CHANGE BOOT ROM PART NUMBER TO T NUMBER

1/13/00
CHANGE UNI-N PART NUMBER TO T NUMBER

2/2/00 (RT)
CHANGE UNI-N TO UNI-N 1.5
REMOVE DEC21154
REMOVE 4TH DIMM SLOT
REMOVE CKE BUFFER
REMOVE SERIES RESISTOR FOR DEC21154
ADDDED AGP4X SIGNALS

2/7/00 (PMT)

CHANGE 402 RESISTORS BACK TO 603
CHANGE NON UNI-N CAPACITORS BACK TO 603
CHANGE PCI CLOCK CHIP TO CS002
FIX PCI CLOCK INPUTS TO UNI-N
ADD FIREWIRE PCI CLOCK
ADD DELAYED MEMORY CLOCK FOR SDRDCLK
REMOVE SCHOTTKY DIODE TERMINATION FROM SDRAM ADDRESS BUS
REMOVE IIC ROM
ADD PULLUP TO FASTBUS, MAKE ACTIVE HIGH
ADD SERIES RESISTORS TO AGP AD STROBES
REMOVE LEFT-OVER CIRCUITRY FROM PCI-PCI BRIDGE
ADD SERIES RESISTOR TO PCIGNT_5 BECAUSE OF STRONGER DRIVE
REMOVE MCLK_CKE, MCLK<12..15>

4/10-18/00 (RT)

ADD FILTERS FOR UNI-N PLLDVD AND AGPPLLDVD
ADD PROTOTYPING NETWORK FOR SD_EXT_R
ADD BULK BYPASS FOR UNI-N POWER RAILS (3.3V,MAXBUS,AGP_IO)
REMOVE LEVEL CONVERSION FOR CPU_INT<0..3>; KEYLARGO HAS OC OUTPUTS
REMOVE UNI-N TRST RESISTOR
CHANGED AGP CONNECTOR TO UNIVERSAL AGP CONNECTOR
FIX BOM OPTIONS FOR 133MHZ OPERATION
CHANGE R9, R361 TO 3.2K FOR EARLY POWER FAIL DETECTION
CONNECT REQ/GNTS TO UNUSED PINS ON NIGEL CONNECTOR
ADD PULLDOWNS FOR INVERTED AGP STROBE SIGNALS
CONNECT UNI-N SPARE3 (E2) TO PME VIA 0 OHM

4/28/00 (RT)
CHANGED U900; BCM5400 TO BCM5401
CHANGED U6: TSBLV23 TO TSBLV26

6/12/00 (RT)
CHANGED MAIN CLOCKING TO C5003; ADDED PULLUPS FOR DLX SIGNALS
CHANGED ESP CONNECTOR TO 515-1387
CHANGED 0.01UF CAPS TO 0402; BOM CONSOLIDATION
REMOVED UNI-N 0402 CAPS THAT COULDN'T BE PLACED
REMOVED SERIES R FOR KWEST_PCI_GRT#
CHANGED AGP PULLUP RAIL FROM 3.3V SLEEP TO AGP_IO_RAIL
ADDED GBIT PULLUPS/PULLDOWNS, ADDED SERIES R FOR GBIL RAILS
REMOVED INTERNAL FIREWIRE PORT, AND RELATED COMPONENTS
REMOVED PHY POWER CONVERTER, FEED IT FROM 3.3V TRICKLE INSTEAD
CHANGED FIREWIRE POWER SUPPLY TO A FET AND DIODE CONTROLLED BY 5V
CHANGED 1.8V POWER SUPPLY TO BE POWERED FROM 5V TRICKLE
ADDED 3.3V SLEEP TO GROUND CIRCUITRY TO ENSURE MEMORY RAIL IS GROUNDED DURING OFF
CHANGED POWER SUPPLY CONNECTOR TO 22 PIN CONNECTOR

6/30/00 (RT)
ADDED AUX POWER SUPPLY CONNECTOR; 4 PIN FOR VGER SUPPORT
REMOVED CPU_INT2 AND CPU_INT3, REUSING KEYLARGO PINS FOR FW_UNI_RST AND FW_LINK_PD
ADDED 1K PULLDOWN FOR AGP_PME* AND FW_TEST

7/14/00 (RT)
CONNECT/RENAME 33PCI_RESET* TO MAIN_RESET*; SLOT_B THRU SLOT_E, SCREAMER, BACKUP FIREWIRE
CHANGED 10KOHM FROM 0603 TO 0402 FOR CLOCK GENERATION EASE OF PLACEMENT

7/15/00 (RT)
CHANGED PULLUP OF AGP_INT* TO 3.3V INSTEAD OF AGP_IO_RAIL
ADDED NOTE ABOUT AGP2X/4X AND AGP_IO_RAIL OPERATION
CHANGED PULLUP OF AGP_TYPEDET* TO 3.3V; 1.5V IS A BIT LOW FOR VTH ON THE FETS

7/24/00 (RT)
REMOVED RP123; MOVED 33PCI_REQ64 TO ANOTHER RPACK

7/26/00 (RT)
CHANGED PINOUT AND SYMBOL FOR SLOT E PCI CONNECTOR; TO UNSWIZZLE PCI ROUTES ON ADD ON CARD
CHANGED SPARE2 PIN IN UNI-N FOR PCI SLOT RESET INPUT
ADDED CONSTRAINTS ON CLOCK LINES FOR EMI

IDSEL ASSIGNMENTS

33 MHZ (PRIMARY) BUS:

AD16 = RESERVED
AD18 = PCI SLOT B
AD19 = PCI SLOT C
AD20 = PCI SLOT D
AD21 = PCI SLOT E (NIGEL)
AD23 = KEYLARGO
AD24 = USB0
AD25 = USB1
AD26 = FIREWIRE (IF NOT IN UNI-N)
AD27 = ETHERNET (IF NOT IN UNI-N)

MLB STACKUP

LAYER	THICKNESS (mils)	TRACE WIDTH (mils)
signal	2.1	5.0
core	4.0	---
ground1	1.4	---
prepreg	8.0	---
signal	1.4	5.0
prepreg	10.0	---
power1	1.4	---
core	6.0	---
power2	1.4	---
prepreg	10.0	---
signal	1.4	5.0
prepreg	8.0	---
ground2	1.4	---
core	4.0	---
signal	2.1	5.0
TOTAL	62.6	---

Signal trace impedance of 55 ohms

CPU ROUTES ARE 60 OHMS?
AGP ROUTES ARE 50 OHMS
RAM ROUTES ARE 40 OHMS

TO DO

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-0997 | REV. 01
SCALE NONE | SHT 47 OF 47