REV	ZONE	ECN	DESCRIPTION OF REVISION	CK APPD / DATE	ENG APPD / DATE
A		51022	PRODUCTION RELEASE 1/97		

	Page	Contents
	1	Title page
Processor	2	603eV Processor
Memory	3	PSX bridge / memory controller
	4	DRAM, DRAM DIMM's
	5	ROM, ROM DIMM's
	6	PCI slot, Comm slot
	7	O'Hare I/O Controller
	8	Clocks
	9	Serial Ports
	10	SCSI, IDE Termination
	11	Cuda, ADB
	12	NVRAM, Cache slot, misc. term.
Audio	13	Audio Mixing
	14	AWACs sound chip
	15	SRS Surround Sound
Video	16	ATI 3D Graphic chip
	17	Video SGRAM & BIOS
	18	Video-In & MACH
Misc.	19	Address & Data buffers
	20	DRAM termination, decoupling, onboard regulator
	21	Pullups, Pulldowns
	22	MLB system connector
	23	Test Points
	24	More test points & vias
	25	Reference Designator Locations
	26	Change History

ArDat(0:63) - bit 0 MSB
ArAdr(0:31) - bit 0 MSB
RAB(11:0) - bit 11 MSB
CASB*(0:7) - bit 0 MSB

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DIMENSIONS ARE IN MILLIMETERS
X.X± ——
X.XX± ——
X.XXX± ——
ANGLES± ——
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THIRD ANGLE PROJECTION

METRIC

DRAFTER / DESIGN CK /
ENG APPD / MFG APPD /
QA APPD / DESIGNER /
RELEASE / SCALE NONE
MATERIAL/FINISH NOTED AS APPLICABLE | SIZE D

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TITLE
SCHEM, MLB, GAZELLE

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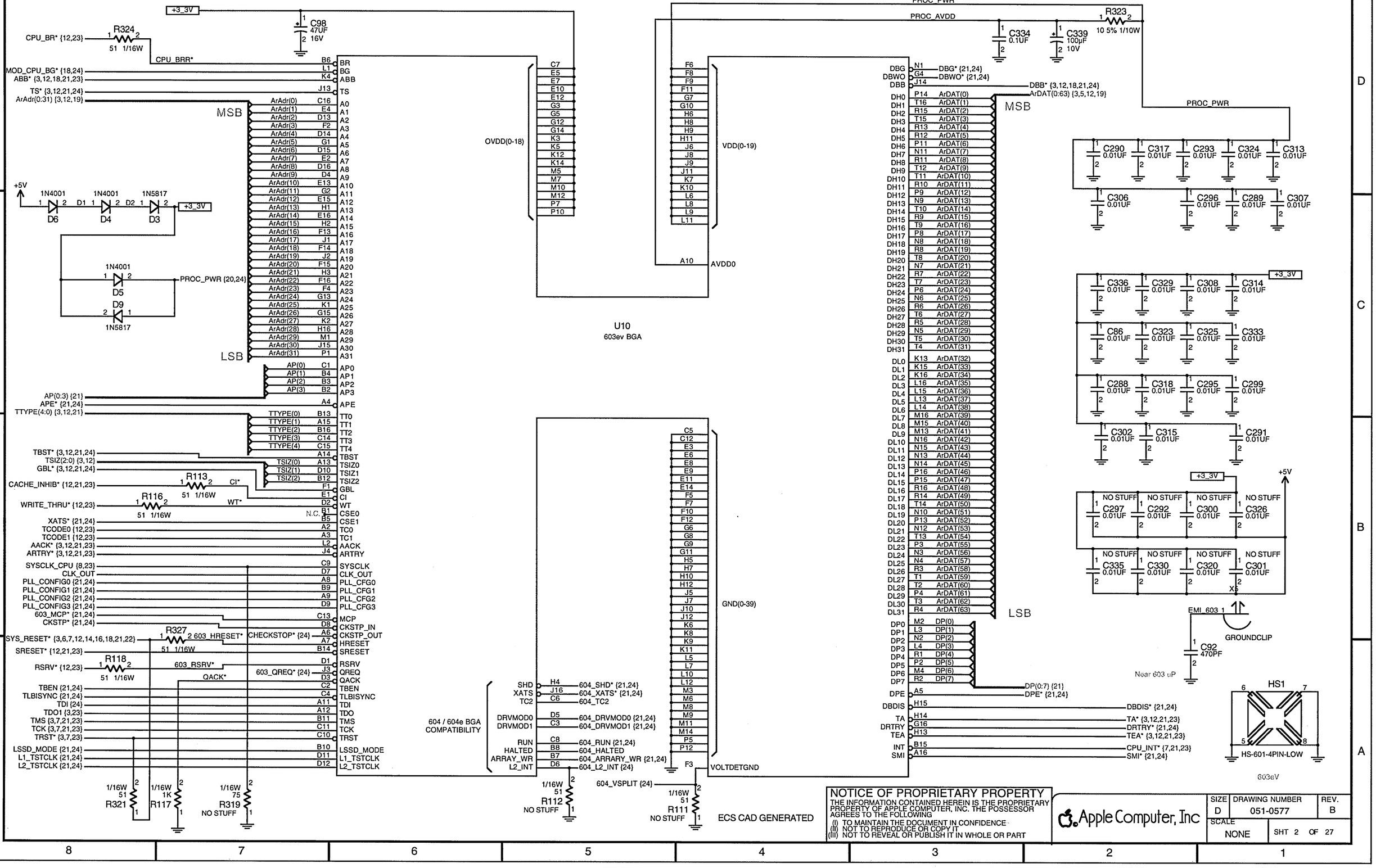
SHT 1 OF 27



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D	051-0577	B
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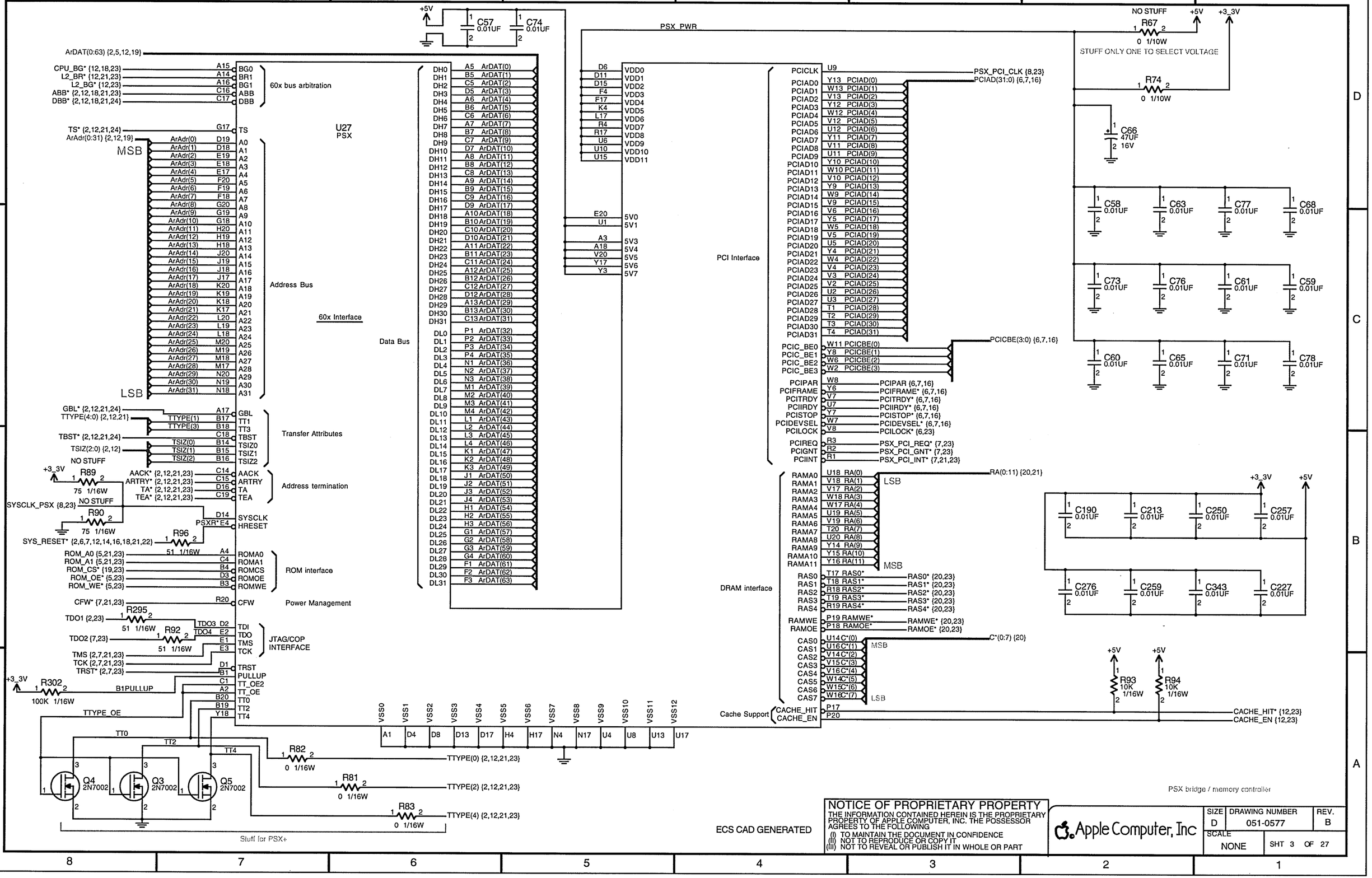
U27
PSX
60x bus arbitration
Address Bus
60x Interface
Data Bus
Transfer Attributes
Address termination
ROM interface
Power Management
JTAG/COP INTERFACE
PCI Interface
DRAM interface
Cache Support
Stuff for PSX+
NO STUFF
STUFF ONLY ONE TO SELECT VOLTAGE
PSX_PWR
+5V
+3_3V
MSB
LSB
ECS CAD GENERATED
PSX bridge / memory controller
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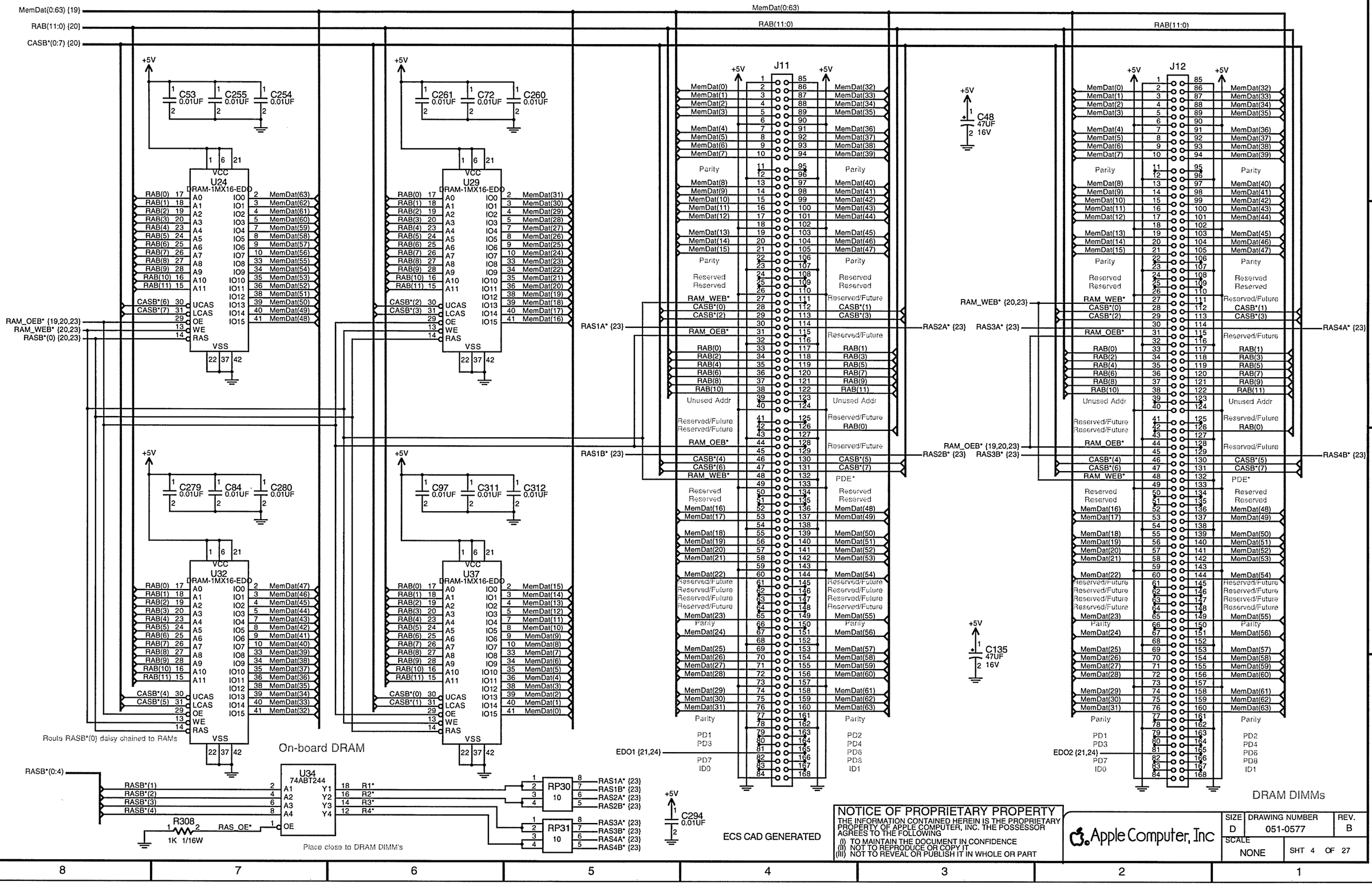

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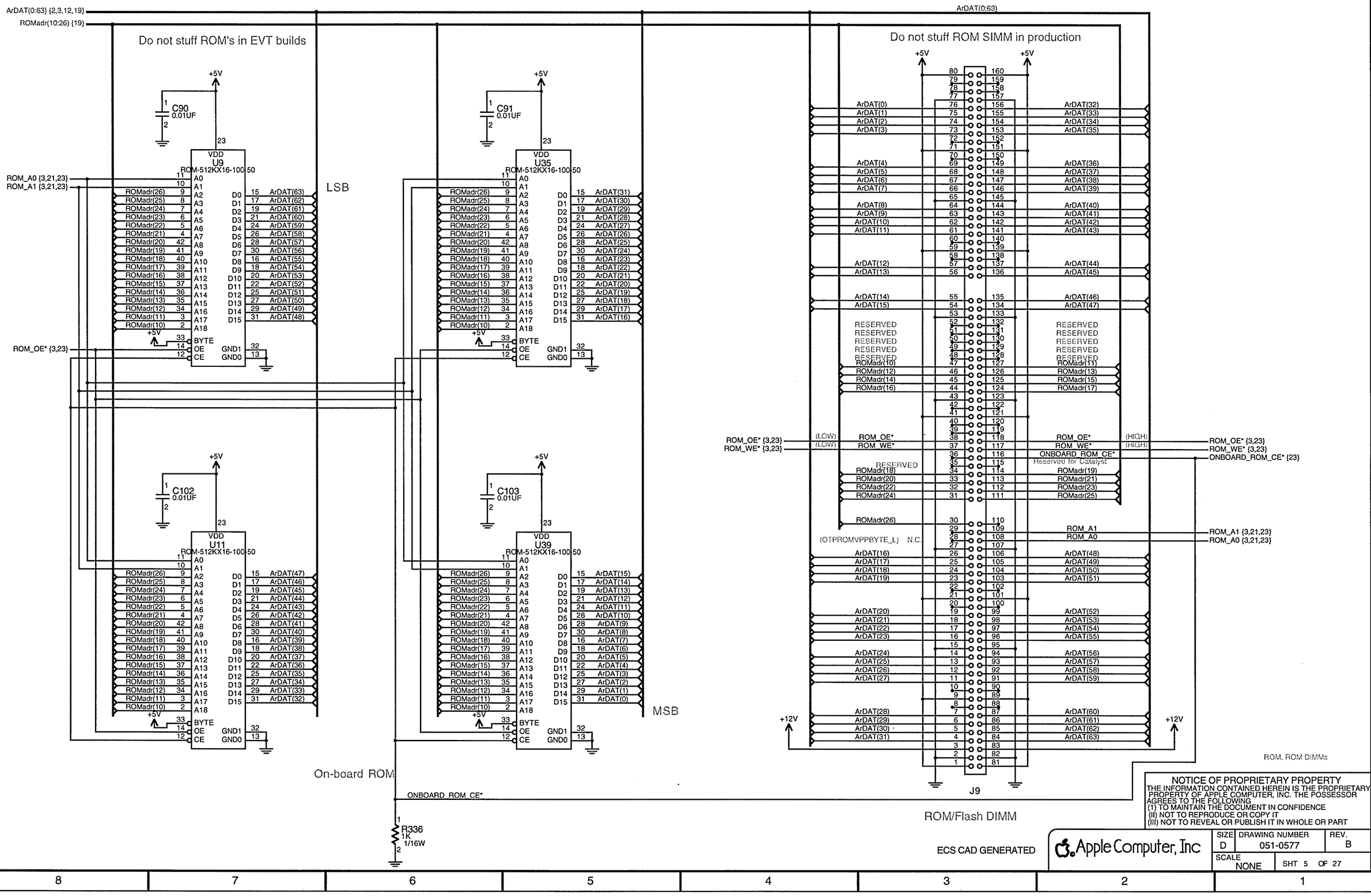

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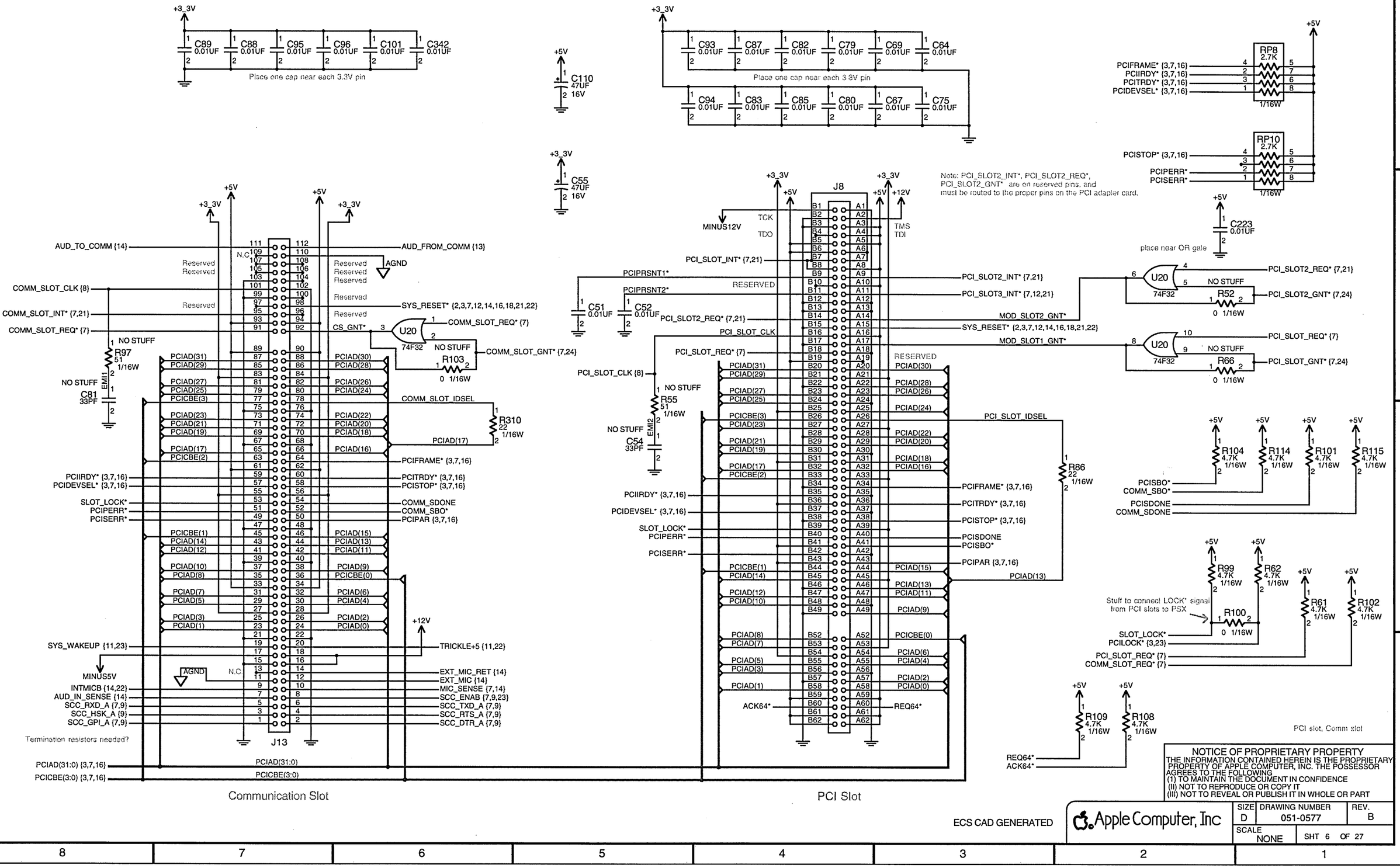
+3_3V
C89 0.01UF
C88 0.01UF
C95 0.01UF
C96 0.01UF
C101 0.01UF
C342 0.01UF
Place one cap near each 3.3V pin
C110 47UF 16V
C55 47UF 16V
C93 0.01UF
C87 0.01UF
C82 0.01UF
C79 0.01UF
C69 0.01UF
C64 0.01UF
C94 0.01UF
C83 0.01UF
C85 0.01UF
C80 0.01UF
C67 0.01UF
C75 0.01UF
Place one cap near each 3.3V pin
RP8 2.7K
PCIFRAME* {3,7,16}
PCIIRDY* {3,7,16}
PCITRDY* {3,7,16}
PCIDEVSEL* {3,7,16}
1/16W
RP10 2.7K
PCISTOP* {3,7,16}
PCIPERR*
PCISERR*
1/16W
Note: PCI_SLOT2_INT*, PCI_SLOT2_REQ*, PCI_SLOT2_GNT* are on reserved pins, and must be routed to the proper pins on the PCI adapter card.
C223 0.01UF
place near OR gate
AUD_TO_COMM {14}
AUD_FROM_COMM {13}
AGND
COMM_SLOT_CLK {8}
SYS_RESET* {2,3,7,12,14,16,18,21,22}
COMM_SLOT_INT* {7,21}
COMM_SLOT_REQ* {7}
CS_GNT*
U20 74F32
NO STUFF
COMM_SLOT_GNT* {7,24}
R97 51 1/16W
R103 0 1/16W
C81 33PF
EMI1
COMM_SLOT_IDSEL
R310 22 1/16W
PCIAD(17)
PCIFRAME* {3,7,16}
PCIIRDY* {3,7,16}
PCIDEVSEL* {3,7,16}
PCITRDY* {3,7,16}
PCISTOP* {3,7,16}
SLOT_LOCK*
PCIPERR*
PCISERR*
COMM_SDONE
COMM_SBO*
PCIPAR {3,7,16}
+12V
SYS_WAKEUP {11,23}
TRICKLE+5 {11,22}
MINUS5V
INTMICB {14,22}
AUD_IN_SENSE {14}
SCC_RXD_A {7,9}
SCC_HSK_A {9}
SCC_GPI_A {7,9}
EXT_MIC_RET {14}
EXT_MIC {14}
MIC_SENSE {7,14}
SCC_ENAB {7,9,23}
SCC_TXD_A {7,9}
SCC_RTS_A {7,9}
SCC_DTR_A {7,9}
Termination resistors needed?
J13
PCIAD(31:0) {3,7,16}
PCICBE(3:0) {3,7,16}
PCIAD(31:0)
PCICBE(3:0)
Communication Slot
J8
MINUS12V
TCK
TDO
TMS
TDI
PCI_SLOT_INT* {7,21}
PCIPRSNT1*
PCIPRSNT2*
RESERVED
C51 0.01UF
C52 0.01UF
PCI_SLOT2_REQ* {7,21}
PCI_SLOT_CLK
PCI_SLOT_REQ* {7}
PCI_SLOT_CLK {8}
R55 51 1/16W
C54 33PF
EMI2
PCI_SLOT2_INT* {7,21}
PCI_SLOT3_INT* {7,12,21}
MOD_SLOT2_GNT*
SYS_RESET* {2,3,7,12,14,16,18,21,22}
MOD_SLOT1_GNT*
PCI_SLOT_IDSEL
R86 22 1/16W
PCIFRAME* {3,7,16}
PCITRDY* {3,7,16}
PCISTOP* {3,7,16}
PCISDONE
PCISBO*
PCIPAR {3,7,16}
PCIAD(13)
ACK64*
REQ64*
PCI Slot
U20 74F32
NO STUFF
PCI_SLOT2_REQ* {7,21}
PCI_SLOT2_GNT* {7,24}
R52 0 1/16W
PCI_SLOT_REQ* {7}
PCI_SLOT_GNT* {7,24}
R66 0 1/16W
R104 4.7K 1/16W
R114 4.7K 1/16W
R101 4.7K 1/16W
R115 4.7K 1/16W
PCISBO*
COMM_SBO*
PCISDONE
COMM_SDONE
R99 4.7K 1/16W
R62 4.7K 1/16W
R61 4.7K 1/16W
R102 4.7K 1/16W
Stuff to connect LOCK* signal from PCI slots to PSX
R100 0 1/16W
SLOT_LOCK*
PCILOCK* {3,23}
PCI_SLOT_REQ* {7}
COMM_SLOT_REQ* {7}
R109 4.7K 1/16W
R108 4.7K 1/16W
REQ64*
ACK64*
PCI slot, Comm slot
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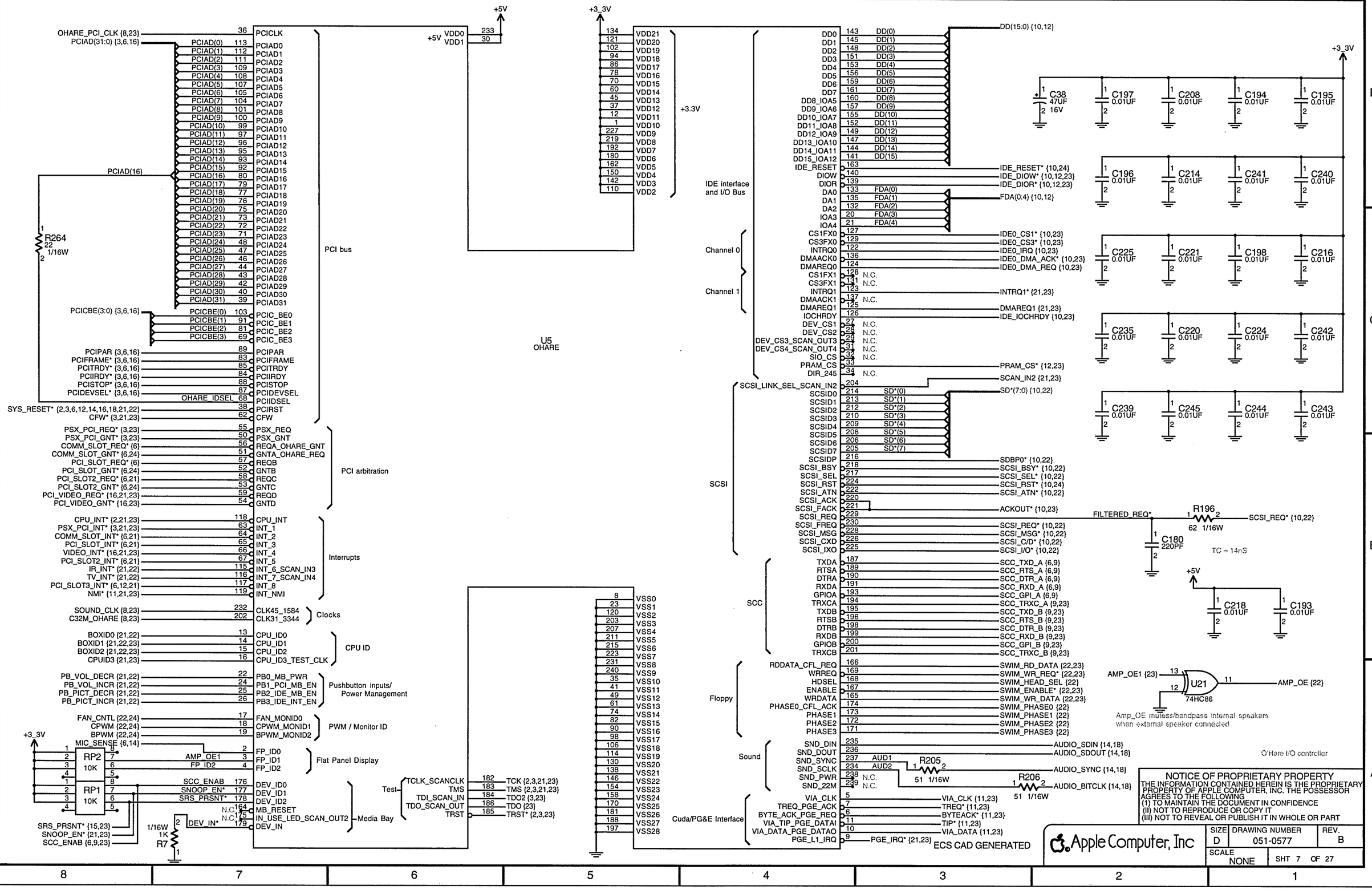
OHARE_PCI_CLK {8,23}
PCIAD{31:0} {3,6,16}
PCIAD(16)
R264 22 1/16W
PCICBE(3:0) {3,6,16}
PCIPAR {3,6,16}
PCIFRAME* {3,6,16}
PCITRDY* {3,6,16}
PCIIRDY* {3,6,16}
PCISTOP* {3,6,16}
PCIDEVSEL* {3,6,16}
OHARE_IDSEL 68
SYS_RESET* {2,3,6,12,14,16,18,21,22}
CFW* {3,21,23}
PCI bus
PSX_PCI_REQ* {3,23}
PSX_PCI_GNT* {3,23}
COMM_SLOT_REQ* {6}
COMM_SLOT_GNT* {6,24}
PCI_SLOT_REQ* {6}
PCI_SLOT_GNT* {6,24}
PCI_SLOT2_REQ* {6,21}
PCI_SLOT2_GNT* {6,24}
PCI_VIDEO_REQ* {16,21,23}
PCI_VIDEO_GNT* {16,23}
PCI arbitration
CPU_INT* {2,21,23}
PSX_PCI_INT* {3,21,23}
COMM_SLOT_INT* {6,21}
PCI_SLOT_INT* {6,21}
VIDEO_INT* {16,21,23}
PCI_SLOT2_INT* {6,21}
IR_INT* {21,22}
TV_INT* {21,22}
PCI_SLOT3_INT* {6,12,21}
NMI* {11,21,23}
Interrupts
SOUND_CLK {8,23}
C32M_OHARE {8,23}
Clocks
BOXID0 {21,22}
BOXID1 {21,22,23}
BOXID2 {21,22,23}
CPUID3 {21,23}
CPU ID
PB_VOL_DECR {21,22}
PB_VOL_INCR {21,22}
PB_PICT_DECR {21,22}
PB_PICT_INCR {21,22}
Pushbutton inputs/ Power Management
FAN_CNTL {22,24}
CPWM {22,24}
BPWM {22,24}
PWM / Monitor ID
MIC_SENSE {6,14}
AMP_OE1
FP_ID2
RP2 10K
RP1 10K
SCC_ENAB
SNOOP_EN*
SRS_PRSNT*
SRS_PRSNT* {15,23}
SNOOP_EN* {21,23}
SCC_ENAB {6,9,23}
1/16W 1K R7
DEV_IN*
Flat Panel Display
Media Bay
+5V
+3_3V
VDD0
VDD1
+3.3V
U5 OHARE
IDE interface and I/O Bus
Channel 0
Channel 1
DD(15:0) {10,12}
IDE_RESET* {10,24}
IDE_DIOW* {10,12,23}
IDE_DIOR* {10,12,23}
FDA(0:4) {10,12}
IDE0_CS1* {10,23}
IDE0_CS3* {10,23}
IDE0_IRQ {10,23}
IDE0_DMA_ACK* {10,23}
IDE0_DMA_REQ {10,23}
INTRQ1* {21,23}
DMAREQ1 {21,23}
IDE_IOCHRDY {10,23}
PRAM_CS* {12,23}
SCAN_IN2 {21,23}
SCSI_LINK_SEL_SCAN_IN2
SD*(7:0) {10,22}
SDBP0* {10,22}
SCSI
SCSI_BSY* {10,22}
SCSI_SEL* {10,22}
SCSI_RST* {10,24}
SCSI_ATN* {10,22}
ACKOUT* {10,23}
SCSI_REQ* {10,22}
SCSI_MSG* {10,22}
SCSI_C/D* {10,22}
SCSI_I/O* {10,22}
FILTERED_REQ*
R196 62 1/16W
C180 220PF
TC = 14nS
SCSI_REQ* {10,22}
SCC
SCC_TXD_A {6,9}
SCC_RTS_A {6,9}
SCC_DTR_A {6,9}
SCC_RXD_A {6,9}
SCC_GPI_A {6,9}
SCC_TRXC_A {9,23}
SCC_TXD_B {9,23}
SCC_RTS_B {9,23}
SCC_DTR_B {9,23}
SCC_RXD_B {9,23}
SCC_GPI_B {9,23}
SCC_TRXC_B {9,23}
Floppy
SWIM_RD_DATA {22,23}
SWIM_WR_REQ* {22,23}
SWIM_HEAD_SEL {22}
SWIM_ENABLE* {22,23}
SWIM_WR_DATA {22,23}
SWIM_PHASE0 {22}
SWIM_PHASE1 {22}
SWIM_PHASE2 {22}
SWIM_PHASE3 {22}
Sound
AUDIO_SDIN {14,18}
AUDIO_SDOUT {14,18}
AUDIO_SYNC {14,18}
AUDIO_BITCLK {14,18}
R205 51 1/16W
R206 51 1/16W
Cuda/PG&E Interface
VIA_CLK {11,23}
TREQ* {11,23}
BYTEACK* {11,23}
TIP* {11,23}
VIA_DATA {11,23}
PGE_IRQ* {21,23}
ECS CAD GENERATED
C38 47UF 16V
C197 0.01UF
C208 0.01UF
C194 0.01UF
C195 0.01UF
C196 0.01UF
C214 0.01UF
C241 0.01UF
C240 0.01UF
C225 0.01UF
C221 0.01UF
C198 0.01UF
C216 0.01UF
C235 0.01UF
C220 0.01UF
C224 0.01UF
C242 0.01UF
C239 0.01UF
C245 0.01UF
C244 0.01UF
C243 0.01UF
C218 0.01UF
C193 0.01UF
AMP_OE1 {23}
U21 74HC86
AMP_OE {22}
Amp_OE mutes s/bandpass internal speakers when external speaker connected
O'Hare I/O controller
Test
TCK {2,3,21,23}
TMS {2,3,21,23}
TDO2 {3,23}
TDO {23}
TRST* {2,3,23}
VSS0 VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28
VDD21 VDD20 VDD19 VDD18 VDD17 VDD16 VDD15 VDD14 VDD13 VDD12 VDD11 VDD10 VDD9 VDD8 VDD7 VDD6 VDD5 VDD4 VDD3 VDD2
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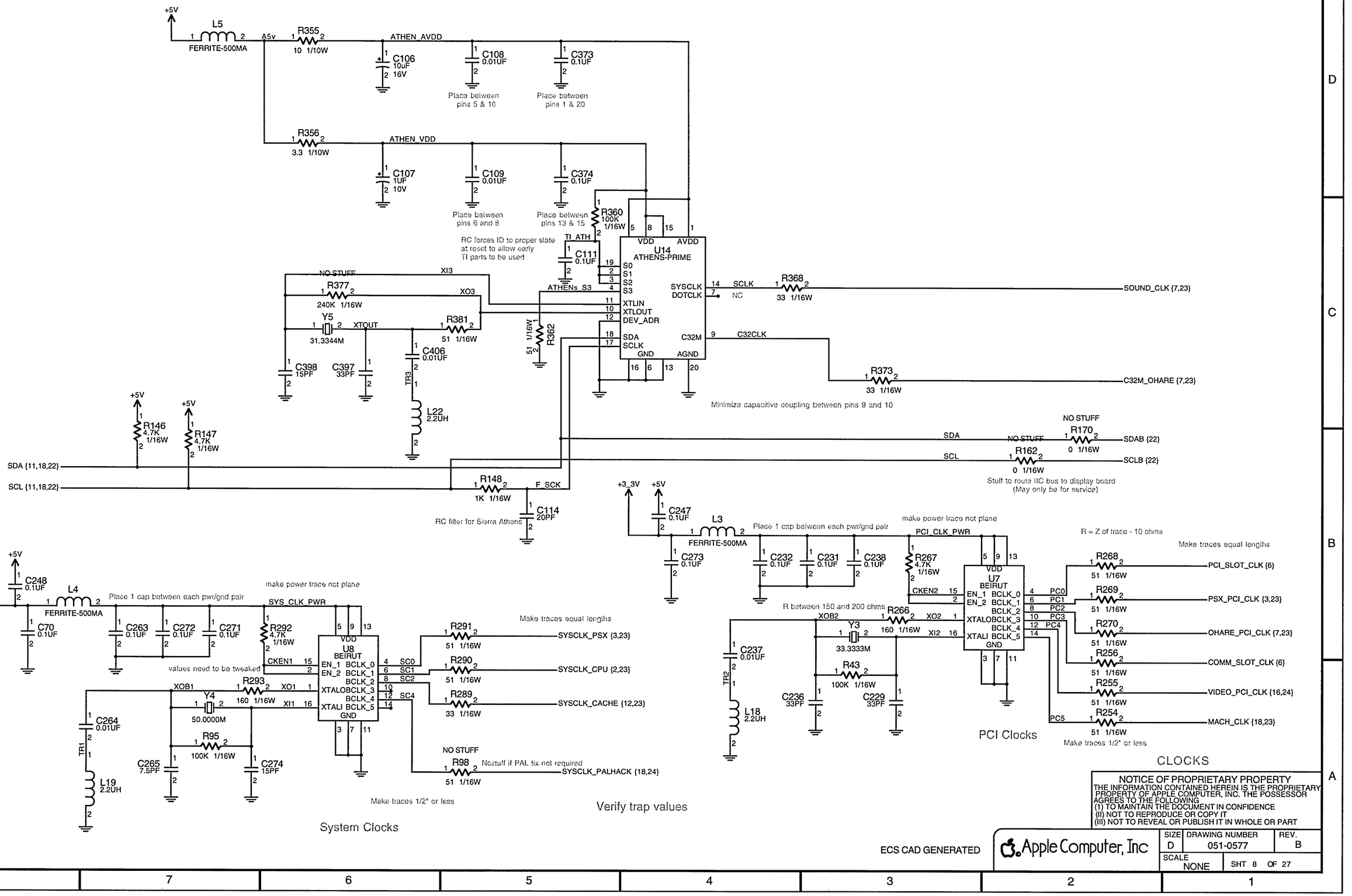
+5V
L5
FERRITE-500MA
A5v
R355
10 1/10W
ATHEN_AVDD
C106
10uF
16V
C108
0.01UF
Place between pins 5 & 16
C373
0.1UF
Place between pins 1 & 20
R356
3.3 1/10W
ATHEN_VDD
C107
1UF
10V
C109
0.01UF
Place between pins 6 and 8
C374
0.1UF
Place between pins 13 & 15
R360
100K
1/16W
RC forces ID to proper state at reset to allow early TI parts to be used
TI_ATH
C111
0.1UF
U14
ATHENS-PRIME
VDD
AVDD
S0
S1
S2
S3
ATHENs_S3
XTLIN
XTLOUT
DEV_ADR
SDA
SCLK
GND
AGND
SYSCLK
DOTCLK
SCLK
NC
R368
33 1/16W
SOUND_CLK {7,23}
C32M
C32CLK
R373
33 1/16W
C32M_OHARE {7,23}
Minimize capacitive coupling between pins 9 and 10
NO STUFF
XI3
XO3
R377
240K 1/16W
Y5
31.3344M
XTOUT
R381
51 1/16W
R362
51 1/16W
C398
15PF
C397
33PF
C406
0.01UF
TR3
L22
2.2UH
R146
4.7K
1/16W
R147
4.7K
1/16W
SDA {11,18,22}
SCL {11,18,22}
R148
1K 1/16W
F_SCK
C114
20PF
RC filter for Sierra Athens
NO STUFF
R170
0 1/16W
SDA
SDAB {22}
R162
0 1/16W
SCL
SCLB {22}
Stuff to route IIC bus to display board (May only be for service)
+3_3V
C247
0.1UF
L3
FERRITE-500MA
C273
0.1UF
Place 1 cap between each pwr/gnd pair
C232
0.1UF
C231
0.1UF
C238
0.1UF
make power trace not plane
PCI_CLK_PWR
R267
4.7K
1/16W
CKEN2
U7
BEIRUT
EN_1 BCLK_0
EN_2 BCLK_1
BCLK_2
BCLK_3
BCLK_4
BCLK_5
XTALOBCLK
XTALI
GND
PC0
PC1
PC2
PC3
PC4
PC5
B = Z of trace - 10 ohms
Make traces equal lengths
R268
51 1/16W
PCI_SLOT_CLK {6}
R269
51 1/16W
PSX_PCI_CLK {3,23}
R270
51 1/16W
OHARE_PCI_CLK {7,23}
R256
51 1/16W
COMM_SLOT_CLK {6}
R255
51 1/16W
VIDEO_PCI_CLK {16,24}
R254
51 1/16W
MACH_CLK {18,23}
Make traces 1/2" or less
R between 150 and 200 ohms
R266
160 1/16W
XO2
XI2
Y3
33.3333M
C237
0.01UF
TR2
L18
2.2UH
R43
100K 1/16W
C236
33PF
C229
33PF
PCI Clocks
+3_3V
C248
0.1UF
L4
FERRITE-500MA
C70
0.1UF
Place 1 cap between each pwr/gnd pair
C263
0.1UF
C272
0.1UF
C271
0.1UF
make power trace not plane
SYS_CLK_PWR
R292
4.7K
1/16W
CKEN1
values need to be tweaked
U8
BEIRUT
EN_1 BCLK_0
EN_2 BCLK_1
BCLK_2
BCLK_3
BCLK_4
BCLK_5
XTALOBCLK
XTALI
GND
SC0
SC1
SC2
SC4
Make traces equal lengths
R291
51 1/16W
SYSCLK_PSX {3,23}
R290
51 1/16W
SYSCLK_CPU {2,23}
R289
33 1/16W
SYSCLK_CACHE {12,23}
XOB1
XO1
XI1
R293
160 1/16W
Y4
50.0000M
C264
0.01UF
TR1
L19
2.2UH
R95
100K 1/16W
C265
7.5PF
C274
15PF
NO STUFF
R98
51 1/16W
Nostuff if PAL fix not required
SYSCLK_PALHACK {18,24}
Make traces 1/2" or less
System Clocks
Verify trap values
CLOCKS
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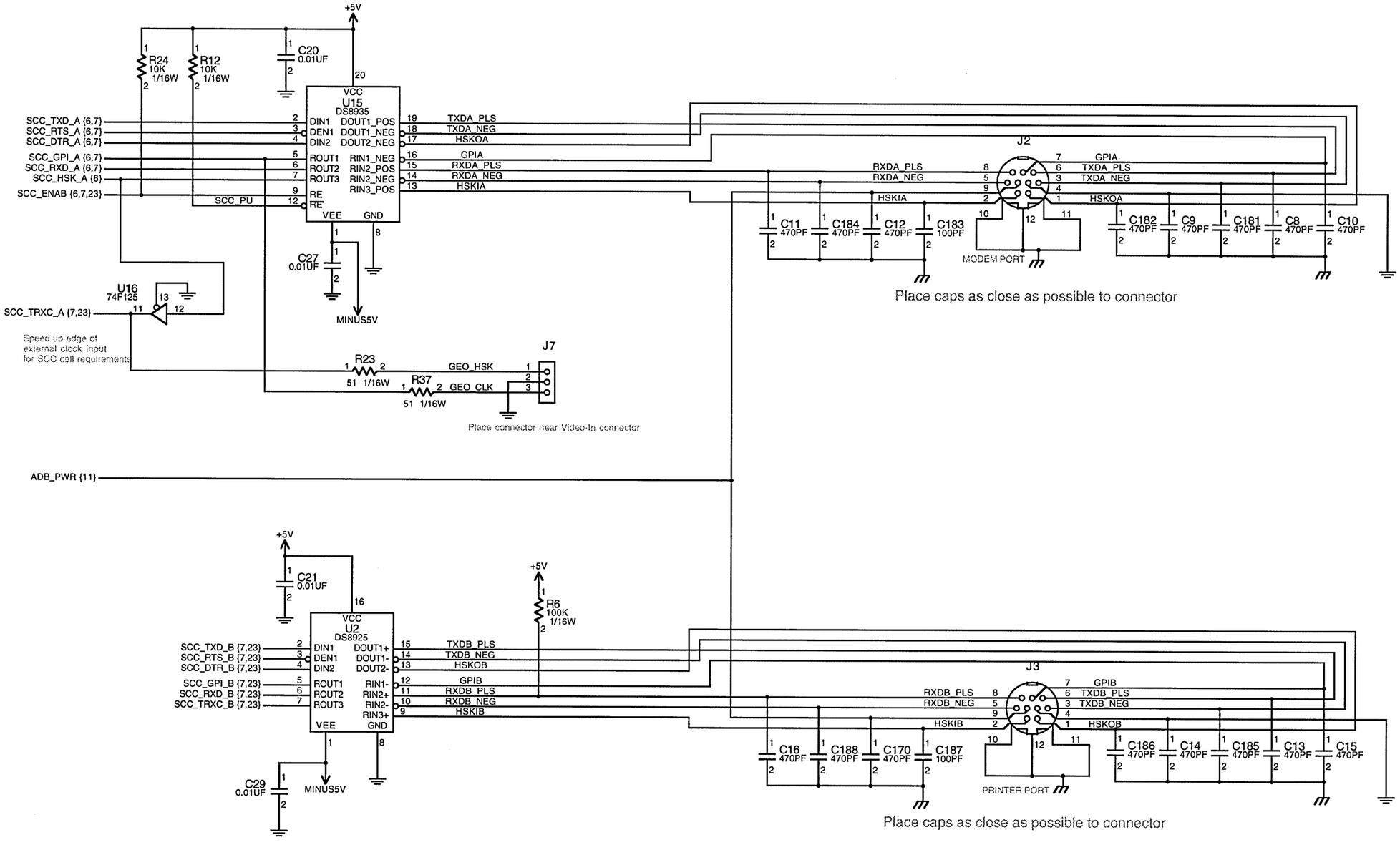

Serial Ports

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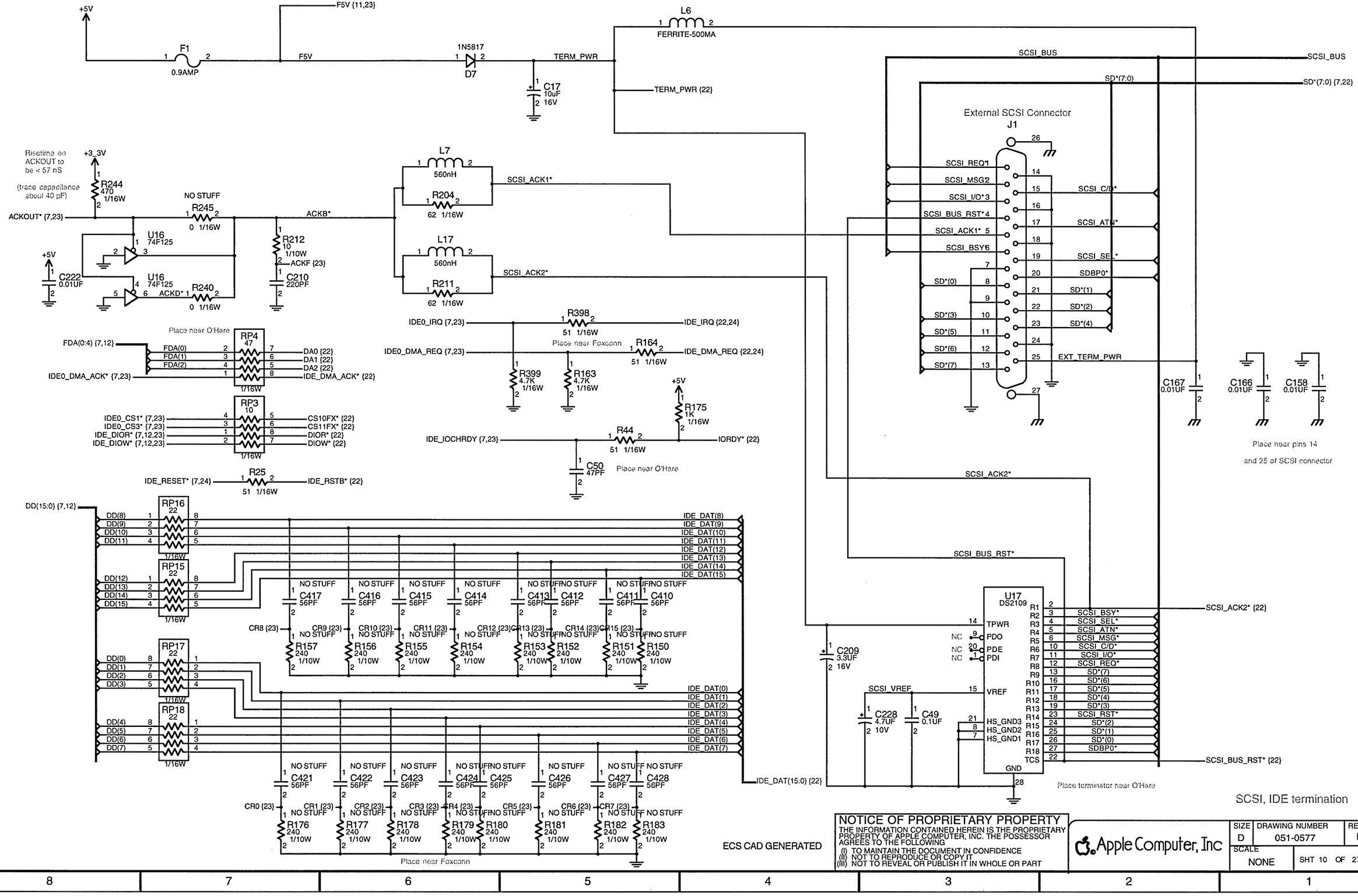
+5V
F5V {11,23}
F1
0.9AMP
F5V
1N5817
D7
TERM_PWR
L6
FERRITE-500MA
C17
10uF
16V
TERM_PWR {22}
SCSI_BUS
SCSI_BUS
SD*(7:0)
SD*(7:0) {7,22}
External SCSI Connector
J1
SCSI_REQ*1
SCSI_MSG*2
SCSI_I/O*3
SCSI_BUS_RST*4
SCSI_ACK1* 5
SCSI_BSY*6
SD*(0) 8
SD*(3) 10
SD*(5) 11
SD*(6) 12
SD*(7) 13
SCSI_C/D*
SCSI_ATN*
SCSI_SEL*
SDBP0*
SD*(1)
SD*(2)
SD*(4)
EXT_TERM_PWR
C167 0.01UF
C166 0.01UF
C158 0.01UF
Place near pins 14
and 25 of SCSI connector
Risetime on ACKOUT to be < 57 nS
(trace capacitance about 40 pF)
+3_3V
R244 470 1/16W
NO STUFF
R245 0 1/16W
ACKOUT* {7,23}
ACKB*
U16 74F125
C222 0.01UF
R240 0 1/16W
ACKD*
R212 10 1/10W
ACKF {23}
C210 220PF
L7 560nH
R204 62 1/16W
SCSI_ACK1*
L17 560nH
R211 62 1/16W
SCSI_ACK2*
SCSI_ACK2*
SCSI_BUS_RST*
IDE0_IRQ {7,23}
R398 51 1/16W
IDE_IRQ {22,24}
IDE0_DMA_REQ {7,23}
Place near Foxconn
R164 51 1/16W
IDE_DMA_REQ {22,24}
R399 4.7K 1/16W
R163 4.7K 1/16W
+5V
R175 1K 1/16W
IDE_IOCHRDY {7,23}
R44 51 1/16W
IORDY* {22}
C50 47PF
Place near O'Hare
Place near O'Hare
FDA(0:4) {7,12}
RP4 47 1/16W
FDA(0)
FDA(1)
FDA(2)
DA0 {22}
DA1 {22}
DA2 {22}
IDE0_DMA_ACK* {7,23}
IDE_DMA_ACK* {22}
RP3 10 1/16W
IDE0_CS1* {7,23}
IDE0_CS3* {7,23}
IDE_DIOR* {7,12,23}
IDE_DIOW* {7,12,23}
CS10FX* {22}
CS11FX* {22}
DIOR* {22}
DIOW* {22}
R25 51 1/16W
IDE_RESET* {7,24}
IDE_RSTB* {22}
DD(15:0) {7,12}
RP16 22 1/16W
RP15 22 1/16W
RP17 22 1/16W
RP18 22 1/16W
DD(8)
DD(9)
DD(10)
DD(11)
DD(12)
DD(13)
DD(14)
DD(15)
DD(0)
DD(1)
DD(2)
DD(3)
DD(4)
DD(5)
DD(6)
DD(7)
IDE_DAT(8)
IDE_DAT(9)
IDE_DAT(10)
IDE_DAT(11)
IDE_DAT(12)
IDE_DAT(13)
IDE_DAT(14)
IDE_DAT(15)
IDE_DAT(0)
IDE_DAT(1)
IDE_DAT(2)
IDE_DAT(3)
IDE_DAT(4)
IDE_DAT(5)
IDE_DAT(6)
IDE_DAT(7)
NO STUFF
C417 56PF
C416 56PF
C415 56PF
C414 56PF
C413 56PF
C412 56PF
C411 56PF
C410 56PF
CR8 {23}
CR9 {23}
CR10 {23}
CR11 {23}
CR12 {23}
CR13 {23}
CR14 {23}
CR15 {23}
R157 240 1/10W
R156 240 1/10W
R155 240 1/10W
R154 240 1/10W
R153 240 1/10W
R152 240 1/10W
R151 240 1/10W
R150 240 1/10W
C421 56PF
C422 56PF
C423 56PF
C424 56PF
C425 56PF
C426 56PF
C427 56PF
C428 56PF
CR0 {23}
CR1 {23}
CR2 {23}
CR3 {23}
CR4 {23}
CR5 {23}
CR6 {23}
CR7 {23}
R176 240 1/10W
R177 240 1/10W
R178 240 1/10W
R179 240 1/10W
R180 240 1/10W
R181 240 1/10W
R182 240 1/10W
R183 240 1/10W
Place near Foxconn
IDE_DAT(15:0) {22}
U17 DS2109
TPWR
PDO
PDE
PDI
VREF
HS_GND3
HS_GND2
HS_GND1
GND
TCS
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
SCSI_BSY*
SCSI_SEL*
SCSI_ATN*
SCSI_MSG*
SCSI_C/D*
SCSI_I/O*
SCSI_REQ*
SD*(7)
SD*(6)
SD*(5)
SD*(4)
SD*(3)
SCSI_RST*
SD*(2)
SD*(1)
SD*(0)
SDBP0*
SCSI_ACK2* {22}
SCSI_BUS_RST* {22}
C209 3.3UF 16V
SCSI_VREF
C228 4.7UF 10V
C49 0.1UF
Place terminator near O'Hare
SCSI, IDE termination
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SIZE D
DRAWING NUMBER 051-0577
REV. B
SCALE NONE
SHT 10 OF 27

This circuit disconnects the PFW pullup when 5V_DETECT not present

NOSTUFF all components in this box for Cuda revisions other than 2.40.

R41 15K 1/16W
R40 15K 1/16W
Q1 2N3906
R32 0 1/16W NO STUFF
Stuff this resistor for Cuda revisions other than 2.40
R38 100K 1/16W
Q2 2N3904

TRICKLE+5 {6,22}
CUDA_VDD {12,23}
KEYBOARD_PWR_ON* {22}
F5V {10,23}
ADB_DAT
ADB_DAT_F {22}
ADB_PWR {9}
TRICKLE_SENSE
+5V_SENSE {22}
SYS_WAKEUP {6,23}
PFW {22}
NMI* {7,21,23}
CHASSIS_SW {22}
FRESET* {24}
SYS_RST* {22,23}

C39 100UF 6.3V
C230 0.1UF
D8 1N914
Y2 32.768K
Y1 32.768K
Stuff only one crystal
C40 33PF
C45 10PF
R31 5.1M 1/10W
R222 330K 1/16W
CUDA_OSCIN
CUDA_OSCOUT

U19 LS1176
VRTC VCC
VTRICKLE VBATT
TRICKE_D5VDECT
GND VREF
BAT

C233 0.01UF
C217 0.01UF
R257 470K 1/16W
S1
C44 3.3UF

U18 CUDA
VDD1 VDDSYN
OSCI
OSCO
PA0 PFW
PA1 CHASSIS_SW
PA2 KEYBOARD_PWR_ON*
PA3 FRESET*
PA4 SYS_WAKEUP
PA5 OFF_SENSE
PA6 ADB_IN
PA7 ADB_OUT
PC0 FILE_SERVER
PC1
PC2 NMI*
PC3 SYS_RST*
GND1
PB0 LED_CNTL {22}
PB1 TREQ* {7,23}
PB2 BYTEACK* {7,23}
PB3 TIP* {7,23}
PB4 VIA_CLK {7,23}
PB5 VIA_DATA {7,23}
PB6 SDA {8,18,22}
PB7 SCL {8,18,22}
RESET CUDA_RESET*
IRQ CUDA_IRQ_TST
XFC
R221 1K 1/16W
C234 0.1UF

R251 4.7K 1/16W
R252 100K 1/16W
R253 100K 1/16W
R261 100K 1/16W
R262 100K 1/16W

R26 470 1/16W
R227 22 1/16W
R241 10K 1/16W
Q9 2N3904
MT

W1
NO STUFF
L8 FERRITE-500MA
L10 FERRITE-500MA
L12 FERRITE-500MA
L14 FERRITE-500MA
LP2 FERR-1A
L15 100-OHM-EMI
L13 100-OHM-EMI
L11 100-OHM-EMI
L9 100-OHM-EMI
R223 0 1/16W NO STUFF
Change part number to 517-1259
J4
ADB_GND 4
ADB_PWR_ON* 2
3 ADB_PWR
1 ADB_DATA
5 7 6

C173 0.01UF
C172 0.01UF
C171 470PF
C178 0.01UF
NO STUFF
To provide 0805 pads, silkscreens are not shown

R248 0 1/10W
Change to 1K if Lithium battery used
J15
BATTERY
NC

R258 100K 1/16W
R263 1K 1/16W

PART NUMBER	QTY	DESCRIPTION	ASSOCIATED REFERENCE DESIGNATORS
742-0025	1	Alkaline battery	EXT BT1

Cuda, ADB

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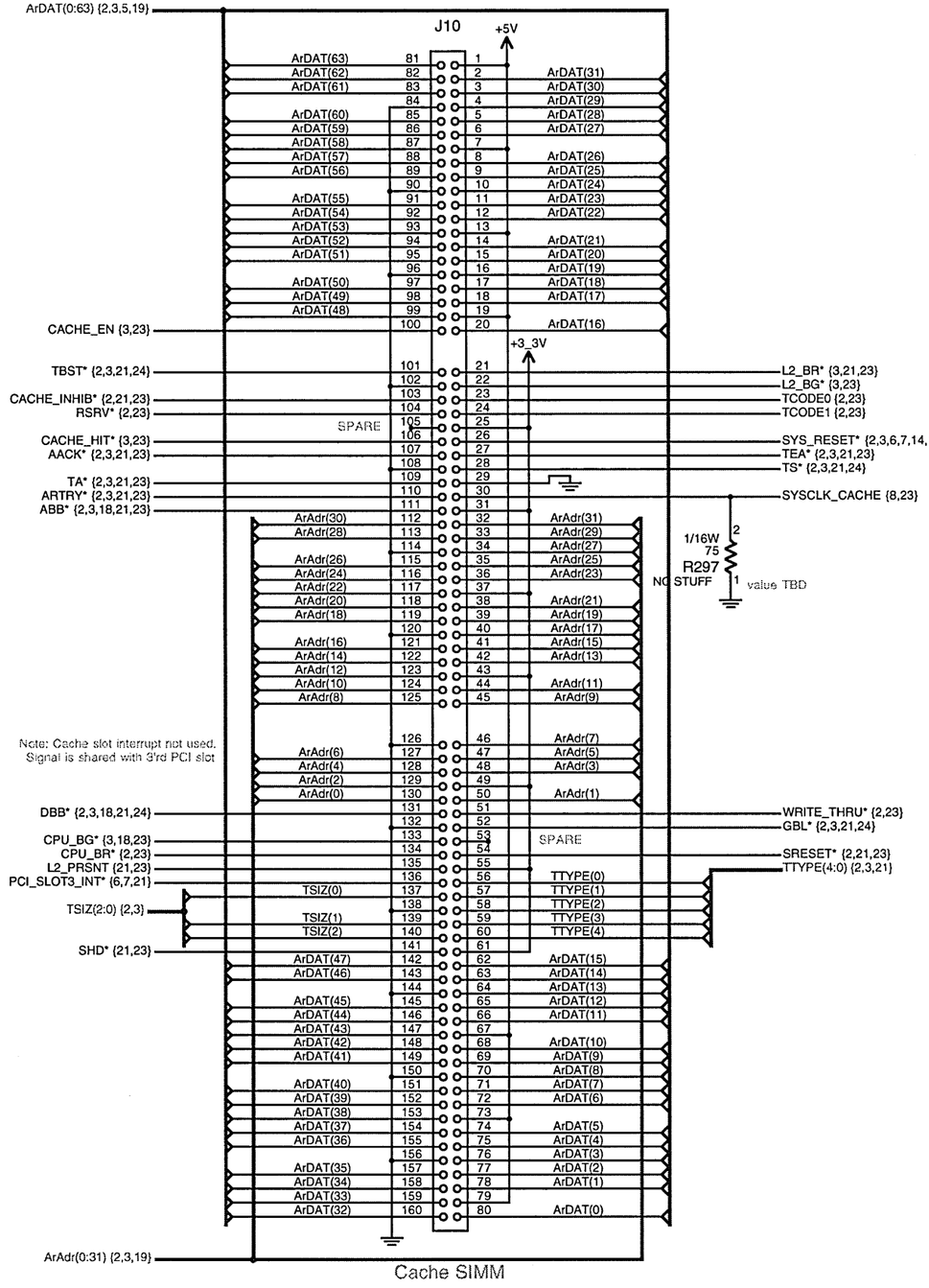
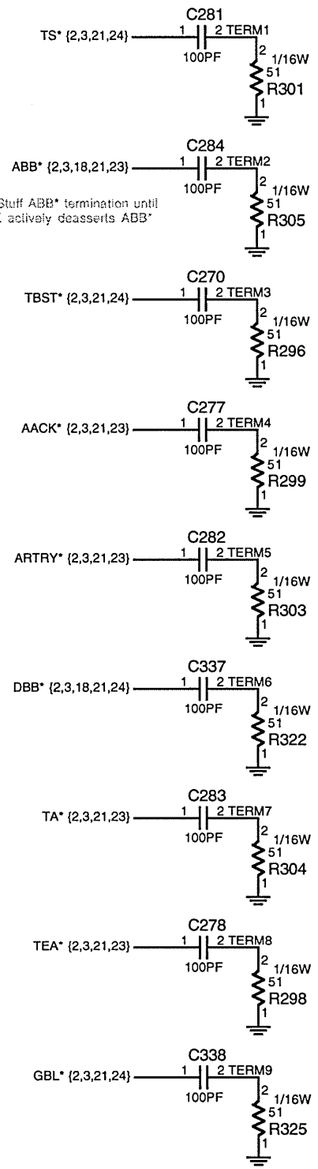
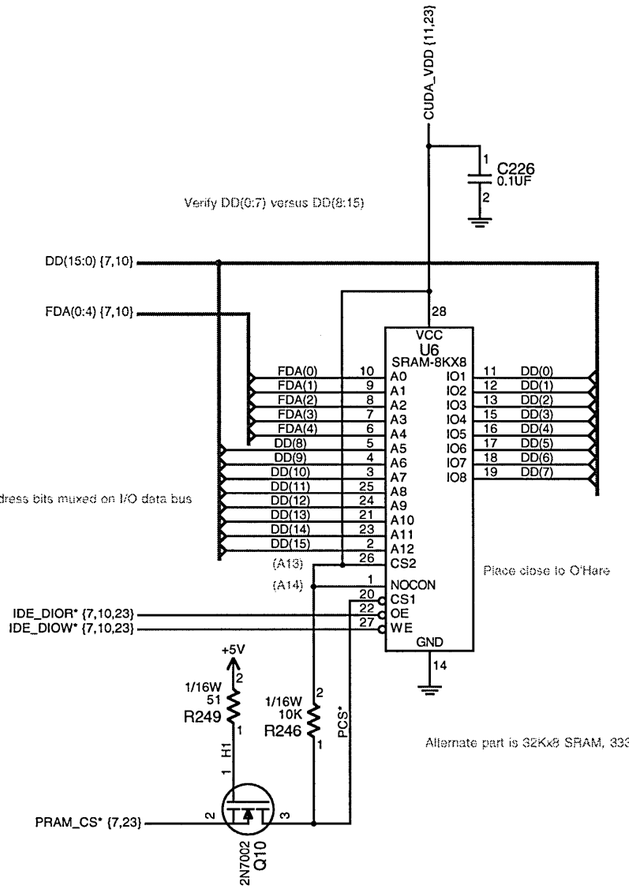
D	051-0577	B
SCALE NONE	SHT 11 OF 27	



Cache SIMM





Non-Volatile RAM

PART NUMBER	QTY	DESCRIPTION	ASSOCIATED REFERENCE DESIGNATORS
333S1192	1	IC, SRAM, 8Kx8, 70ns	U6

NVRAM, Cache slot, term.

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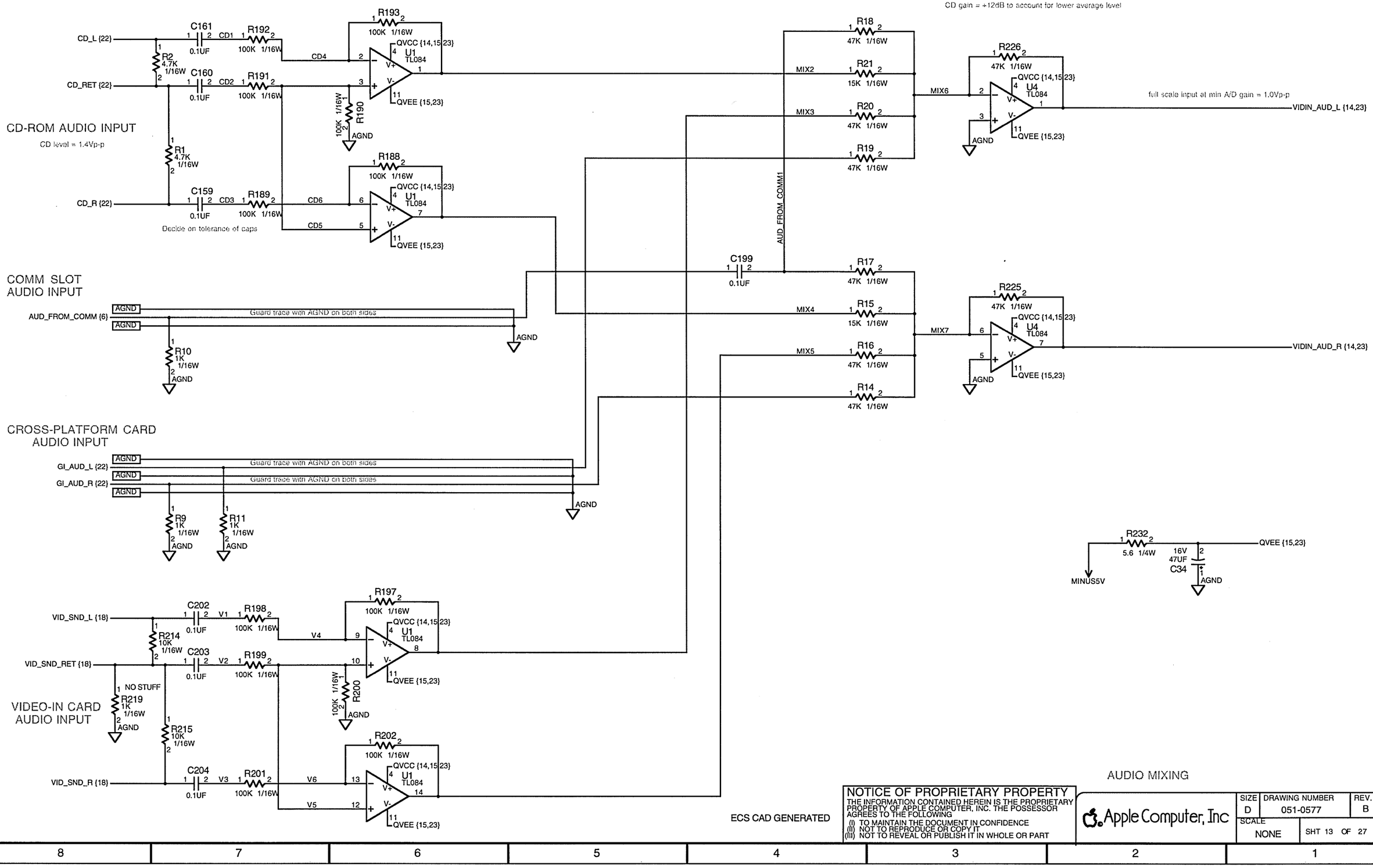
SCALE NONE	SHT 12 OF 27	


CD gain = +12dB to account for lower average level
CD-ROM AUDIO INPUT
CD level = 1.4Vp-p
CD_L {22}
CD_RET {22}
CD_R {22}
C161
C160
C159
0.1UF
R2 4.7K 1/16W
R1 4.7K 1/16W
R192
R191
R189
100K 1/16W
CD1
CD2
CD3
CD4
CD5
CD6
R193
R188
R190
100K 1/16W
U1 TL084
QVCC {14,15,23}
QVEE {15,23}
AGND
Decide on tolerance of caps
COMM SLOT AUDIO INPUT
AUD_FROM_COMM {6}
AGND
Guard trace with AGND on both sides
R10 1K 1/16W
CROSS-PLATFORM CARD AUDIO INPUT
GI_AUD_L {22}
GI_AUD_R {22}
R9 1K 1/16W
R11 1K 1/16W
VIDEO-IN CARD AUDIO INPUT
VID_SND_L {18}
VID_SND_RET {18}
VID_SND_R {18}
C202
C203
C204
R214 10K 1/16W
R219 1K 1/16W
NO STUFF
R215 10K 1/16W
R198
R199
R201
R197
R200
R202
V1
V2
V3
V4
V5
V6
AUD_FROM_COMM1
C199
R18
R21
R20
R19
R17
R15
R16
R14
47K 1/16W
15K 1/16W
MIX2
MIX3
MIX4
MIX5
R226
R225
U4 TL084
MIX6
MIX7
full scale input at min A/D gain = 1.0Vp-p
VIDIN_AUD_L {14,23}
VIDIN_AUD_R {14,23}
R232 5.6 1/4W
16V 47UF
C34
MINUS5V
AUDIO MIXING
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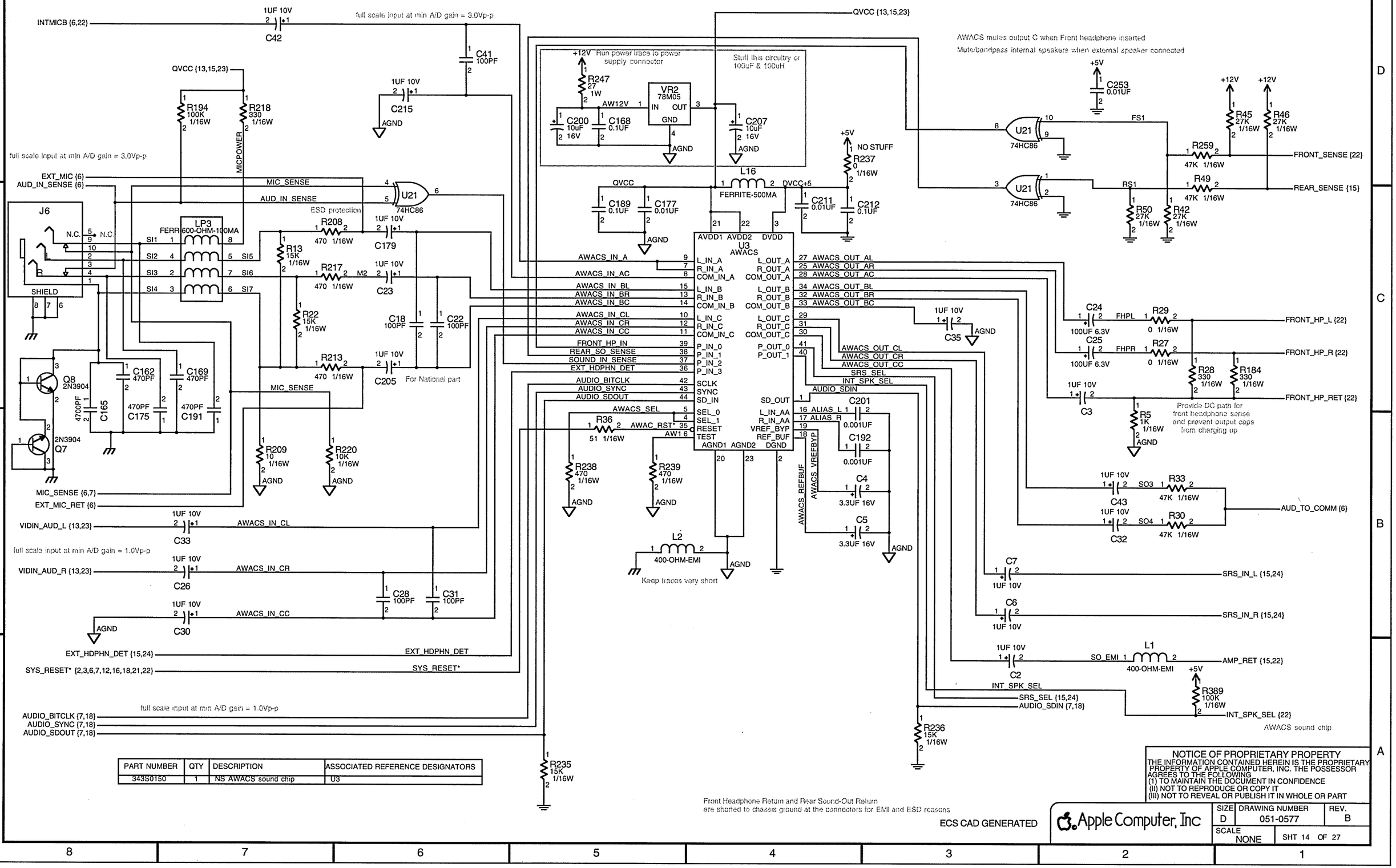
REV. B
SCALE NONE
SHT 13 OF 27



PART NUMBER	QTY	DESCRIPTION	ASSOCIATED REFERENCE DESIGNATORS
343S0150	1	NS AWACS sound chip	U3

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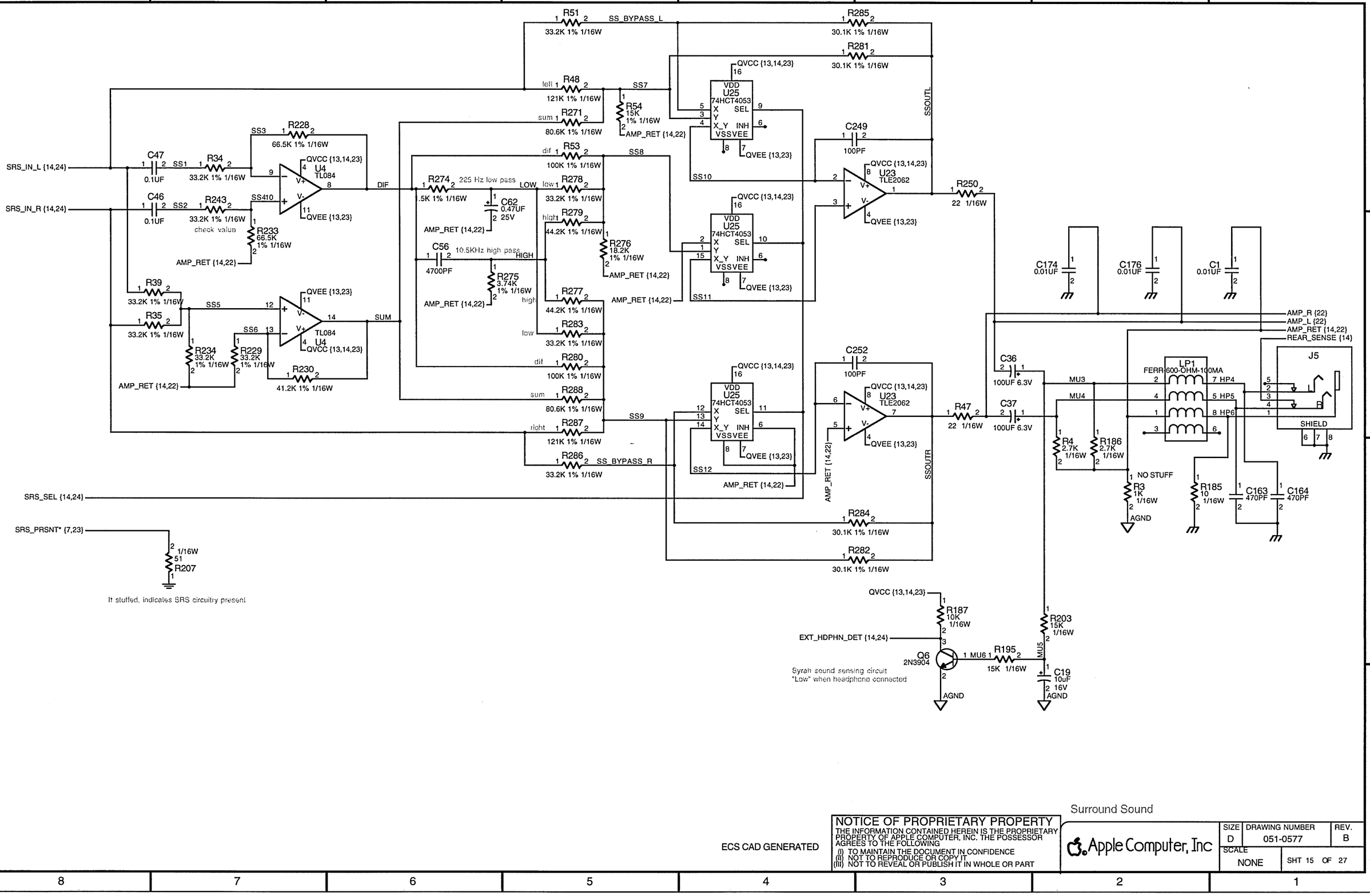
SIZE	DRAWING NUMBER	REV.
D	051-0577	B
SCALE NONE	SHT 14 OF 27	



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Surround Sound

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SIZE	DRAWING NUMBER	REV.
D	051-0577	B
SCALE		SHT 15 OF 27
NONE		

U13
ATI-264GT

ATI 3D GRAPHIC CHIP

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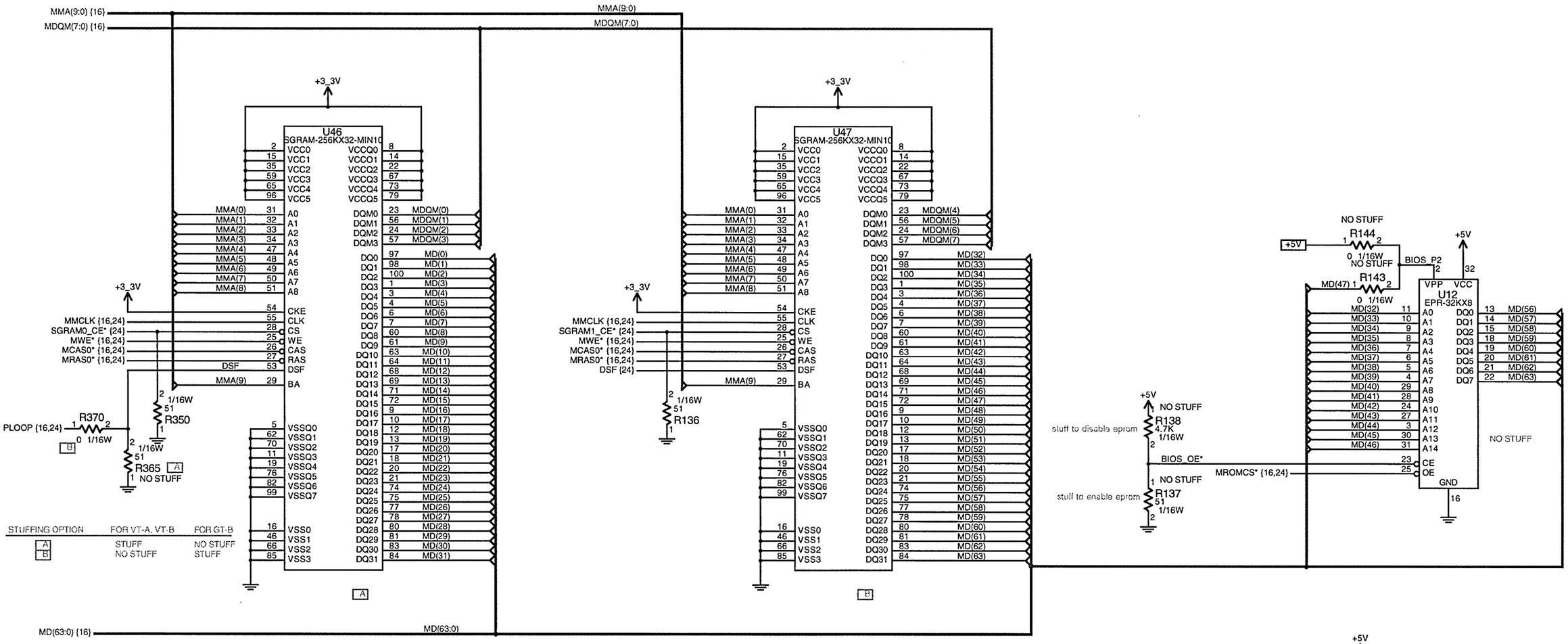
SIZE	DRAWING NUMBER	REV.
D	051-0577	B
SCALE NONE	SHT 16 OF 27	



VIDEO SGRAM & BIOS

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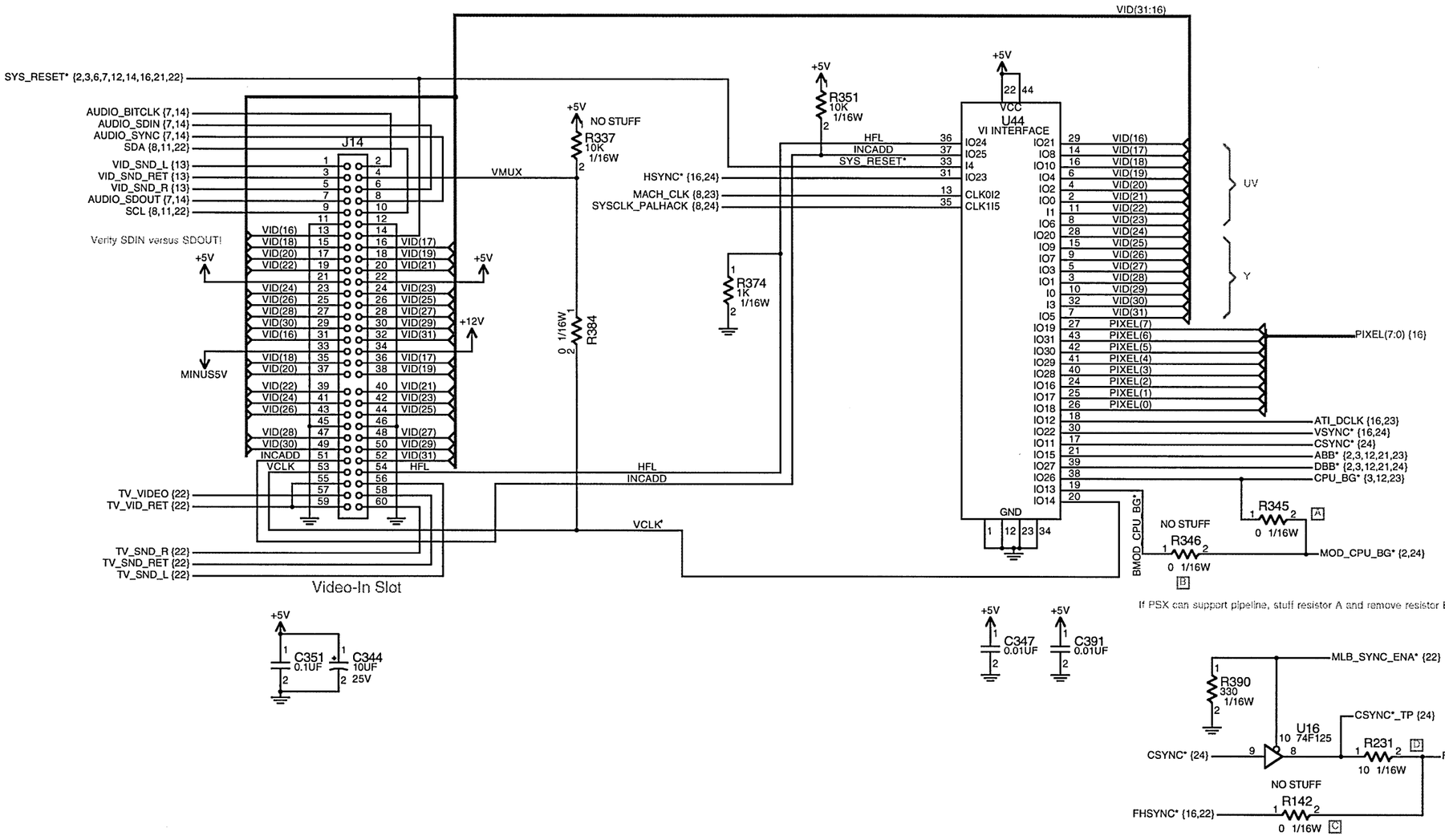
SIZE	DRAWING NUMBER	REV.
D	051-0577	B
SCALE: NONE	SHT 17 OF 27	



VIDEO-IN & MACH

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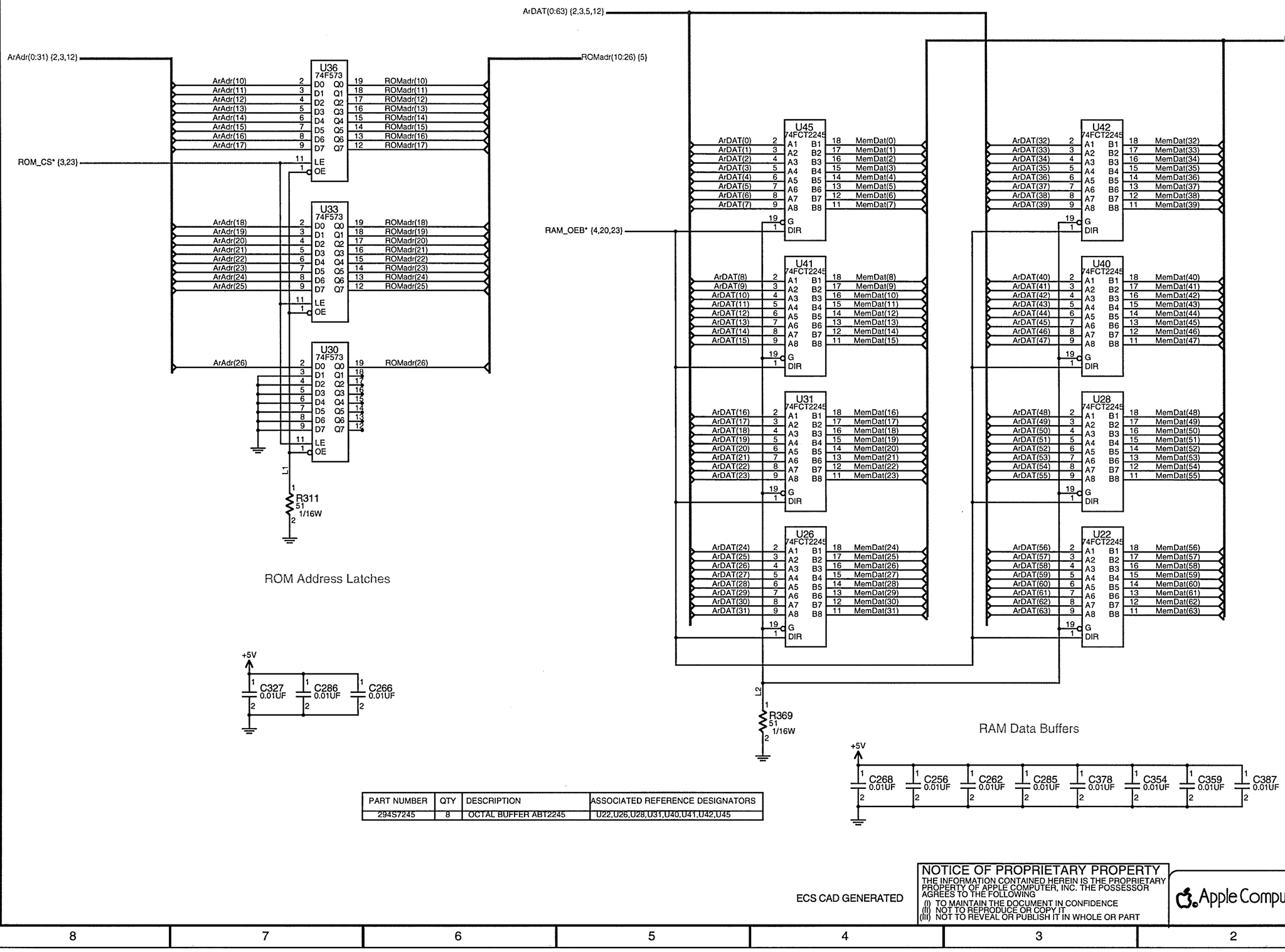
D	051-0577	B
SCALE: NONE	SHT 18 OF 27	



PART NUMBER	QTY	DESCRIPTION	ASSOCIATED REFERENCE DESIGNATORS
294S7245	8	OCTAL BUFFER ABT2245	U22,U26,U28,U31,U40,U41,U42,U45

Address and Data buffers

ECS CAD GENERATED

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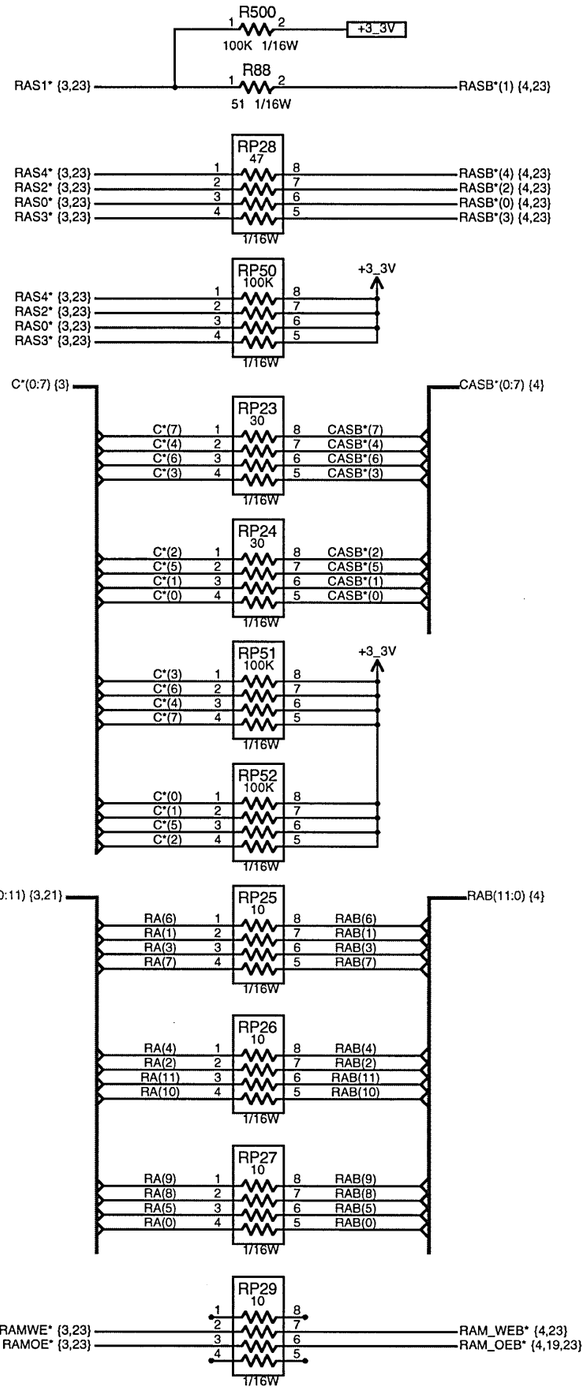
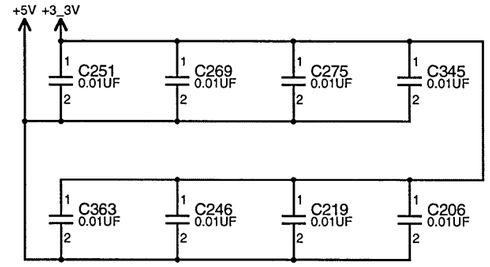
D	051-0577	B
SCALE NONE	SHT 19 OF 27	



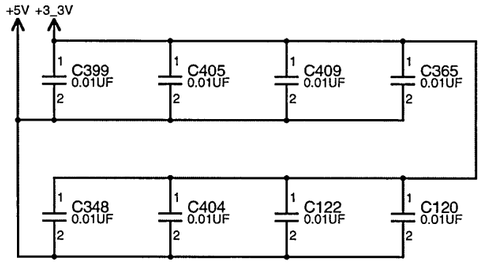
DRAM Termination

Place near PSX



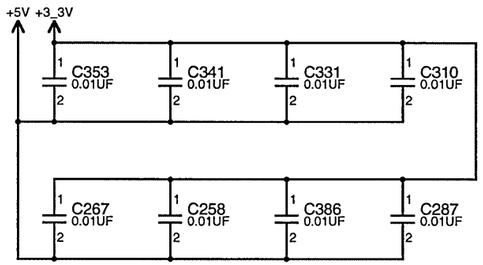
Decoupling for O'Hare

Place evenly around periphery of chip



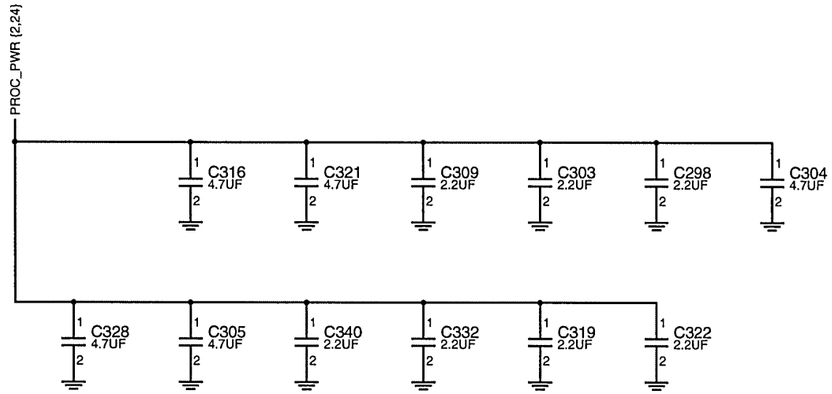
Decoupling for ATI264

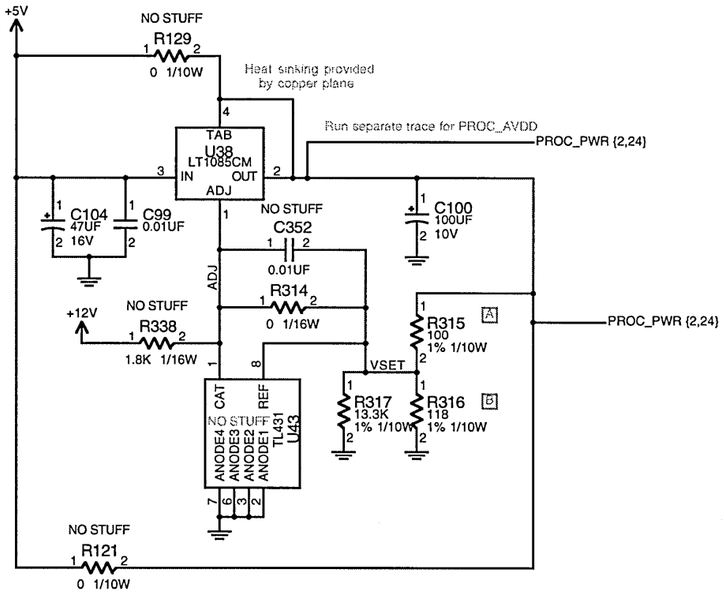
Place evenly around periphery of chip



Decoupling for L2 cache module

Place evenly around periphery of L2 DIMM





A/B	PROC_PWR
118/100 ohms for 2.309V	
118/110 ohms for 2.415V	
100/100 ohms for 2.5V	
100/110 ohms for 2.625V	
100/118 ohms for 2.725V	
100/121 ohms for 2.7625V	
100/133 ohms for 2.92V	

DRAM termination, decoupling, onboard regulator

PART NUMBER	QTY	DESCRIPTION	ASSOCIATED REFERENCE DESIGNATORS
805-1067	1	EMI Shield	
805-1618	1	Sound Jack EMI clip	
805-1518	1	GROUND CLIP	
820-0816	1	GAZELLE MLB PCB	PCB1
730-0101	1	Heaksink	HS1
600-3358	1	Heaksink with processor fan	HS1

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SIZE	DRAWING NUMBER	REV.
D	051-0577	B
SCALE	NONE	SHT 20 OF 27

O'Hare pullups

RP21 2.7K 1/16W: CFW* {3,7,23}, PSX_PCI_INT* {3,7,23}, COMM_SLOT_INT* {6,7}, PCI_SLOT_INT* {6,7} — +3_3V, +5V

RP20 10K 1/16W: PCI_SLOT3_INT* {6,7,12}, PCI_SLOT2_INT* {6,7}, PCI_VIDEO_REQ* {7,16,23}, PCI_SLOT2_REQ* {6,7} — +3_3V

RP19 2.7K 1/16W: PB_VOL_DECR {7,22}, PB_PICT_DECR {7,22}, PB_VOL_INCR {7,22}, PB_PICT_INCR {7,22} — +3_3V

RP22 2.7K 1/16W: CPU_INT* {2,7,23}, VIDEO_INT* {7,16,23} — +3_3V, +5V

Place near O'Hare?

RP5 2.7K 1/16W: IR_INT* {7,22}, TV_INT* {7,22}, NMI* {7,11,23} — +5V

R165, R272, R273, R224 4.7K 1/16W: +3_3V; BOXID0 {7,22}, BOXID1 {7,22,23}, BOXID2 {7,22,23}, CPUID3 {7,23}

R300 10K 1/16W: +3_3V; L2_BR* {3,12,23}, SNOOP_EN* {7,23}

Stuff to cause S/W to enable snooping

R8 51 1/16W — NO STUFF

R210, R265, R216 10K 1/16W: +3_3V; SCAN_IN2 {7,23}, INTRQ1* {7,23}, PGE_IRQ* {7,23}, DMAREQ1 {7,23}

R260 10K 1/16W

Clamp input to 3.3V to protect non-5V tolerant inputs of TI PSX

R84 20K 1/16W, D2 1N914: +3_3V

R56 10K 1/16W, D1 1N914: +3_3V

EDO1 {4,24} — R57 1K 1/16W

EDO2 {4,24} — R58 1K 1/16W

Select EDO mode only if all banks are EDO
Assumes PD5 grounded for Fast Page Mode, open otherwise

EDO3

L2_PRSNT {12,23} — R87 1K 1/16W — L2_PRSNTR

R73 1K 1/16W

Burst ROM | 60nS DRAM

R75, R68, R63, R77, R70, R59 1K 1/16W; R65 10K 1/16W: +3_3V

RA(0:11) {3,20}: RA(11), RA(10), RA(9), RA(8), RA(7), RA(6), RA(5), RA(4), RA(3), RA(2), RA(1), RA(0)

ROM_A0 {3,5,23}, ROM_A1 {3,5,23}

R135, R134 2K 1/16W — No self-refresh DRAM

R76, R69, R64, R78, R79, R71, R60, R80, R85, R72 2K 1/16W — NO STUFF

RA(1:0)=11 for 50MHz	No Burst ROM	No FLASH in DRAM space	Flash mapping	70nS DRAM	No EDO DRAM	System ID=00 for Entry Level design center	PCI bus number =01

Initialization settings for PSX

Processor pullups

R334, R333, R332 10K 1/16W: +3_3V; TTYPE(1) {2,3,12,23}, TTYPE(3) {2,3,12,23}, TBST* {2,3,12,24}

R107, R375, R306, R386, R120, R320, R331, R307, R110, R106, R379, R294 10K 1/16W: +3_3V; GBL* {2,3,12,24}, TA* {2,3,12,23}, TS* {2,3,12,24}, ARTRY* {2,3,12,23}, TBEN {2,24}, TLBISYNC {2,24}, SRESET* {2,12,23}, ABB* {2,3,12,18,23}, DBWO* {2,24}, DBB* {2,3,12,18,24}, AACK* {2,3,12,23}, TEA* {2,3,12,23}, DBG* {2,24}, DPE* {2,24}, APE* {2,24}

TTYPE(4), TTYPE(2), TTYPE(0) — TTYPE(4:0) {2,3,12}

R124, R126, R123, R125, R128, R309 1K 1/16W

Change pull down to 1k for PSX+

RP11 10K 1/16W: +3_3V; LSSD_MODE {2,24}, L1_TSTCLK {2,24}, L2_TSTCLK {2,24}, CKSTP* {2,24}

R127 51 1/16W

Stuff to increase uP output hold time

Stuff resistor to select No-DRTRY mode (interfereres with L2 cache operation)

R312 0 1/16W — NO STUFF

SYS_RESET* {2,3,6,7,12,14,16,18,22}

RP9 10K 1/16W: +3_3V; XATS* {2,24}, DBDIS* {2,24}, DRTRY* {2,24}, SMI* {2,24}

RP32 10K 1/16W — NO STUFF: +3_3V; 604_RUN {2,24}, 604_ARRARY_WR {2,24}, 604_XATS* {2,24}, 604_SHD* {2,24}

R340, R342 4.7K 1/16W — NO STUFF: +3_3V

604_DRVMOD0 {2,24}, 604_DRVMOD1 {2,24}

R339, R341 51 1/16W — NO STUFF

For 604

R119, R91, R335, R313 10K 1/16W: +3_3V; 603_MCP* {2,24}, TMS {2,3,7,23}, SHD* {12,23}, CACHE_INHIB* {2,12,23}, TCK {2,3,7,23}

R318 51 1/16W

0 1 2 3	Mode
H H H L	50/175MHz
H L H L	50/200MHz
L H H H	50/225MHz
H L H H	50/250MHz
H L L H	50/275MHz
H H L H	50/300MHz

AP(0:3) {2}

RP12 2.7K 1/16W: AP(0) AP(3) AP(2) AP(1)

DP(0:7) {2}

RP7 2.7K 1/16W: DP(0) DP(2) DP(1) DP(3)

RP6 2.7K 1/16W: DP(4) DP(5) DP(6) DP(7)

R132, R133, R131, R130 4.7K 1/16W: +3_3V — NO STUFF

PLL_CONFIG3 {2,24}, PLL_CONFIG2 {2,24}, PLL_CONFIG1 {2,24}, PLL_CONFIG0 {2,24}

R326, R330, R329, R328 51 1/16W — NO STUFF

Pullups, Pulldowns

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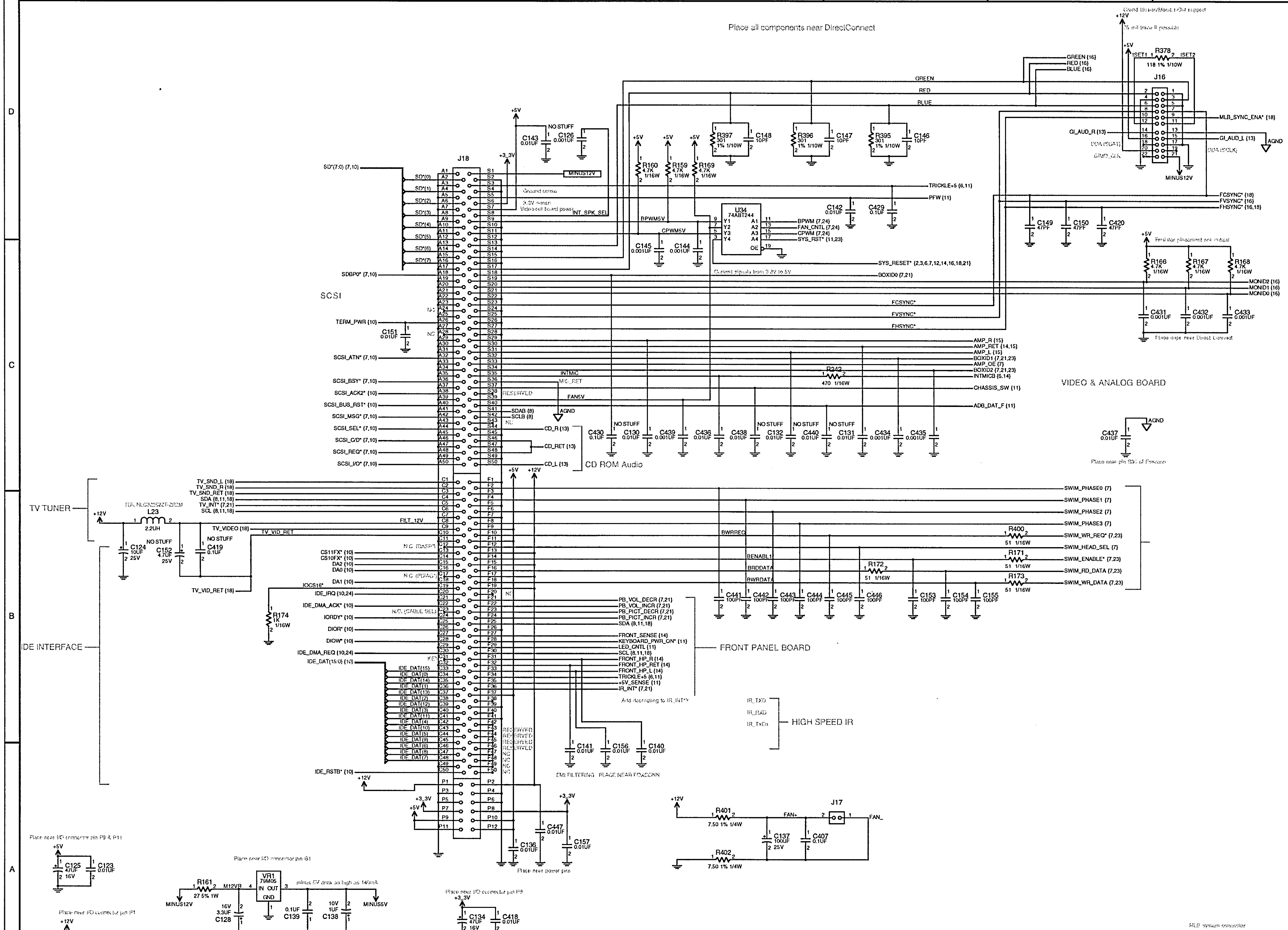
Apple Computer, Inc

SIZE	DRAWING NUMBER	REV.
D	051-0577	B
SCALE: NONE	SHT 21 OF 27	



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Apple Computer, Inc

SIZE	DRAWING NUMBER	REV.
E	051-0577	B
SCALE NONE	SHT 22 OF 27	

AACK* {2,3,12,21} — TP441
ABB* {2,3,12,18,21} — TP334
ACKF {10} — TP73
ACKOUT* {7,10} — TP65
ADB_IN {11} — TP152
ADB_OUT {11} — TP157
ALIAS_L {14} — TP39
ALIAS_R {14} — TP26

ARTRY* {2,3,12,21} — TP440
ATHEN_AVDD {8} — TP655
ATHEN_VDD {8} — TP665
AUD1 {7} — TP22
AUD2 {7} — TP23

AW1 {14} — TP111

AWACS_IN_A {14} — TP120
AWACS_IN_BC {14} — TP48
AWACS_IN_BL {14} — TP35
AWACS_IN_BR {14} — TP55
AWACS_IN_CC {14} — TP80
AWACS_IN_CL {14} — TP96
AWACS_IN_CR {14} — TP61
AWACS_OUT_AC {14} — TP19
AWACS_OUT_AL {14} — TP45
AWACS_OUT_AR {14} — TP30
AWACS_OUT_BL {14} — TP60
AWACS_OUT_BR {14} — TP47
AWACS_REFBUF {14} — TP20
AWACS_SEL {14} — TP103
AWACS_VREFBYP {14} — TP14

ArAdr(12) {2,3,12,19} — TP433

ArAdr(15) {2,3,12,19} — TP340
ArAdr(16) {2,3,12,19} — TP682
ArAdr(17) {2,3,12,19} — TP345
ArAdr(18) {2,3,12,19} — TP670
ArAdr(19) {2,3,12,19} — TP328

ArAdr(21) {2,3,12,19} — TP687
ArAdr(22) {2,3,12,19} — TP448
ArAdr(23) {2,3,12,19} — TP353

ArAdr(25) {2,3,12,19} — TP343
ArAdr(26) {2,3,12,19} — TP657
ArAdr(27) {2,3,12} — TP336
ArAdr(28) {2,3,12} — TP647
ArAdr(29) {2,3,12} — TP354

ArAdr(30) {2,3,12} — TP648
ArAdr(31) {2,3,12} — TP344
ArAdr(4) {2,3,12} — TP698

ArDAT(0) {2,3,5,12,19} — TP366
ArDAT(1) {2,3,5,12,19} — TP390
ArDAT(10) {2,3,5,12,19} — TP391
ArDAT(11) {2,3,5,12,19} — TP359
ArDAT(12) {2,3,5,12,19} — TP379
ArDAT(13) {2,3,5,12,19} — TP367
ArDAT(14) {2,3,5,12,19} — TP351
ArDAT(15) {2,3,5,12,19} — TP352
ArDAT(16) {2,3,5,12,19} — TP368
ArDAT(17) {2,3,5,12,19} — TP363
ArDAT(18) {2,3,5,12,19} — TP376
ArDAT(19) {2,3,5,12,19} — TP377
ArDAT(2) {2,3,5,12,19} — TP358
ArDAT(20) {2,3,5,12,19} — TP380
ArDAT(21) {2,3,5,12,19} — TP339
ArDAT(22) {2,3,5,12,19} — TP392
ArDAT(23) {2,3,5,12,19} — TP382
ArDAT(24) {2,3,5,12,19} — TP332
ArDAT(25) {2,3,5,12,19} — TP271
ArDAT(26) {2,3,5,12,19} — TP270
ArDAT(27) {2,3,5,12,19} — TP263
ArDAT(28) {2,3,5,12,19} — TP253
ArDAT(29) {2,3,5,12,19} — TP244
ArDAT(3) {2,3,5,12,19} — TP542
ArDAT(30) {2,3,5,12,19} — TP232
ArDAT(31) {2,3,5,12,19} — TP218
ArDAT(32) {2,3,5,12,19} — TP538
ArDAT(33) {2,3,5,12,19} — TP639
ArDAT(34) {2,3,5,12,19} — TP549
ArDAT(35) {2,3,5,12,19} — TP627
ArDAT(36) {2,3,5,12,19} — TP613
ArDAT(37) {2,3,5,12,19} — TP541
ArDAT(38) {2,3,5,12,19} — TP598
ArDAT(39) {2,3,5,12,19} — TP535
ArDAT(4) {2,3,5,12,19} — TP374
ArDAT(40) {2,3,5,12,19} — TP587
ArDAT(41) {2,3,5,12,19} — TP572
ArDAT(42) {2,3,5,12,19} — TP556
ArDAT(43) {2,3,5,12,19} — TP559
ArDAT(44) {2,3,5,12,19} — TP528
ArDAT(45) {2,3,5,12,19} — TP554
ArDAT(46) {2,3,5,12,19} — TP546
ArDAT(47) {2,3,5,12,19} — TP532
ArDAT(48) {2,3,5,12,19} — TP310
ArDAT(49) {2,3,5,12,19} — TP305
ArDAT(5) {2,3,5,12,19} — TP375

ArDAT(51) {2,3,5,12,19} — TP294
ArDAT(52) {2,3,5,12,19} — TP606
ArDAT(53) {2,3,5,12,19} — TP288
ArDAT(54) {2,3,5,12,19} — TP608
ArDAT(55) {2,3,5,12,19} — TP282
ArDAT(56) {2,3,5,12,19} — TP216

ArDAT(57) {2,3,5,12,19} — TP205
ArDAT(58) {2,3,5,12,19} — TP203
ArDAT(59) {2,3,5,12,19} — TP202
ArDAT(6) {2,3,5,12,19} — TP588
ArDAT(60) {2,3,5,12,19} — TP252
ArDAT(61) {2,3,5,12,19} — TP231
ArDAT(62) {2,3,5,12,19} — TP192
ArDAT(63) {2,3,5,12,19} — TP215
ArDAT(7) {2,3,5,12,19} — TP595
ArDAT(8) {2,3,5,12,19} — TP378
ArDAT(9) {2,3,5,12,19} — TP543
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C*(0) {3,20} — TP243
C*(1) {3,20} — TP262
C*(2) {3,20} — TP230
C*(3) {3,20} — TP242
C*(4) {3,20} — TP228
C*(5) {3,20} — TP217
C*(6) {3,20} — TP229
C*(7) {3,20} — TP240
C32CLK {8} — TP706
C32M_OHARE {7,8} — TP688

CACHE_EN {3,12} — TP290
CACHE_HIT* {3,12} — TP303
CACHE_INHIB* {2,12,21} — TP470
CASB*(0) {4,20} — TP493
CASB*(1) {4,20} — TP492
CASB*(2) {4,20} — TP447
CASB*(3) {4,20} — TP446
CASB*(4) {4,20} — TP397
CASB*(5) {4,20} — TP410
CASB*(6) {4,20} — TP373
CASB*(7) {4,20} — TP396
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CD2 {13} — TP6
CD3 {13} — TP5
CD4 {13} — TP13
CD5 {13} — TP12
CD6 {13} — TP11
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BOXID2 {7,21,22} — TP81
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CPU_BR* {2,12} — TP496
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CR0 {10} — TP773
CR1 {10} — TP774
CR10 {10} — TP755
CR11 {10} — TP754
CR12 {10} — TP753
CR13 {10} — TP752
CR14 {10} — TP751
CR15 {10} — TP750
CR2 {10} — TP775
CR3 {10} — TP776

CR4 {10} — TP777
CR5 {10} — TP778
CR6 {10} — TP779
CR7 {10} — TP780
CR8 {10} — TP757
CR9 {10} — TP756

CUDA_IRQ_TST {11} — TP83
CUDA_OSCOUT {11} — TP84
CUDA_RESET* {11} — TP127
CUDA_VDD {11,12} — TP125

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SRS_PRSNT* {7,15} — TP44
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DMAREQ1 {7,21} — TP164

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F5V {10,11} — TP74
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FDA(2) {7,10,12} — TP171
FDA(3) {7,12} — TP130
FDA(4) {7,12} — TP131
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FILTERED_REQ* {7} — TP21

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H1 {12} — TP140

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IDE0_CS1* {7,10} — TP165
IDE0_CS3* {7,10} — TP161
IDE0_DMA_ACK* {7,10} — TP172
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IDE_DIOW* {7,10,12} — TP100
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L2_BR* {3,12,21} — TP325
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M2 {14} — TP62

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SI5 {14} — TP49
SI6 {14} — TP63
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MIX3 {13} — TP29
MIX4 {13} — TP4
MIX5 {13} — TP34
MIX6 {13} — TP79
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MemDat(10) {4,19} — TP557
MemDat(11) {4,19} — TP555
MemDat(12) {4,19} — TP548
MemDat(13) {4,19} — TP540
MemDat(14) {4,19} — TP534
MemDat(15) {4,19} — TP531
MemDat(16) {4,19} — TP372
MemDat(17) {4,19} — TP355
MemDat(18) {4,19} — TP364
MemDat(19) {4,19} — TP356
MemDat(20) {4,19} — TP341
MemDat(21) {4,19} — TP357
MemDat(22) {4,19} — TP326
MemDat(23) {4,19} — TP322
MemDat(24) {4,19} — TP295
MemDat(25) {4,19} — TP291
MemDat(26) {4,19} — TP279
MemDat(27) {4,19} — TP275
MemDat(28) {4,19} — TP268
MemDat(29) {4,19} — TP221
MemDat(30) {4,19} — TP264
MemDat(31) {4,19} — TP220
MemDat(40) {4,19} — TP567
MemDat(41) {4,19} — TP561

TDO {7} — TP24

MemDat(42) {4,19} — TP530
MemDat(43) {4,19} — TP551
MemDat(44) {4,19} — TP547
MemDat(45) {4,19} — TP544
MemDat(46) {4,19} — TP533
MemDat(47) {4,19} — TP525
MemDat(48) {4,19} — TP306
MemDat(49) {4,19} — TP307

MemDat(50) {4,19} — TP311
MemDat(51) {4,19} — TP298
MemDat(52) {4,19} — TP289
MemDat(53) {4,19} — TP283
MemDat(54) {4,19} — TP314
MemDat(55) {4,19} — TP278
MemDat(56) {4,19} — TP206
MemDat(57) {4,19} — TP219
MemDat(58) {4,19} — TP201
MemDat(59) {4,19} — TP198

MemDat(60) {4,19} — TP195
MemDat(61) {4,19} — TP191
MemDat(62) {4,19} — TP186
MemDat(63) {4,19} — TP178

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MemDat(9) {4,19} — TP560
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RA(10) {3,20,21} — TP241
RA(11) {3,20,21} — TP227
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RA(3) {3,20,21} — TP233
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RA(5) {3,20,21} — TP247
RA(6) {3,20,21} — TP249
RA(7) {3,20,21} — TP261
RA(8) {3,20,21} — TP248
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RAB(0) {4,20} — TP223
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RAB(10) {4,20} — TP212
RAB(11) {4,20} — TP434
RAB(2) {4,20} — TP224
RAB(3) {4,20} — TP438
RAB(4) {4,20} — TP514
RAB(5) {4,20} — TP507
RAB(6) {4,20} — TP511
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RAS1* {3,20} — TP257
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RAS1B* {4} — TP437
RAS2* {3,20} — TP266
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RAS2B* {4} — TP426
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RAS3B* {4} — TP403
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RASB*(1) {4,20} — TP302
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ROM_A0 {3,5,21} — TP360
ROM_A1 {3,5,21} — TP331
ROM_CS* {3,19} — TP472
ROM_OE* {3,5} — TP346
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ROMadr(11) {5,19} — TP450
ROMadr(12) {5,19} — TP449
ROMadr(13) {5,19} — TP443
ROMadr(14) {5,19} — TP442
ROMadr(15) {5,19} — TP432
ROMadr(16) {5,19} — TP471
ROMadr(17) {5,19} — TP430
ROMadr(18) {5,19} — TP400

ROMadr(19) {5,19} — TP406
ROMadr(20) {5,19} — TP398
ROMadr(21) {5,19} — TP401
ROMadr(22) {5,19} — TP395
ROMadr(23) {5,19} — TP394
ROMadr(24) {5,19} — TP393
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TSIZ(2) {2,3,12} — TP503
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TTYPE(1) {2,3,12,21} — TP513
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TTYPE(3) {2,3,12,21} — TP515
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V1 {13} — TP36
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V3 {13} — TP33
V4 {13} — TP15
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Test Points

Test points

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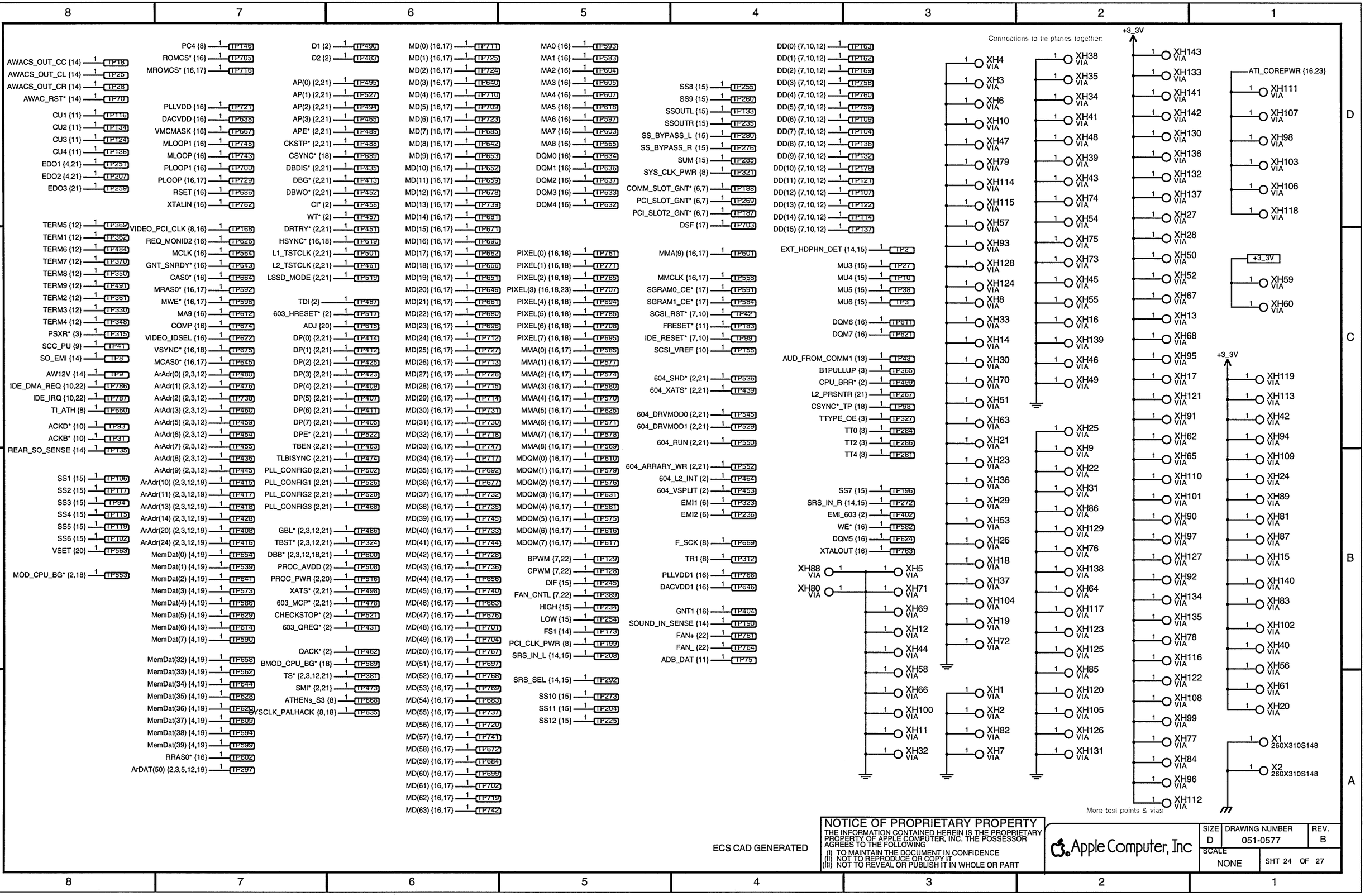
Apple Computer, Inc

SIZE	DRAWING NUMBER	REV.
D	051-0577	B
SCALE: NONE	SHT 23 OF 27	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AWAC_RST* {14}
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CU2 {11}
CU3 {11}
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SS3 {15}
SS4 {15}
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MLOOP1 {16}
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PLOOP {16,17}
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VIDEO_PCI_CLK {8,16}
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MCAS0* {16,17}
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ArAdr(1) {2,3,12}
ArAdr(2) {2,3,12}
ArAdr(3) {2,3,12}
ArAdr(5) {2,3,12}
ArAdr(6) {2,3,12}
ArAdr(7) {2,3,12}
ArAdr(8) {2,3,12}
ArAdr(9) {2,3,12}
ArAdr(10) {2,3,12,19}
ArAdr(11) {2,3,12,19}
ArAdr(13) {2,3,12,19}
ArAdr(14) {2,3,12,19}
ArAdr(20) {2,3,12,19}
ArAdr(24) {2,3,12,19}
MemDat(0) {4,19}
MemDat(1) {4,19}
MemDat(2) {4,19}
MemDat(3) {4,19}
MemDat(4) {4,19}
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R21 13-D4
R22 14-C7
R23 9-C7
R24 9-D7
R25 10-B7
R26 11-C3
R27 14-C2
R28 14-C2
R29 14-C2
R30 14-B2
R31 11-C6
R32 11-D5
R33 14-B2
R34 15-D7
R35 15-C8
R36 14-B5
R37 9-C6
R38 11-D6
R39 15-C8
R40 11-D5
R41 11-D5
R42 14-C2
R43 8-A3
R44 10-B5
R45 14-D1
R46 14-D1
R47 15-C3
R48 15-D5
R49 14-C2
R50 14-C2
R51 15-D5
R52 6-C2
R53 15-D5
R54 15-D5
R55 6-B5
R56 21-B6
R57 21-B6
R58 21-B6
R59 21-B6
R60 21-A6
R61 6-B1
R62 6-B1
R63 21-B7
R64 21-A7
R65 21-B5
R66 6-C2
R67 3-D2
R68 21-B7
R69 21-A7
R70 21-B6
R71 21-A6
R72 21-A5
R73 21-B7
R74 3-D2
R75 21-B7
R76 21-A7
R77 21-B6
R78 21-A7
R79 21-A6
R80 21-A6
R81 3-A6
R82 3-A7
R83 3-A6
R84 21-B7
R85 21-A5
R86 6-B2
R87 21-B7
R88 20-D7
R89 3-B8
R90 3-B8
R91 21-B3
R92 3-B8
R93 3-A2
R94 3-A2
R95 8-A7
R96 3-B7
R97 6-C8
R98 8-A5
R99 6-B2
R100 6-B2
R101 6-B1
R102 6-B1
R103 6-C6
R104 6-B2
R105 16-A1
R106 21-D2
R107 21-D4
R108 6-A2
R109 6-A2
R110 21-D2
R111 2-A4
R112 2-A5
R113 2-B7
R114 6-B1
R115 6-B1
R116 2-B8
R117 2-A7
R118 2-A8
R119 21-B3
R120 21-D3
R121 20-A3
R122 20-B3
R123 21-C3
R124 21-C3
R125 21-C2
R126 21-C3
R127 21-C4
R128 21-C2
R129 20-C3
R130 21-B1
R131 21-B1
R132 21-B2
R133 21-B1
R134 21-A8
R135 21-A8
R136 17-C5
R137 17-B3
R138 17-B3
R139 16-A7
R140 16-A3
R141 16-A3
R142 18-A3
R143 17-C2
R144 17-C2
R145 16-B8
R146 8-B7
R147 8-B7
R148 8-B5
R149 16-B7
R150 10-A5
R151 10-A6
R152 10-A6
R153 10-A6
R154 10-A6
R155 10-A6
R156 10-A6
R157 10-A7
R158 16-A8
R159 22-D4
R160 22-D5
R161 22-A7
R162 8-B2
R163 10-C5
R164 10-C5
R165 21-C6
R166 22-C2
R167 22-C1
R168 22-C1
R169 22-D4
R170 8-B2
R171 22-B2
R172 22-B3
R173 22-B2
R174 22-B7
R175 10-B5
R176 10-A7
R177 10-A7
R178 10-A6
R179 10-A6
R180 10-A6
R181 10-A6
R182 10-A6
R183 10-A5
R184 14-C1
R185 15-B2
R186 15-B2
R187 15-B3
R188 13-D6
R189 13-C7
R190 13-D6
R191 13-D7
R192 13-D7
R193 13-D6
R194 14-D7
R195 15-B3
R196 7-B2
R197 13-B6
R198 13-B7
R199 13-A7
R200 13-A6
R201 13-A7
R202 13-A6
R203 15-B2
R204 10-C6
R205 7-A3
R206 7-A3
R207 15-B7
R208 14-C7
R209 14-B7
R210 21-C8
R211 10-C6
R212 10-C7
R213 14-C7
R214 13-A7
R215 13-A7
R216 21-C7
R217 14-C7
R218 14-D7
R219 13-A8
R220 14-B7
R221 11-B6
R222 11-C6
R223 11-C2
R224 21-C6
R225 13-C3
R226 13-D3
R227 11-B3
R228 15-D7
R229 15-C7
R230 15-C7
R231 18-B2
R232 13-B2
R233 15-C7
R234 15-C7
R235 14-A5
R236 14-A3
R237 14-D4
R238 14-B5
R239 14-B5
R240 10-C7
R241 11-B4
R242 22-C4
R243 15-D7
R244 10-C8
R245 10-C7
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R247 14-D5
R248 11-B7
R249 12-B2
R250 15-D3
R251 11-C5
R252 11-C4
R253 11-C4
R254 8-A2
R255 8-A2
R256 8-A2
R257 11-C6
R258 11-B4
R259 14-D2
R260 21-B8
R261 11-C4
R262 11-C4
R263 11-A4
R264 7-C8
R265 21-C7
R266 8-B3
R267 8-B3
R268 8-B2
R269 8-B2
R270 8-B2
R271 15-D5
R272 21-C6
R273 21-C6
R274 15-D6
R275 15-C6
R276 15-C5
R277 15-C5
R278 15-D5
R279 15-C5
R280 15-C5
R281 15-D4
R282 15-B4
R283 15-C5
R284 15-B4
R285 15-D4
R286 15-B5
R287 15-C5
R288 15-C5
R289 8-A5
R290 8-A5
R291 8-B5
R292 8-B6
R293 8-A7
R294 21-D1
R295 3-B8
R296 12-D4
R297 12-C6
R298 12-B4
R299 12-C4
R300 21-C5
R301 12-D4
R302 3-A8
R303 12-C4
R304 12-B4
R305 12-D4
R306 21-D3
R307 21-D2
R308 4-A7
R309 21-C2
R310 6-B6
R311 19-B7
R312 21-B3
R313 21-B2
R314 20-B2
R315 20-B2
R316 20-B2
R317 20-B2
R318 21-B3
R319 2-A7
R320 21-D3
R321 2-A8
R322 12-C4
R323 2-D2
R324 2-D8
R325 12-B4
R326 21-A2
R327 2-A7
R328 21-A1
R329 21-A1
R330 21-A1
R331 21-D2
R332 21-D4
R333 21-D5
R334 21-D5
R335 21-B2
R336 5-A6
R337 18-C5
R338 20-B3
R339 21-A4
R340 21-A4
R341 21-A4
R342 21-A4
R343 16-B3
R344 16-A7
R345 18-B3
R346 18-B3
R347 16-A7
R348 16-B3
R349 16-A7
R350 17-C8
R351 18-D5
R352 16-B3
R353 16-A7
R354 16-D7
R355 8-D6
R356 8-D6
R357 16-B2
R358 16-D8
R359 16-D8
R360 8-C5
R361 16-B3
R362 8-C5
R363 16-B8
R364 16-A2
R365 17-C8
R366 16-A3
R367 16-A7
R368 8-C4
R369 19-A4
R370 17-C8
R371 16-A6
R372 16-A3
R373 8-C3
R374 18-C5
R375 21-D4
R376 16-B7
R377 8-C6
R378 22-D2
R379 21-D1
R380 16-C7
R381 8-C6
R382 16-D2
R383 16-D2
R384 18-C5
R385 16-C8
R386 21-D3
R387 16-D8
R388 16-D8
R389 14-A2
R390 18-B3
R391 16-C7
R392 16-C7
R393 16-C7
R394 16-C7
R395 22-D3
R396 22-D4
R397 22-D4
R398 10-C5
R399 10-C5
R400 22-B2
R401 22-A4
R402 22-A4
R500 20-D7

RP1 7-A8
RP2 7-A8
RP3 10-B7
RP4 10-C7
RP5 21-D6
RP6 21-B1
RP7 21-B1
RP8 6-D1
RP9 21-B3
RP10 6-C1
RP11 21-C4
RP12 21-C1
RP13 16-C3
RP14 16-C3
RP15 10-B7
RP16 10-B7
RP17 10-A7
RP18 10-A7
RP19 21-C8
RP20 21-D8
RP21 21-D8
RP22 21-D6
RP23 20-C7
RP24 20-C7
RP25 20-B7
RP26 20-B7
RP27 20-A7
RP28 20-D7
RP29 20-A7
RP30 4-A5
RP31 4-A5
RP32 21-B4
RP33 16-B3
RP34 16-B3
RP35 16-B1
RP50 20-D7
RP51 20-C7
RP52 20-B7

S1 11-B7

U1 13-A6
U2 9-A7
U3 14-B5
U4 13-C3
U5 7-A7
U6 12-B2
U7 8-A3
U8 8-A6
U9 5-C7
U10 2-A7
U11 5-A7
U12 17-B2
U13 16-A6
U14 8-C5
U15 9-C7
U16 9-C7
U17 10-A3
U18 11-B5
U19 11-C8
U20 6-C6
U21 7-A2
U22 19-B3
U23 15-C4
U24 4-C7
U25 15-B4
U26 19-B4
U27 3-A7
U28 19-B3
U29 4-C6
U30 19-B7
U31 19-B4
U32 4-A7
U33 19-C7
U34 4-A7
U35 5-C5
U36 19-D7
U37 4-A6
U38 20-B3
U39 5-A5
U40 19-C3
U41 19-C4
U42 19-C3
U43 20-A2
U44 18-B4
U45 19-C4
U46 17-B7
U47 17-B5

VR1 22-A7
VR2 14-D5

W1 11-C3

X1 24-A1
X2 24-A1
X5 2-B1

XH1 24-A3
XH2 24-A3
XH3 24-D3
XH4 24-D3
XH5 24-B3
XH6 24-D3
XH7 24-A3
XH8 24-C3
XH9 24-B2
XH10 24-D3
XH11 24-A3
XH12 24-B3
XH13 24-C2
XH14 24-C3
XH15 24-B1
XH16 24-C2
XH17 24-C2
XH18 24-B3
XH19 24-B3
XH20 24-A1
XH21 24-C3
XH22 24-B2
XH23 24-B3
XH24 24-B1
XH25 24-C2
XH26 24-B3
XH27 24-D2
XH28 24-C2
XH29 24-B3
XH30 24-C3
XH31 24-B2
XH32 24-A3
XH33 24-C3
XH34 24-D2
XH35 24-D2
XH36 24-B3
XH37 24-B3
XH38 24-D2
XH39 24-D2
XH40 24-B1
XH41 24-D2
XH42 24-C1
XH43 24-D2
XH44 24-B3
XH45 24-C2
XH46 24-C2
XH47 24-D3
XH48 24-D2
XH49 24-C2
XH50 24-C2
XH51 24-C3
XH52 24-C2
XH53 24-B3
XH54 24-D2
XH55 24-C2
XH56 24-B1
XH57 24-D3
XH58 24-A3
XH59 24-C1
XH60 24-C1
XH61 24-A1
XH62 24-C2
XH63 24-C3
XH64 24-B2
XH65 24-B2
XH66 24-A3
XH67 24-C2
XH68 24-C2
XH69 24-B3
XH70 24-C3
XH71 24-B3
XH72 24-B3
XH73 24-C2
XH74 24-D2
XH75 24-C2
XH76 24-B2
XH77 24-A2
XH78 24-B2
XH79 24-D3
XH80 24-B3
XH81 24-B1
XH82 24-A3
XH83 24-B1
XH84 24-A2
XH85 24-A2
XH86 24-B2
XH87 24-B1
XH88 24-B3
XH89 24-B1
XH90 24-B2
XH91 24-C2
XH92 24-B2
XH93 24-C3
XH94 24-C1
XH95 24-C2
XH96 24-A2
XH97 24-B2
XH98 24-D1
XH99 24-A2
XH100 24-A3
XH101 24-B2
XH102 24-B1
XH103 24-D1
XH104 24-B3
XH105 24-A2
XH106 24-D1
XH107 24-D1
XH108 24-A2
XH109 24-B1
XH110 24-B2
XH111 24-D1
XH112 24-A2
XH113 24-C1
XH114 24-D3
XH115 24-D3
XH116 24-B2
XH117 24-B2
XH118 24-D1
XH119 24-C1
XH120 24-A2
XH121 24-C2
XH122 24-A2
XH123 24-B2
XH124 24-C3
XH125 24-B2
XH126 24-A2
XH127 24-B2
XH128 24-C3
XH129 24-B2
XH130 24-D2
XH131 24-A2
XH132 24-D2
XH133 24-D2
XH134 24-B2
XH135 24-B2
XH136 24-D2
XH137 24-D2
XH138 24-B2
XH139 24-C2
XH140 24-B1
XH141 24-D2
XH142 24-D2
XH143 24-D2

Y1 11-C6
Y2 11-C6
Y3 8-B3
Y4 8-A7
Y5 8-C6
Y6 16-B8

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C448	
D9	
F1	
HS1	
J18	
L23	
LP3	
Q10	
R500	R403-499
RP52	RP36-49
S1	
TP787	
U47	
VR2	
W1	
X5	X3-4
XH143	
Y6	

ECS CAD GENERATED

REF Designator Summary

Apple Computer, Inc

SIZE	DRAWING NUMBER	REV.
D	051-0577	B
SCALE: NONE	SHT 25 OF 27	

Version V1	1/15/96
All sheets	Duplicate Alchemy EVT4
Sheet 15	Remove Valky AR. Add ATI264
Sheet 24	Add 4pcs 256kx16 EDO DRAM as video buffer
Sheet 25	Add VI connector and Mach for VI interface
Sheet 2	Change 603e to 603eV
Sheet 19	Add voltage regulator for uP core voltage

Version V1	2/1/96
Sheet 10	Change passive SCSI term to active
Sheet 23	Repin VI Mach's pixel signals
	Use MACH_CLK instead of C32M_VID as clk for VI Mach

Version V1	2/5/96
Sheet 10	Remove active SCSI term.
Sheet 15	Run ATI_DCLK from VI Mach to ATI's DCLK
Sheet 23	Repin HSYNC* at VI Mach
	Connect VCLK from VI Mach to VMUX of VI slot

Version V1 --> use for pre EVT1	2/12/96
All sheets	Rename all ref designators

Version V2 --> use for EVT1	2/12/96

Version V3	2/13/96
Sheet 15	Add decoupling caps to ATI264
Sheet 19	Add decoupling caps btw 5v and 3.3v around ATI264

Version V3	2/15/96
Sheet 15	Change monitor ID 0 to pin136 of ATI264
Sheet 6	Correct the connection of PCI_VIDEO_REQ* to PCI slot

Version V3	2/17/96
Sheet 15	Add more res stuffing option for GT-B

Version V3	2/23/96
Sheet 2	Change heatsink to 790-0074 (blue heatsink)
Sheet 15	Change stuffing to supply 3.3v to AVdd of ATI264
	Change stuffing to enable VGA mode for ATI264
Sheet 24	Run ROMCS from ATI264 to enable OE* of Bios eprom
Sheet 23	Change VI Mach from Mach110 to Mach211

Version V3	3/4/96
Sheet 15,24	Change video buffer to SGRAM

Version V3	3/5/96
Sheet 8	Delete GIMO clk
Sheet 10	Change passive SCSI term to active

Version V3	3/6/96
Sheet 19	Delete regulator for uP core. Use one regulator for 603e or 603eV

Version V3	3/6/96
Sheet 6	Add OR gate to PCI Grant and Request signals
	Remove support for 3rd PCI slot
Sheet 7	Add Comm slot detect and snoop enable bit to O'Hare
Sheet 9	Add 100k pullup to DS8925's +ve differential input
Sheet 15	Change all series term res from 33 to 51
Sheet 16	Add pull up to PMW signals and change EMI caps smaller
Sheet 18	Change PSX pullup and pulldown to 10k
	Add resistor enable snooping
Sheet 20	Remove TL082A replace with TLE2062 (higher drive)
Sheet 11	No connection for VREF of LS1176

Version V4	4/9/96
Sheet 15-25	Resequence sheets
Sheet 2,18	Support for Sirocco
	Add parallel term res to uP clk
Sheet 6	Add RC parallel term to comm and PCI slot clk
Sheet 8	Add option to connect dotclk from Athens to ATI264
	Add RC filter to the II2C bus clk input of Athens
Sheet 9	Use F125 to buffer SCC clk
Sheet 10	Add series term res to IDE signals
	Use Dallas DS2109 as active SCSI termation
Sheet 11,23	Use ABT244 to buffer sys_reset
Sheet 12	Add parallel term res to L2 cache clk
Sheet 13	Increase CD audio gain by 2
Sheet 14,22	Change sense logic to support Syrah monitor
Sheet 15	Change sound out jack to 4-channel type
Sheet 16	Update the ATI264 connection with ATI's review
Sheet 18	Add pullup for INCADD and pull down for HFL
	Use F125 to tri-state CSYNC*.
	Support ATI's CSYNC* on HSYNC* feature
Sheet 20	Add 5v to 3.3v decoupling caps around L2 cache slot
Sheet 21	Pull up GBL*
	Change pullup and pulldown value of PSX
Sheet 22	Change PMW pullup

Version V3 --> use for pre EVT2	4/26/96
Sheet 16	Enable relocatable IO space for ATI264

Version V4 --> use for EVT2	4/30/96
Sheet 8	Change series term res of Athens from 51 to 33
	Change cap at PCI clk Beruit's XTALi to 33pf

Version V5	5/6/96
Sheet 14,15	Change sense logic to support Syrah using 3-channel jack
Sheet 7	Reroute mic sense to O'Hare
Sheet 11	Add EMI cap to ADB ground

Version V5	5/7/96
Sheet 14	Add NS AWACS as alt to Crystal AWACS

Version V5	5/8/96
Sheet 16	Hard join ATI_DCLK from VI Mach to ATI264

Version V5	5/13/96
Sheet 14	Finalize the sense logic using OR gate
	Use OR gate to buffer the spk off signal from AWACS's P_OUT_1
Sheet 7	Route AMP_OE signal from O'Hare, buffered by OR gate

Version V5	5/29/96
Sheet 13	Add decoupling cap to audio signal from Comm slot

Version V5	6/4/996
Sheet 11	No stuff the decoupling cap at CUDA's reset pin

Version V5	6/5/96
Sheet 14	Use 74HC32 as OR gate for sense logic
Sheet 16,17	Change stuffing option to ATI264GT-B
Sheet 15	Tweak SRS resistor values

Version V5	6/6/96
Sheet 11	Add 0805 pads for ferrite at ADB port
Sheet 3	Change PSX to PSX+

Version V5	6/10/96
Sheet 2	Add series term res to CPU_BR*
Sheet 8	Teak Athens Vdd series res to 3.3
	Tweak series term res of Athens to 33
Sheet 21	Change pullup for PSX to 10k
	Add pull down to L2_TSTCLK
	Add pullup to TT(1), TT(3) and TBST*
	Add 3.3V clamp for EDO sense signal

Version V5	6/11/96
Sheet 7	Disconnect 3.3V pullup for MIC_SENSE

Version V5	6/13/96
Sheet 3	Update PSX+ symbol. Add transistor circuit to TT(0), TT(2) and TT(4)
Sheet 8	No stuff the res that connect II2C bus to foxconn

Version V5	6/20/96
Sheet 20	Remove socket for ATI264
	Change voltage regulator to 2.62V
Sheet 18	Change VI Mach part# to custom ASIC 343s0014
	Remove VI Mach socket
Sheet 22	Change direct connector part# 513-0215 (high current)
Sheet 13	Change -5V series resistor to 5.6ohm
Sheet 21	Stuff resistor to add uP output hold time
Sheet 12	Change part# of 8kx8 SRAM to 333s1068 (100ns part)

Version V5	7/4/96
Sheet 20	Change ground clip part# to 805-1518
Sheet 24	Add ground vias for shielding VI sound signals

Version V5	7/18/96
Sheet 8, 16	Delete DCLK connection from Athens to ATI264
Sheet 13	Add 1k pull down to VID_SND_RET
Sheet 14	Connect AWACS's AGND2 pin directly to AGND
	Connect AWACS's DGND pin to DGND
	Remove components around AWACS that are NO STUFF
Sheet 15	Remove Transistors and resistors that are no longer used by SRS
	Add three EMI cap to chassis gnd for AMP_R, AMP_L and AMP_RET
Sheet 19	Change FCT245 to FCT2245 / ABT245-1 with balanced drive
Sheet 10	Change series res of IDE signals, CSxxFX, DIOR, DIOW to 10
	No stuff AC termination for IDE data lines
Sheet 16	Add caps in parallel with the 75ohms at RGB lines
Sheet 22	No stuff EMI caps for RGB lines near foxconn
Sheet 18	Change stuffing option such that CSYNC is provided by MLB
Sheet 16,22	Replace parallel 75//301 resistors on RGB by 60.4 resistors

Version V5 --> preDVT	7/19/96
Sheet 20	Change sound jack emi clip part# to 805-1264
Sheet 21	No stuff snoop enable resistor

Version V6 --> preEVT3	7/29/96
Sheet 3	Add pull up resistor pads to SYSCLK_PSX
Sheet 21	Pull CUP_ID3 up. Remove pull down
Sheet 22	Add 12V supply for cpu fan
Sheet 14	XOR Mic_Sense & Aud_In_Sense to interrupt AWACS
	Add 100k pull up for INT_SPK_SEL

Version V7 --> EVT3	8/6/96
Sheet 11	Revert stuffing option back to Cuda 2.4

Version V8	8/19/96
Sheet 17	Change geometry for SGRAMs to enlarge pad size
Sheet 3	Change PSX+ symbol. Pin C1 for TT_OE instead of pin A2.
Sheet 20	Replace R339 by short.
	Run separate PROC_PWR trace from regulator for PROC_AVDD
Sheet 8	Change term resistor at SYSCLK_CACHE to 33 (align to cpu clk)
Sheet 15,22	To reduce EMI leakage from RGB signals, stuff 75ohm with 100pf near ATI264 and stuff 301ohm with 12pf near foxconn
Sheet 2	Run 3.3V directly to processor IO power
Sheet 20	Change five 2.2uF caps for processor core power to 4.7uF
Sheet 11	Add resistor (stuffing option) to route or unroute ADB signal to foxconn
Sheet 6	No stuff 33pf caps for PCI clk
Sheet 17	No stuff pull down resistor for EPROM's chip enable

Version V8 --> preDVT2	8/23/96
Sheet 3,8,21	Change stuffings for PSX+

Version V9 --> DVT	9/10/96
Sheet 15	Change R connecting sound out shield to MLB shield from 47 to 10
Sheet 16	Change term R for MMCLK from 51 to 0 (reduce skew)
Sheet 17	No stuff resistor connecting to A15/VPP of ATI EPROM
Sheet 22	Change EMI cap for BOXID0 from 0.001uF to 0.1uF (improve video)
Sheet 2	No stuff 0.01uF caps connecting 5V and cpu IO power (3.3V)
All Sheets	Resequence reference designators
Sheet 12	Add 333S1192 (70ns) as alt part for SRAM
Sheet 8	Change 33.33 and 31.3344MHz crystals to 3rd overtone part #.
Sheet 3	Change seris term res for TT0,2,4 signals from 51 to 0
Sheet 2,21	Remove resistors stuffings for 604
Sheet 3	Change pull down transistors for TT0,2,4 signals to MOSFET 2N7002
Sheet 22	Change EMI caps for RGB lines from 12pf to 10pf

Version V10 --> rev B proto	10/10/96
Sheet 20	Add 100k pull up for RAS and CAS signals
	Add associate part for heatsink with fan
	No stuff gnd clip and move heatsinks to higher assembly BOM
Sheet 8	Change trap circuit for 50Mhz Beirut such that 20pf is 7.5pf

Version V11 --> rev B	11/14/96
Sheet 16	Change RSET resistor from 316 to 294
	Change RGB caps from 100pf to 47pf
	Change AVDD caps from 22uF and 0.1uF to 47uF and 0.001uF
Sheet 20	Change part# of EMI sound clip to 805-1618
Sheet 12	Change resistor at FET gate from 1k to 51

Version V12 --> rev C	11/15/96
Sheet 20	Short out resistor routing 5V to 1085 regulator
Sheet 5	Stuff mask ROM
Sheet 21	Stuff resistor to trun on burst mode

Change History

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Version V13 --> rev D	5/16/97
Sheet 12	Pads change to U6 only

Version V14 --> rev E	6/11/97
Sheet 2	Change C339 from 10µF to 100µF low ESR
Sheet 16	Change R363 from 10 to 100 Change C385 0.1µF to 1.0µF Add C449 22µF in parallel to C385
Sheet 20	Change C100 from 100µF to 100µF low ESR Add more vias to the input of regulator

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