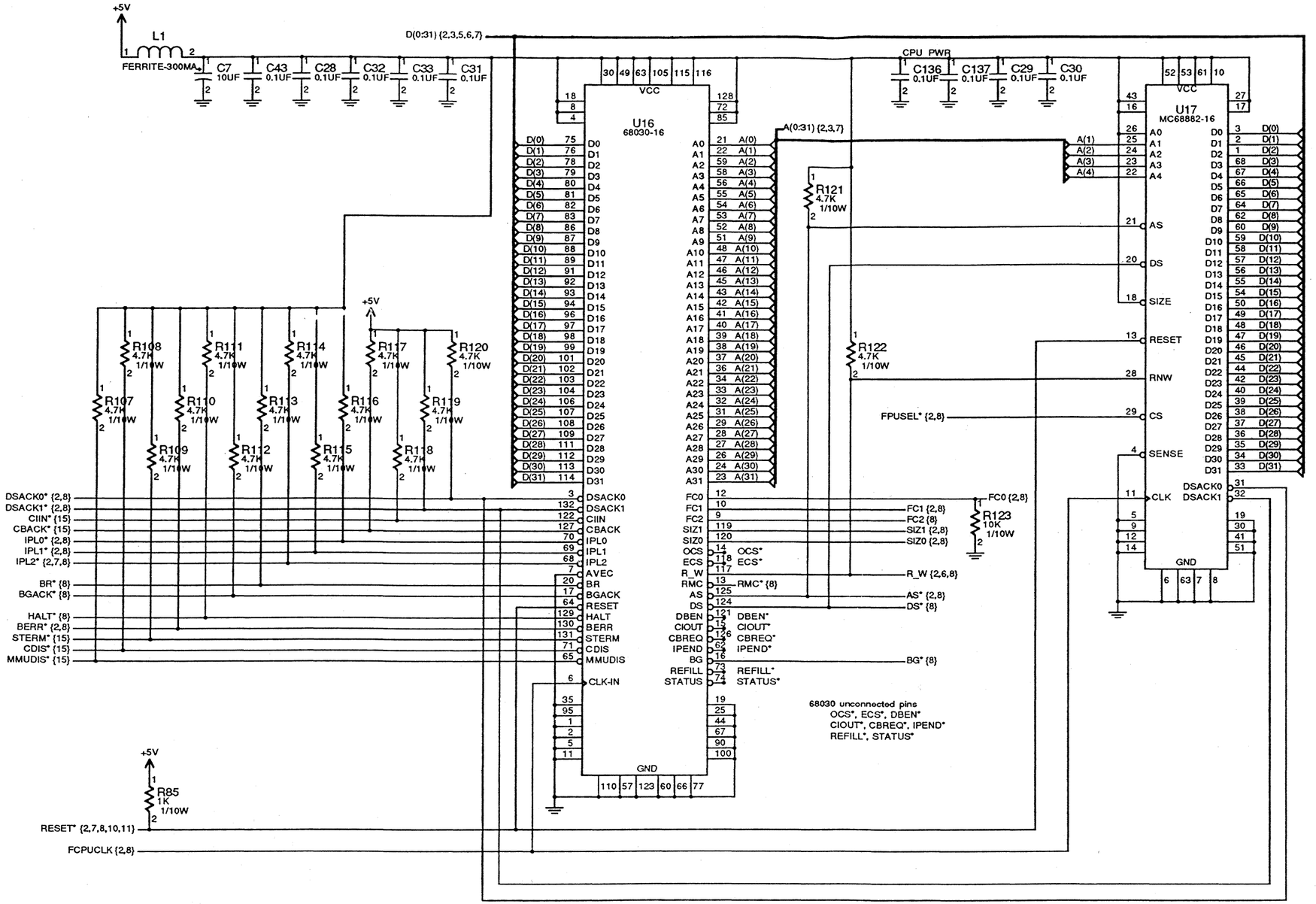
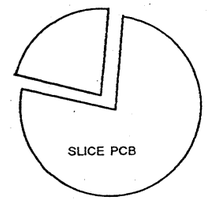
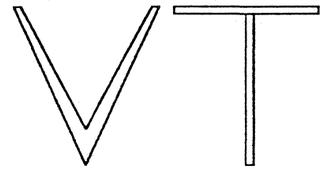
sheet	CONTENTS
1	CPU & FPU
2	System ASIC, clock, RAM buffers
3	ROM & ROM SIMM
4	DRAM & DRAM SIMM
5	VRAM & VRAM SIMM
6	ARIEL
7	Combo & SCSI connector
8	96-pin PDS connector
9	serial ports
10	DFAC II, sound I/O
11	CUDA
12	Foxconn connector
13	revision history (start to EVT)
14	revision history (post-EVT)
15	test points







In FF, DSACK0, DSACK1, IPL[2] pulled up by 1kΩ (instead of 4.7kΩ).

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DIMENSIONS ARE IN MILLIMETERS
X.X± ____
X.XX± ____
X.XXX± ____
ANGLES± ____
DO NOT SCALE DRAWINGS

THIRD ANGLE PROJECTION

METRIC

DRAFTER	/	DESIGN CK	/
ENG APPD	/	MFG APPD	/
QA APPD	/	DESIGNER	/
RELEASE	/	SCALE	

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer, Inc

TITLE
CPU & FPU

Zenon Kuc, x2-5086

SLICEV301

October 6, 1992

This space for rent.

DRAWING NUMBER

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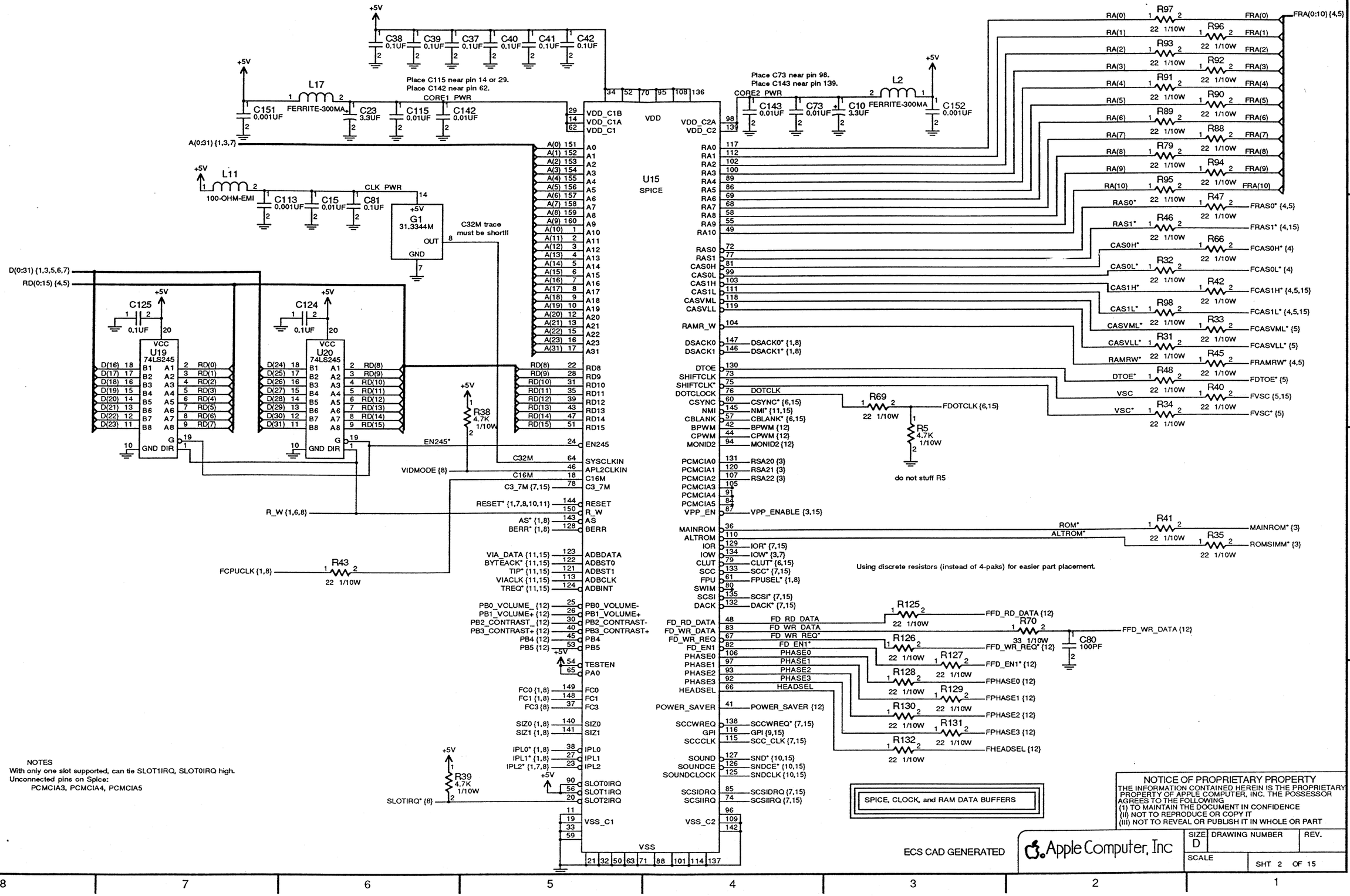
SHT 1 OF 15


+5V
C38 0.1UF
C39 0.1UF
C37 0.1UF
C40 0.1UF
C41 0.1UF
C42 0.1UF
L17
FERRITE-300MA
C151 0.001UF
C23 3.3UF
C115 0.01UF
C142 0.01UF
Place C115 near pin 14 or 29.
Place C142 near pin 62.
CORE1 PWR
34 52 70 95 108 136
VDD_C1B
VDD_C1A
VDD_C1
VDD
A(0:31) {1,3,7}
L11
100-OHM-EMI
C113 0.001UF
C15 0.01UF
C81 0.1UF
CLK PWR
G1
31.3344M
OUT
GND
C32M trace must be short!!
U15
SPICE
D(0:31) {1,3,5,6,7}
RD(0:15) {4,5}
C125 0.1UF
C124 0.1UF
U19
U20
74LS245
VCC
GND DIR
R38 4.7K 1/10W
EN245*
C32M
VIDMODE {8}
C16M
C3_7M {7,15}
RESET* {1,7,8,10,11}
R_W {1,6,8}
AS* {1,8}
BERR* {1,8}
FCPUCLK {1,8}
R43 22 1/10W
VIA_DATA {11,15}
BYTEACK* {11,15}
TIP* {11,15}
VIACLK {11,15}
TREQ* {11,15}
PB0_VOLUME_ {12}
PB1_VOLUME+ {12}
PB2_CONTRAST_ {12}
PB3_CONTRAST+ {12}
PB4 {12}
PB5 {12}
TESTEN
PA0
FC0 {1,8}
FC1 {1,8}
FC3 {8}
SIZ0 {1,8}
SIZ1 {1,8}
IPL0* {1,8}
IPL1* {1,8}
IPL2* {1,7,8}
R39 4.7K 1/10W
SLOTIRQ* {8}
SLOT0IRQ
SLOT1IRQ
SLOT2IRQ
SYSCLKIN
APL2CLKIN
C16M
C3_7M
RESET
R_W
AS
BERR
ADBDATA
ADBST0
ADBST1
ADBCLK
ADBINT
PB0_VOLUME-
PB1_VOLUME+
PB2_CONTRAST-
PB3_CONTRAST+
PB4
PB5
VSS_C1
VSS_C2
VSS
Place C73 near pin 98.
Place C143 near pin 139.
CORE2 PWR
L2
C143 0.01UF
C73 0.01UF
C10 3.3UF
C152 0.001UF
VDD_C2A
VDD_C2
RA0
RA1
RA2
RA3
RA4
RA5
RA6
RA7
RA8
RA9
RA10
RAS0
RAS1
CAS0H
CAS0L
CAS1H
CAS1L
CASVML
CASVLL
RAMR_W
DSACK0
DSACK1
DTOE
SHIFTCLK
SHIFTCLK*
DOTCLOCK
CSYNC
NMI
CBLANK
BPWM
CPWM
MONID2
PCMCIA0
PCMCIA1
PCMCIA2
PCMCIA3
PCMCIA4
PCMCIA5
VPP_EN
MAINROM
ALTROM
IOR
IOW
CLUT
SCC
FPU
SWIM
SCSI
DACK
FD_RD_DATA
FD_WR_DATA
FD_WR_REQ
FD_EN1
PHASE0
PHASE1
PHASE2
PHASE3
HEADSEL
POWER_SAVER
SCCWREQ
GPI
SCCCLK
SOUND
SOUNDCE
SOUNDCLOCK
SCSIDRQ
SCSIIRQ
R97 22 1/10W
R96 22 1/10W
R93 22 1/10W
R92 22 1/10W
R91 22 1/10W
R90 22 1/10W
R89 22 1/10W
R88 22 1/10W
R79 22 1/10W
R94 22 1/10W
R95 22 1/10W
R47 22 1/10W
R46 22 1/10W
R66 22 1/10W
R32 22 1/10W
R42 22 1/10W
R98 22 1/10W
R33 22 1/10W
R31 22 1/10W
R45 22 1/10W
R48 22 1/10W
R40 22 1/10W
R34 22 1/10W
FRA(0:10) {4,5}
FRAS0* {4,5}
FRAS1* {4,15}
FCAS0H* {4}
FCAS0L* {4}
FCAS1H* {4,5,15}
FCAS1L* {4,5,15}
FCASVML* {5}
FCASVLL* {5}
FRAMRW* {4,5}
FDTOE* {5}
FVSC {5,15}
FVSC* {5}
R69 22 1/10W
FDOTCLK {6,15}
R5 4.7K 1/10W
do not stuff R5
R41 22 1/10W
R35 22 1/10W
MAINROM* {3}
ROMSIMM* {3}
Using discrete resistors (instead of 4-paks) for easier part placement.
R125 22 1/10W
R70 33 1/10W
C80 100PF
R126 22 1/10W
R127 22 1/10W
R128 22 1/10W
R129 22 1/10W
R130 22 1/10W
R131 22 1/10W
R132 22 1/10W
FFD_RD_DATA {12}
FFD_WR_DATA {12}
FFD_WR_REQ* {12}
FFD_EN1* {12}
FPHASE0 {12}
FPHASE1 {12}
FPHASE2 {12}
FPHASE3 {12}
FHEADSEL {12}
SPICE, CLOCK, and RAM DATA BUFFERS
NOTES
With only one slot supported, can tie SLOT1IRQ, SLOT0IRQ high.
Unconnected pins on Spice:
PCMCIA3, PCMCIA4, PCMCIA5
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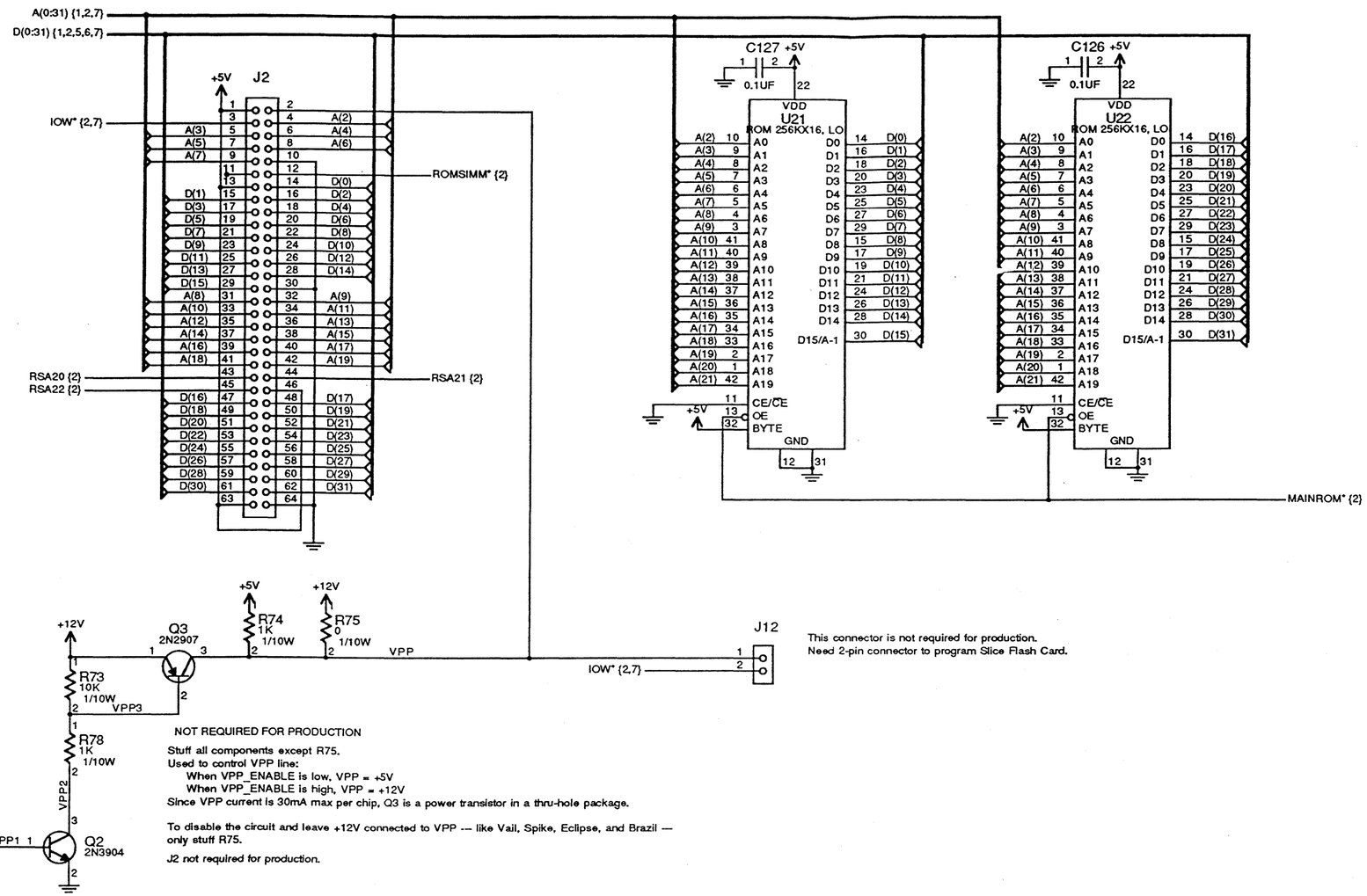

This connector is not required for production.
Need 2-pin connector to program Slice Flash Card.

NOT REQUIRED FOR PRODUCTION

Stuff all components except R75.
Used to control VPP line:
When VPP_ENABLE is low, VPP = +5V
When VPP_ENABLE is high, VPP = +12V
Since VPP current is 30mA max per chip, Q3 is a power transistor in a thru-hole package.

To disable the circuit and leave +12V connected to VPP -- like Vail, Spike, Eclipse, and Brazil -- only stuff R75.

J2 not required for production.

ROM and ROM SIMM

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RD(0:15) {2,5}
FRA(0:10) {2,5}
FRAMRW* {2,5}
FRAS1* {2,15}
FCAS0L* {2}
FCAS0H* {2}
FCAS1L* {2,5,15}
FCAS1H* {2,5,15}
FRAS0* {2,5}

C128 +5V — 0.1UF — U23 DRAM-1MX4: FRA(0:9) → A0–A9; WE; RAS; CE; CAS; VSS; VCC; IO1 → RD(0); IO2 → RD(1); IO3 → RD(2); IO4 → RD(3)

C129 +5V — 0.1UF — U24 DRAM-1MX4: FRA(0:9) → A0–A9; WE; RAS; CE; CAS; VSS; VCC; IO1 → RD(4); IO2 → RD(5); IO3 → RD(6); IO4 → RD(7)

C130 +5V — 0.1UF — U25 DRAM-1MX4: FRA(0:9) → A0–A9; WE; RAS; CE; CAS; VSS; VCC; IO1 → RD(8); IO2 → RD(9); IO3 → RD(10); IO4 → RD(11)

C131 +5V — 0.1UF — U26 DRAM-1MX4: FRA(0:9) → A0–A9; WE; RAS; CE; CAS; VSS; VCC; IO1 → RD(12); IO2 → RD(13); IO3 → RD(14); IO4 → RD(15)

C134 +5V — 0.1UF — U30 DRAM-1MX4: FRA(0:9) → A0–A9; WE; RAS; CE; CAS; VSS; VCC; IO1 → RD(0); IO2 → RD(1); IO3 → RD(2); IO4 → RD(3)

C132 +5V — 0.1UF — U27 DRAM-1MX4: FRA(0:9) → A0–A9; WE; RAS; CE; CAS; VSS; VCC; IO1 → RD(4); IO2 → RD(5); IO3 → RD(6); IO4 → RD(7)

C135 +5V — 0.1UF — U28 DRAM-1MX4: FRA(0:9) → A0–A9; WE; RAS; CE; CAS; VSS; VCC; IO1 → RD(8); IO2 → RD(9); IO3 → RD(10); IO4 → RD(11)

C133 +5V — 0.1UF — U29 DRAM-1MX4: FRA(0:9) → A0–A9; WE; RAS; CE; CAS; VSS; VCC; IO1 → RD(12); IO2 → RD(13); IO3 → RD(14); IO4 → RD(15)

J1 — DRAM SIMM: +5V; RD(0:15); FRA(0:10)

DRAM SIMM connector is a thru-hole part, saves $0.37

DRAM & DRAM SIMMs

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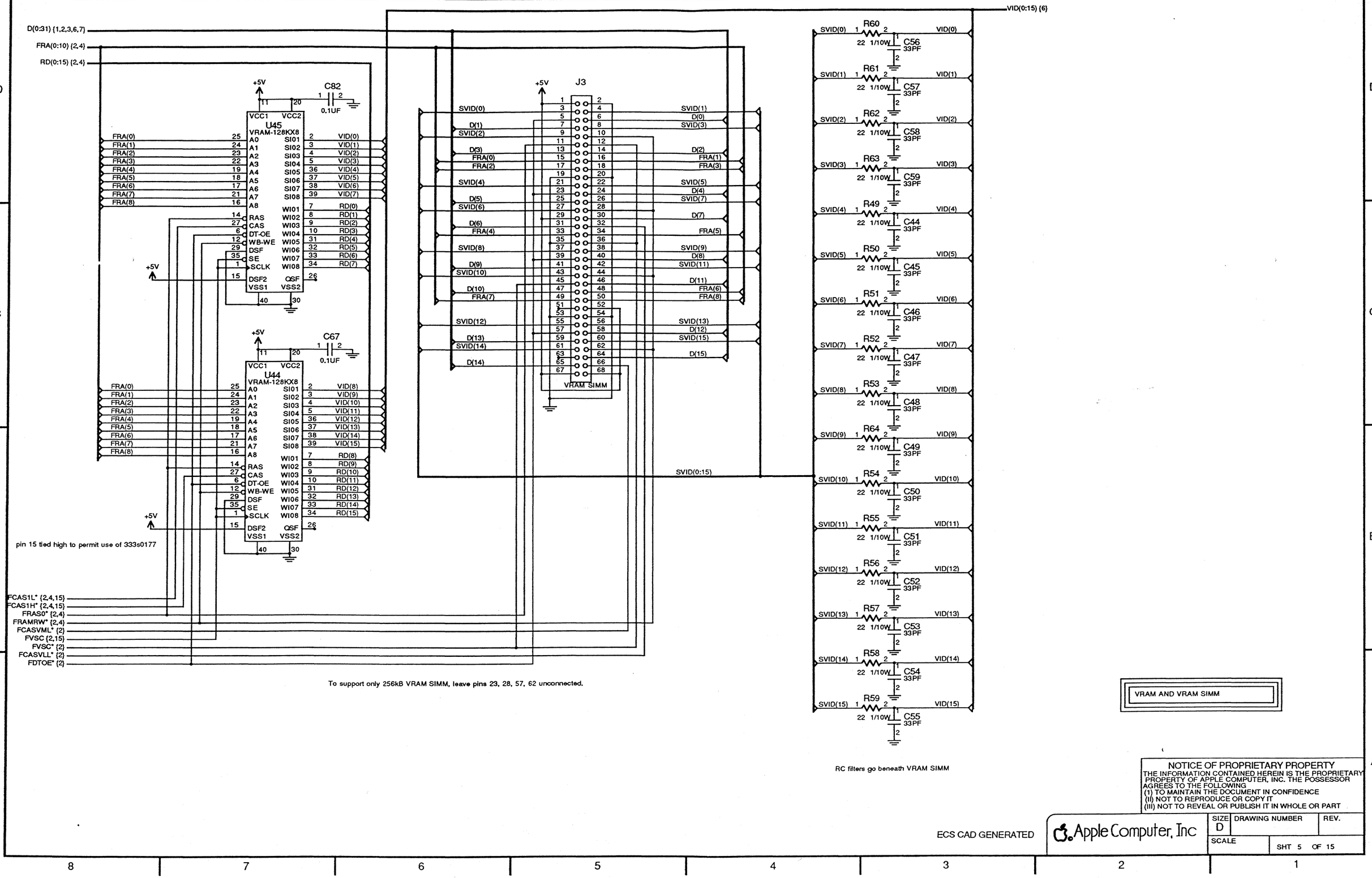
D(0:31) {1,2,3,6,7}
FRA(0:10) {2,4}
RD(0:15) {2,4}
+5V
C82
0.1UF
U45
VRAM-128KX8
VCC1 VCC2
A0 A1 A2 A3 A4 A5 A6 A7 A8
SI01 SI02 SI03 SI04 SI05 SI06 SI07 SI08
WI01 WI02 WI03 WI04 WI05 WI06 WI07 WI08
RAS CAS DT-OE WB-WE DSF SE SCLK
DSF2 QSF VSS1 VSS2
FRA(0) FRA(1) FRA(2) FRA(3) FRA(4) FRA(5) FRA(6) FRA(7) FRA(8)
VID(0) VID(1) VID(2) VID(3) VID(4) VID(5) VID(6) VID(7)
RD(0) RD(1) RD(2) RD(3) RD(4) RD(5) RD(6) RD(7)
C67
U44
VID(8) VID(9) VID(10) VID(11) VID(12) VID(13) VID(14) VID(15)
RD(8) RD(9) RD(10) RD(11) RD(12) RD(13) RD(14) RD(15)
pin 15 tied high to permit use of 333s0177
J3
VRAM SIMM
SVID(0) SVID(1) SVID(2) SVID(3) SVID(4) SVID(5) SVID(6) SVID(7) SVID(8) SVID(9) SVID(10) SVID(11) SVID(12) SVID(13) SVID(14) SVID(15)
D(0) D(1) D(2) D(3) D(4) D(5) D(6) D(7) D(8) D(9) D(10) D(11) D(12) D(13) D(14) D(15)
FRA(0) FRA(1) FRA(2) FRA(3) FRA(4) FRA(5) FRA(6) FRA(7) FRA(8)
SVID(0:15)
VID(0:15) {6}
R60 R61 R62 R63 R49 R50 R51 R52 R53 R54 R55 R56 R57 R58 R59 R64
22 1/10W
C56 C57 C58 C59 C44 C45 C46 C47 C48 C49 C50 C51 C52 C53 C54 C55
33PF
FCAS1L* {2,4,15}
FCAS1H* {2,4,15}
FRAS0* {2,4}
FRAMRW* {2,4}
FCASVML* {2}
FVSC {2,15}
FVSC* {2}
FCASVLL* {2}
FDTOE* {2}
To support only 256kB VRAM SIMM, leave pins 23, 28, 57, 62 unconnected.
RC filters go beneath VRAM SIMM
VRAM AND VRAM SIMM
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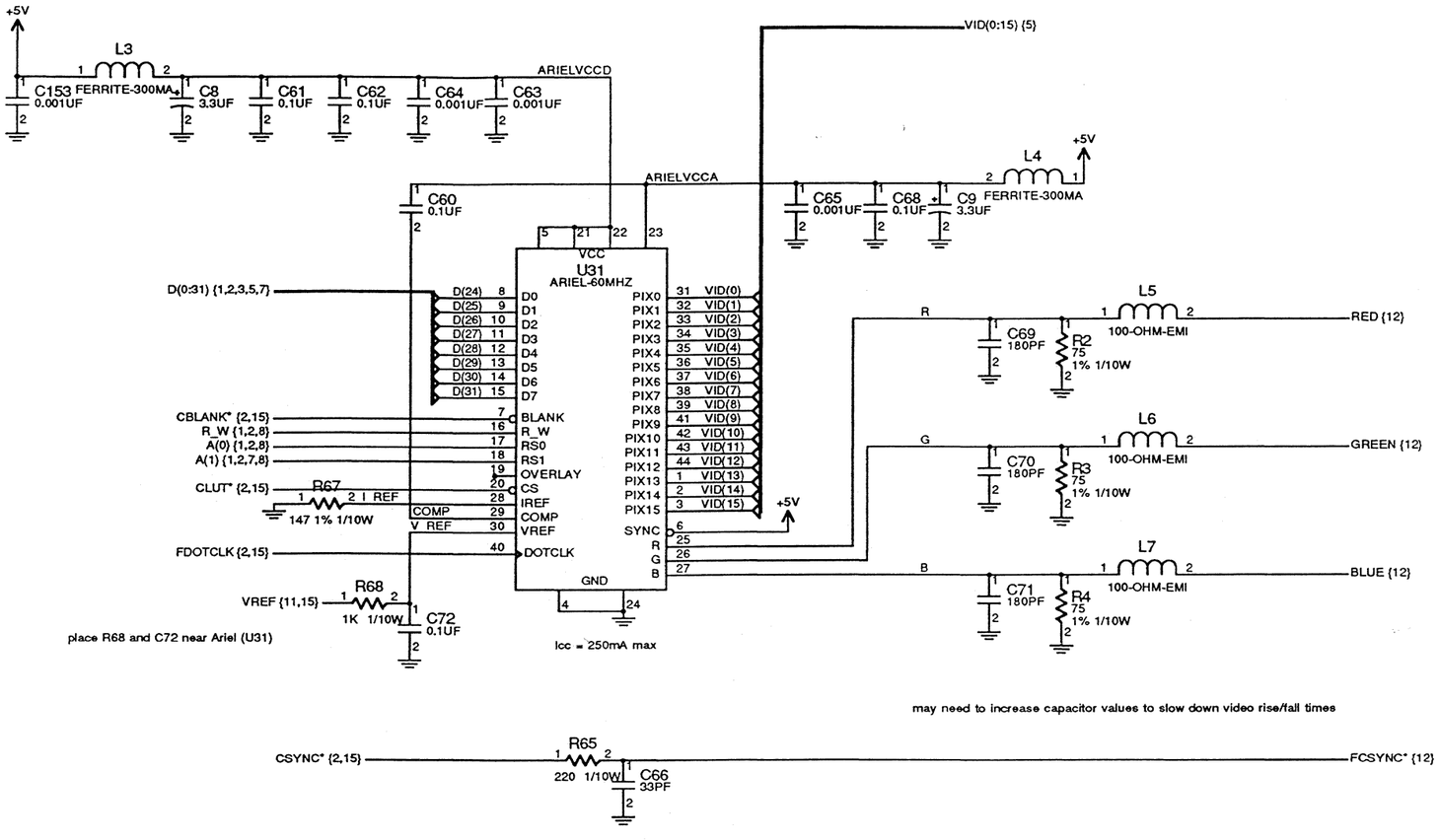

ARIEL

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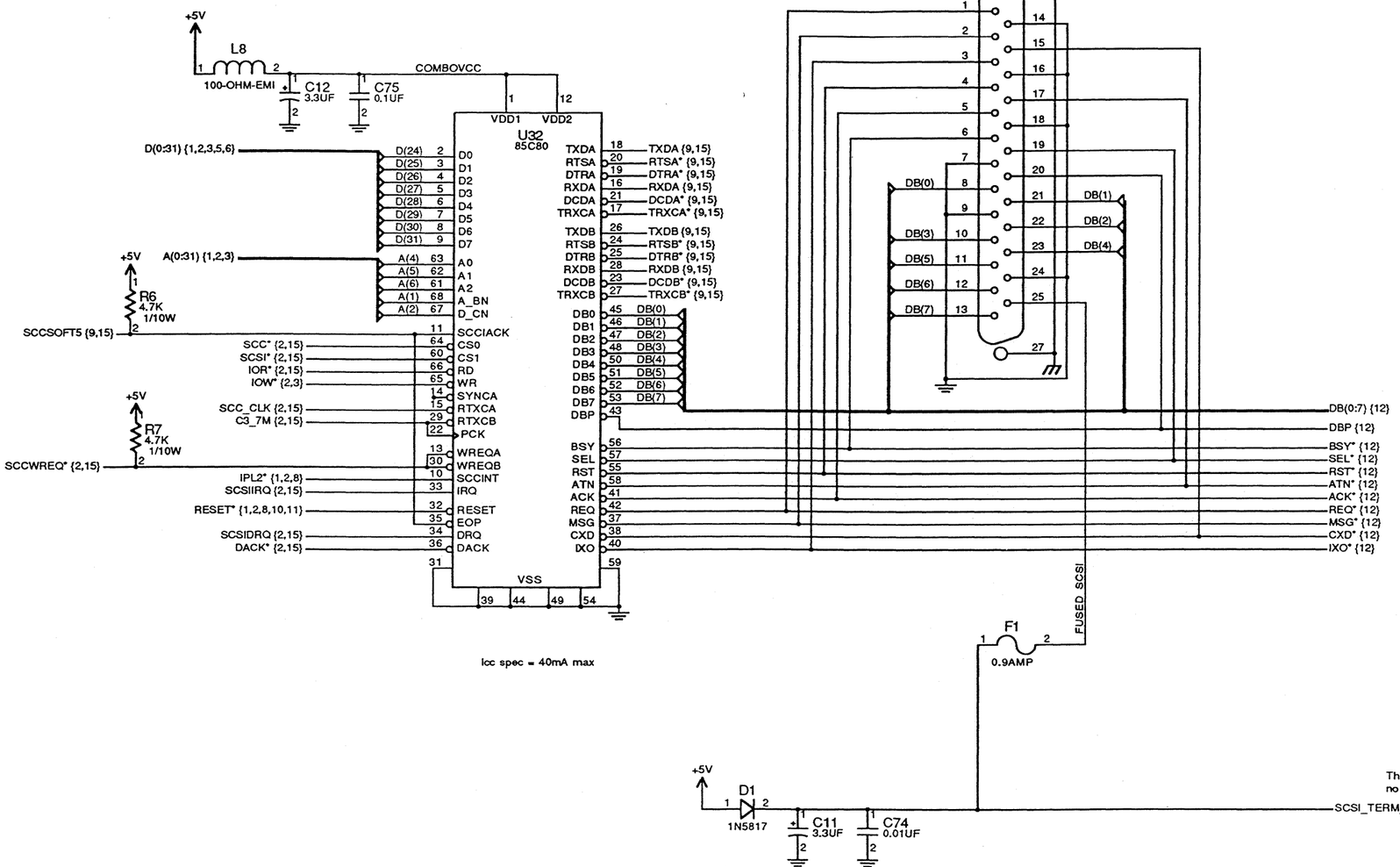

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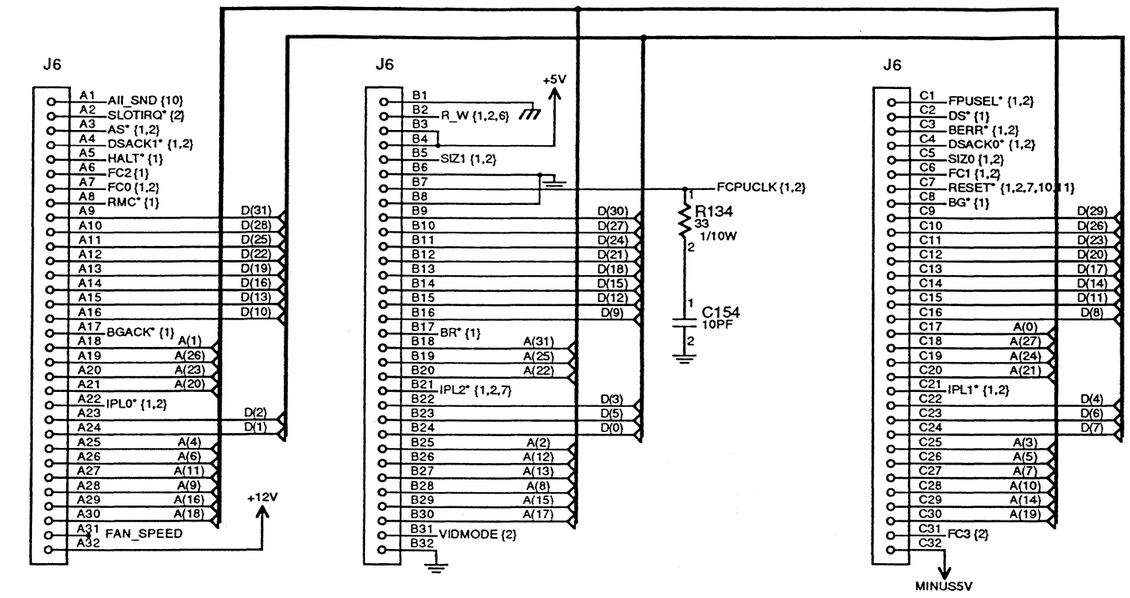

FAN_SPEED is only unconnected net.

LC-COMPATIBLE PDS CONNECTOR

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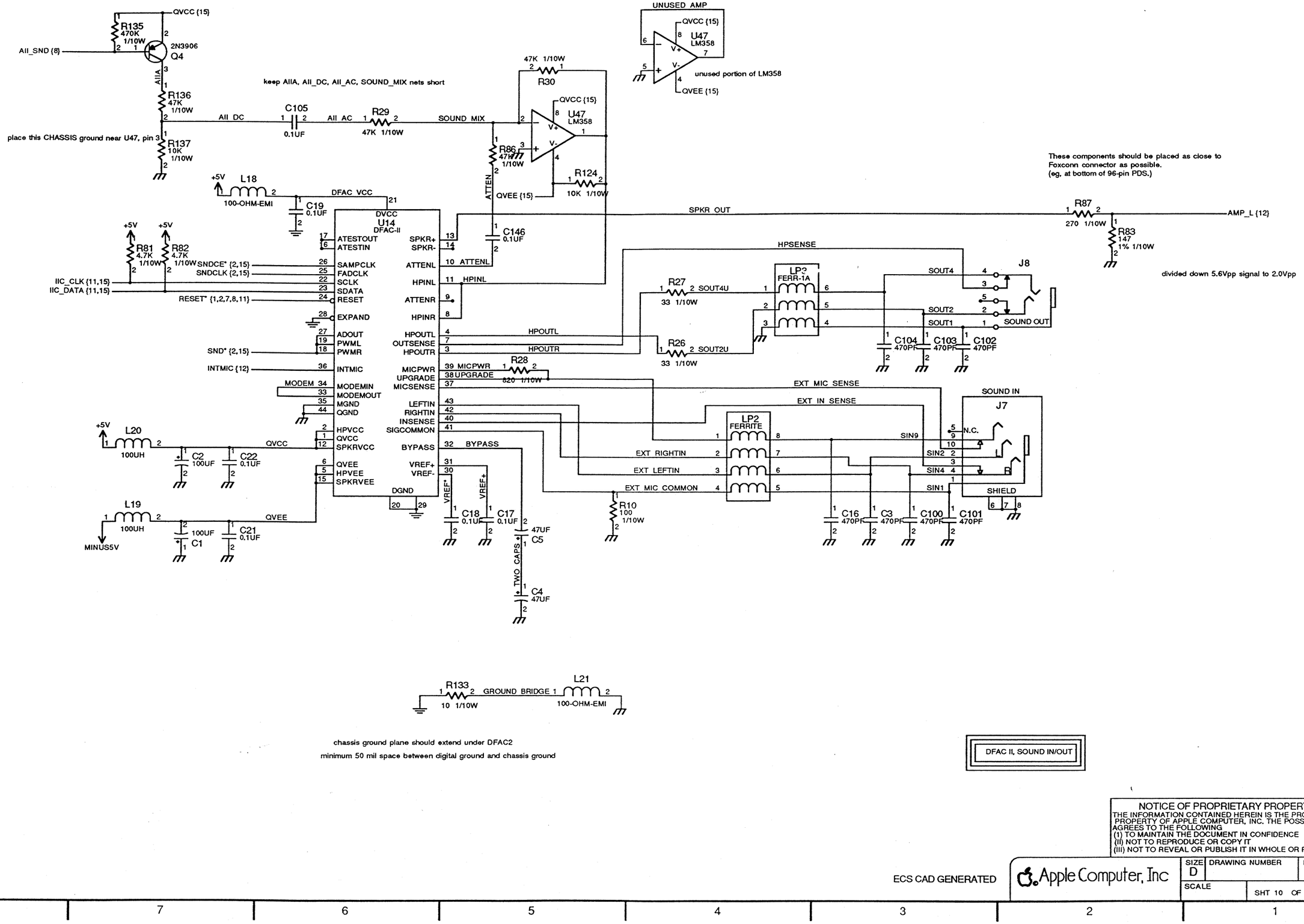

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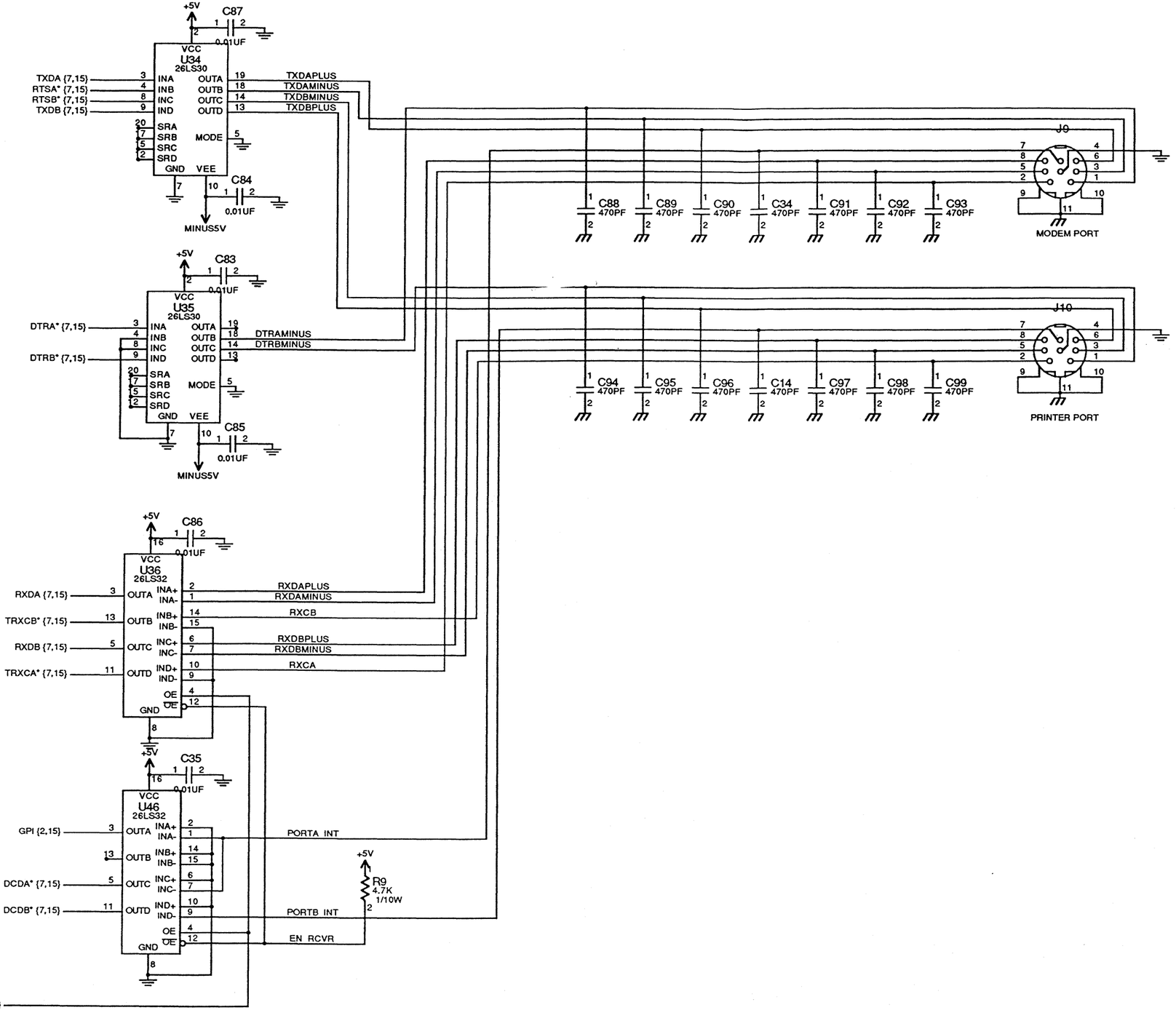
SCALE	SHT 10 OF 15	



SCC TRANSCEIVERS, MODEM PORT, PRINTER PORT

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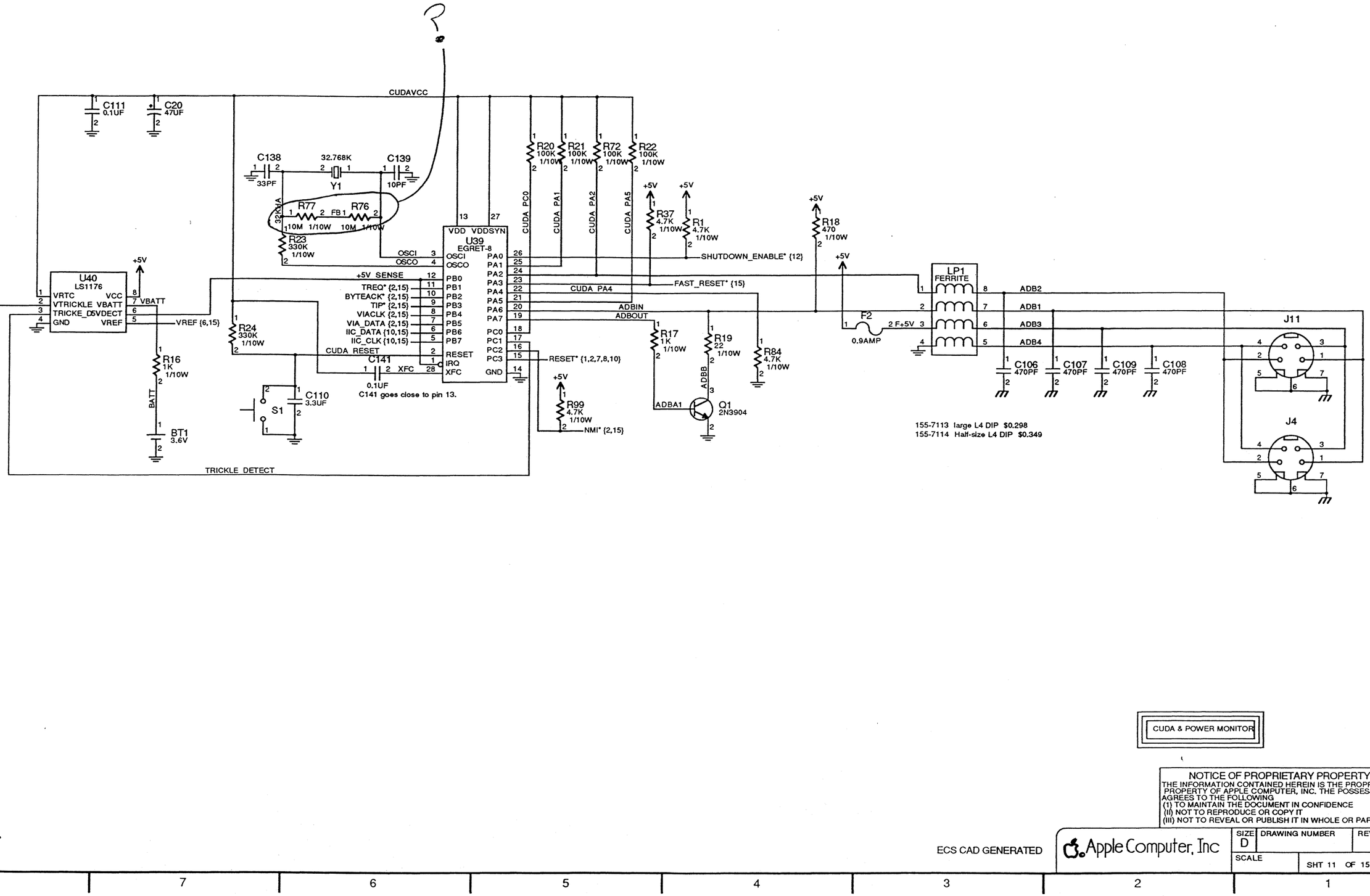
D		
SCALE	SHT 9 OF 15	



CUDA & POWER MONITOR

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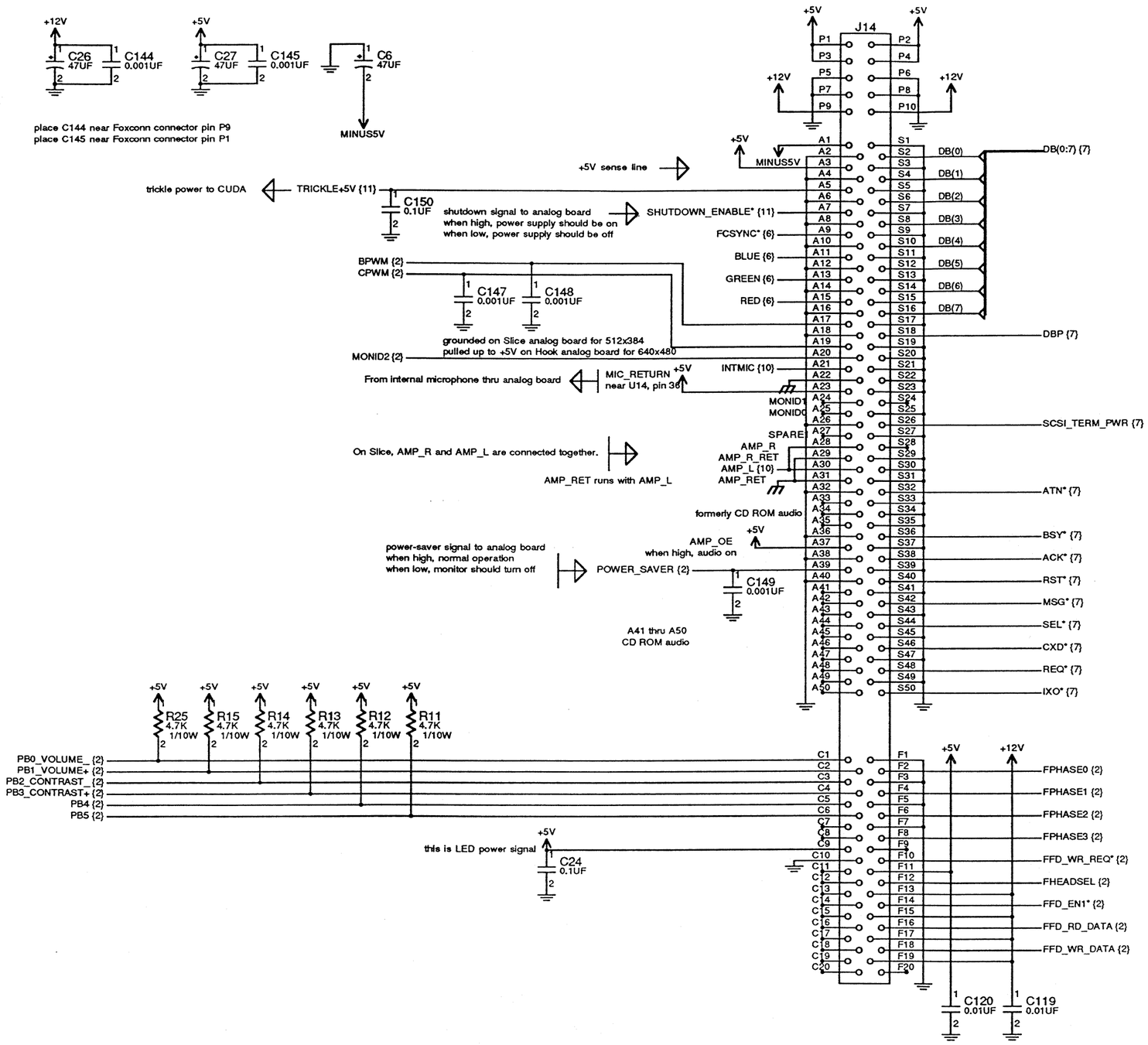

FOXCONN CONNECTOR

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D		
SCALE	SHT 12 OF 15	

REVISION HISTORY

Version 0.1 — deltas from Foster Farms schematic
March 16, 1992

sheet 1	5 0.1µF caps on 68030 (was 2 0.1µF, 2 0.01µF, 300pF caps) 2 0.1µF caps on FPU (was no caps) DSACK0, DSACK1, and IPL2 pulled up by 4.7kΩ (was 1kΩ)
sheet 2	0.1µF caps on LS245s (was 0.01µF) No VGA clock support (was separate VGA clock) Support for only 1 slot (was three slots)
sheet 3	two x16 ROMs (was four x8 ROMs) ROM SIMM added PLD added for Flash ROM support
sheet 4	0.1µF caps on each DRAM (was 0.1µF and 0.01µF)
sheet 6	eliminated video out support (was DB-25 connector)
sheet 7	eliminated 50-pin HD connector eliminated 4-pin SCSI connector
sheet 8	eliminated 20-pin floppy connector
sheet 12	using CUDA (was Egret)
sheet 15	added FoxConn symbol: SCSI, floppy, analog, power connectors

Version 0.2 — deltas from version 0.1
April 3, 1992

all	using 0805 packages for discrete Rs and Cs (was 1206)
sheet 2	22Ω discrete resistors used (was RPAKs) 22Ω resistors placed near system ASIC (was on various pages) added notes on placement of C73, C115 eliminated R42 on TESTEN* pin (was 0Ω) eliminated labels on unused pins fixed C15 (was wrong symbol, wrong value) connected MONID2 so ASIC can detect 512 vs 640 resolution grounded MONID0 (was floating)
sheet 4	22Ω resistors moved to sheet 2 DRAM SIMM moved from sheet 5
sheet 5	22Ω resistors moved to sheet 2 256kB VRAM added
sheet 6	filtered VSYNC signal removed 12-pin video overlay connector removed video RC filters moved to sheet 5
sheet 7	added 1A fuse on external SCSI connector
sheet 8	using SWIM2 (was SWIM) — no schematic change required
sheet 10	added second 75175 for GPI support on serial ports will try to eliminate RC paks
sheet 11	changed C17, C18 to 3.3µF (was 10µF)
sheet 12	added 1A fuse on ADB port eliminated C140 on U40 (was 0.1µF) hooked up CUDA for soft-power added note on placement of C141 second ADB port added
sheet 13	eliminated Q2, R32, R79, since no internal CD-ROM drive changed C142, C3, and C1 to 3.3µF (was 10µF)
sheet 14	changed C24, C25, C122 to 3.3µF (was 10µF)
sheet 15	added lots of comments A20 connected to MONID2 (was called RES640) A25 renamed SPARE_1 (was RESERVED) A27–A30 renamed to AMP.... (was SPKR....) A31 and A37 named SPARE_2 and SPARE_3 A39 named POWER_SAVER

Version 0.2b — deltas from version 0.2 schematic
April 8, 1992

sheet 11	consolidated sheets 11, 13, & 14 into one sheet eliminated DFAC, added DFAC II

Version 0.3b — deltas from version 0.2b schematic
April 12, 1992

sheet 2	eliminated V8.3, added Spice system ASIC added 22Ω resistors to four new pins: CASVML*, CASVLL*, VSC*, ALTROM*
sheet 3	eliminated ROM SIMM PAL
sheet 5	fixed CAS connections to VRAM banks
sheet 8	fixed FD_WR_DATA connection to SWIM2
sheet 11	specified R and C values on sheet
sheet 12	added pull-up resistor to SHUTDOWN_ENABLE* line
sheet 13	added push-button interface

Version 0.4b — deltas from version 0.3b schematic
April 16, 1992

sheet 2	pinned out Spice, adding extra VSS
sheet 3	three-pin jumper added for on-board Flash ROM support connected FLASH_WE* to IOW* on Spice
sheet 11	added 4-conductor stereo-in jack (was 3-conductor jack) added L 3-pak and L 4-pak (was discrete inductors) placed back-to-back electrolytic caps on BYPASS pin (was non-polarized cap) added 4.7kΩ pull-up to SND* (sound PWM) AC-coupled speaker output from DFAC II
sheet 13	moved push-button interface to A[41:50] (was C[1:10])

Version 0.5b — deltas from version 0.4b schematic
April 28, 1992

sheet 2	changed clock oscillator to plastic surface-mount (was full-size metal can) added inductor and caps to ground pin on clock oscillator added resistor and capacitor to C32M line updated Spice symbol
sheet 3	changed J12 to two-pin jumper (was three-pin jumper)
sheet 4	changed DRAM SIMM to 0.3" row spacing (was 0.4")
sheet 12	changed R21 connection to CUDAVCC (was +5V) added pull-up resistor to CUDA_PA2 line changed switch part number

Version 0.6b — deltas from version 0.5b schematic
April 28, 1992

sheet 2	removed inductor and caps to ground pin on clock oscillator removed resistor and capacitor on C32M line added ~0.001µF capacitor to CLK_PWR line updated Spice symbol

Version 0.7b — deltas from version 0.6b schematic
April 30, 1992

sheet 3	added superfluous VPP_ENABLE circuitry
sheet 9	changed pin B1 on PDS to DFAC_GND (was CHASSIS)
sheet 11	changed L19 and L20 to new 100µH part (was 82µH)

Version 0.8b — deltas from version 0.7b schematic
May 12, 1992

sheet 2	updated Spice symbol
sheet 11	added 4.7kΩ pull-up resistors to DFAC_DATA and DFAC_CLK lines changed R20, R21, R22 and R72 to 100kΩ pull-ups (was 4.7kΩ)

Version 1.0 — deltas from version 0.8b schematic
May 14, 1992

sheet 2	connected SCC_CLK on Spice to Combo chip (sheet 7) (was C3_7M to all three pins: RTXCA, RTXCB, PCK)
sheet 11	added U47 and associated resistors and capacitors (was All_SND connected to U14, pins 34 and 35; was 2.2µF capacitors between pins 8 & 9, and pins 10 & 11).

——> PRE-EVT PCB <——
Version 1.01 — deltas from version 1.0 schematic
May 15, 1992

sheet 2	need to connect Spice pin 29 to CORE1_PWR
sheet 11	added attenuation resistors R87 and R83 on speaker output signal
sheet 12	added pull-down resistor R84 on CUDA_PA4 net
sheet 13	disconnected All_SND from Foxconn pin A24 disconnected TRICKLE+5V from Foxconn pin A47 disconnected GND from Foxconn pins C1:C20

Version 2.0 — deltas from version 1.01 schematic
May 30, 1992

sheet 2	need to connect Spice pin 29 to CORE1_PWR need to change pin name VSYNC (pin 145) to NMI added net NMI* to pin 145
sheet 5	placed on-board VRAM (U44 and U45) on RD[0:15] bus (was on D[16:31] bus — changed for loading reasons)
sheet 12	connected U39, pin 16 (CUDA PC2) to NMI* (was connected to IPL2* — changed to be able to generate NMI) added pull-up resistor R99 to NMI* net

Version 2.01 — deltas from version 2.0 schematic
June 13, 1992

	updated to ECS version 2.4
sheet 1	updated U16, U17 and RP1
sheet 2	updated U15
sheet 4	updated U23, U24, U25, U26, U27, U28, U29 and U30
sheet 7	changed U32 to 85C80 (was 85C81)
sheet 8	deleted U33 (SWIM2), moved R70, R71, and C80 to page 2 —> ELIMINATED SHEET 8 <— (other sheets move up one)
sheet 10	updated U14, U47, LP2
sheet 11	updated LP1

Version 2.02 — deltas from version 2.01 schematic
June 21, 1992

sheet 2	changed G1 to full-size metal can (was plastic surface mount)
sheet 5, sheet 6	connected on-board VRAMs directly to ARIEL (was through RC filter)
sheet 6	changed L5, L6, L7 to 0805 parts (were 159S0003) changed U31 to Ariel+ (was Ariel)
sheet 7	changed L8 to 0805 part (was 159S0003)
sheet 9	removed L12, L13, L14 removed RC paks from the serial ports replaced U36 and U46 (was 75175, is 26LS32)
sheet 10	added dual surface-mount LPAKs
sheet 12	moved push-buttons back to C1-C10 (was A41-A50) moved AMP_OE to pin A37 (was A27) connected DFAC_GND to pin A31 connected pin A23 to +5V (was MICPWR)

Version 2.03 — deltas from version 2.02 schematic
June 22, 1992

sheet 8	replaced DFAC_GND with CHASSIS
sheet 10	changed L18 to 0805 part (was 159S0003) added 4.7kΩ pull-up resistor to All_SND replaced DFAC_GND with CHASSIS changed resistance values on R83 and R87
sheet 12	replaced DFAC_GND with CHASSIS on microphone (pin A22) replaced DFAC_GND with GND on speaker (pins A29 and A31) eliminated speaker signals to push-button board grounded pin C7 (for Hook PCB in Slice box)

Version 2.04 — deltas from version 2.03 schematic
June 29, 1992

sheet 2	changed L11 to 0805 part (was 159S0003) cleaned up Rs and Cs so that ref. designators and values are readable
sheet 12	replaced GND with CHASSIS on speaker (pins A29 and A31)

Version 2.05 — deltas from version 2.04 schematic
July 10, 1992

sheet 1	connected RMC* to PDS connector (sheet 8)
sheet 2	removed R44 (don't need FSWIMCLK net anymore) removed SWIM* net
sheet 8	connected RMC* to CPU (sheet 1) deleted FANSPD net on pin A31 (added FAN_SPEED label)
sheet 12	deleted unconnected nets to A24, A25, A27, A33-A35, C11-C20

Version 2.06 — deltas from version 2.05 schematic
July 20, 1992

sheet 1	added 15 discrete 0805 4.7kΩ resistors as pull-ups (R107-R121) (removed 16-pin SOIC Rpak RP1)
sheet 3	updated VPP circuit notes
sheet 6	changed C69, C70, C71 to 180pF (was 100pF) to slow down analog video edges
sheet 10	added C114 to far side of voltage divider, deleted C112 (0.22µF) changed R87 to 270Ω (was 390Ω) changed R83 to 150Ω (was 220Ω)
sheet 12	disconnected pin C7 from GND

Version 2.10 — deltas from version 2.06 schematic
July 22, 1992

sheet 1	added 4.7kΩ pull-up resistor (R122) to R_W added 10kΩ pull-down resistor (R123) on FC0 added two 0.1µF capacitors (C136, C137) on U17 (FPU)
sheet 2	deleted R8, BURNIN net on PA0 (U15, pin 65) — now +5V deleted R71 (47Ω) on FFDDWR T-network moved R69 and R5 to sheet 2 from sheet 6 (DOTCLK)
sheet 6	moved R69 and R5 from sheet 6 to sheet 2 (DOTCLK)
sheet 10	changed R103 to 33kΩ (was 4.7kΩ) deleted R36 (was 4.7kΩ pull-up on SND*) added 10kΩ resistor (R124) between op-amp output and QVEE R124 to be stuffed only when U47 is LM358 added unused portion of U47 to schematic deleted C114 (0.1µF capacitor on AMP_L)
	connected HPOUTL to R26 (was R27) connected HPOUTR to R27 (was R26)
	EXT_RIGHTIN connected to LP2 pin 2 (was pin 3) EXT_LEFTIN connected to LP2 pin 3 (was pin 2) SIN2 connected to LP2 pin 6 (was pin 7) SIN4 connected to LP2 pin 7 (was pin 6)
	DFAC_CLK net name changed to IIC_CLK DFAC_DATA net name changed to IIC_DATA
sheet 11	DFAC_CLK net name changed to IIC_CLK DFAC_DATA net name changed to IIC_DATA
	R24 changed to 330kΩ (was 100kΩ) C110 changed to 3.3µF (was 0.1µF)

——> EVT PCB <—— (version 2.2222)
deltas from version 2.10 schematic
August 6, 1992

sheet 1	R107–R116, R121, R122 pulled up to CPU_PWR (was +5V) (change made for more flexible routing)
sheet 10	named 3 nets (MODEM, TWO_CAPS, UNUSED_AMP)
sheet 11	named 4 nets (XFC, VBATT, BATT, CUDA_RESET)
sheet 14	added 156 test points

REVISION HISTORY
page 1

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SIZE	DRAWING NUMBER	REV.
D		
SCALE	SHT 13 OF 15	

Version 3.00 — deltas from version 2.2222 schematic September 24, 1992	
sheet 2	added 0.01µF cap (C142) on CORE1_PWR added 0.01µF cap (C143) on CORE2_PWR disconnected FAST_RESET* line from Spice pin 54 now pulled up to +5V added Apple p/n on Spice — 343S0132 added 22Ω resistors on floppy signals (R125-R132) FFDDWR net name changed to FFD_WR_DATA
sheet 3	added Apple p/n on U21 — 341-0531 added Apple p/n on U22 — 341-0532
sheet 5	updated Apple p/n on VRAM (U44, U45) — 333S0176
sheet 6	changed C66 to 33pF (was 47 pF)
sheet 10	eliminated LP2A, LP3A (dual SMT footprints) changed C4, C5 to 47µF (was 22µF) added Apple p/n on L19, L20 — 152S0041 added CPNR on U47 — CPNR 18676 changed R83 to 147Ω (was 150Ω) added 10Ω resistor (R133) and inductor (L21) between GND and CHASSIS named one net (GROUND_BRIDGE)
sheet 11	updated Apple p/n on CUDA — 341S0417 named one net (F+5V)
sheet 12	added 0.001µF cap (C144) on +12V net added 0.001µF cap (C145) on +5V net added Apple p/n on Foxconn (J14) — 513-0302 added 0.001µF cap (C147) to CPWM net added 0.001µF cap (C148) to BPWM net added 0.001µF cap (C149) to POWER_SAVER net added 0.1µF cap (C150) to TRICKLE+5V net

Version 3.01 — deltas from version 3.00 schematic October 6, 1992	
sheet 2	added 0.001µF cap (C151) on +5V at L17 added 0.001µF cap (C152) on +5V at L2 changed R70 to 33Ω (was 47Ω)
sheet 5	changed C44—C59 to 33pF (was 100pF) connected +5V to pin 15 of U44 and U45 (permits use of 333s0177)
sheet 6	added 0.001µF cap (C153) on +5V at L3
sheet 8	added 33Ω resistor (R134) and 10pF capacitor (C154) on FCPUCLK
sheet 10	deleted R103 (was pull-up on All_SND) added R135, R136, R137, Q4 on All_SND net
sheet 12	disconnected F20 on Foxconn (was +5V)

REVISION HISTORY
page 2

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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT 14 OF 15	

TP1 +5V_SENSE {11}
TP2 ADBA {11}
TP3 ADBB {11}
TP4 ADBOUT {11}
TP5 AII_AC {10}
TP6 ALTROM* {2}
TP7 ARIELVCCA {6}
TP8 ARIELVCCD {6}
TP9 ATTEN {10}
TP10 ATTENL {10}

TP11 B {6}
TP12 BYPASS {10}
TP13 BYTEACK* {2,11}
TP14 C16M {2}
TP15 C3_7M {2,7}
TP16 CAS0H* {2}
TP17 CAS0L* {2}
TP18 CAS1H* {2}
TP19 CAS1L* {2}
TP20 CASVLL* {2}

TP21 CASVML* {2}
TP22 CBACK* {1}
TP23 CBLANK* {2,6}
TP24 CDIS* {1}
TP25 CIIN* {1}
TP26 CLUT* {2,6}
TP27 COMBOVCC {7}
TP28 COMP {6}
TP29 CORE1_PWR {2}
TP30 CORE2_PWR {2}

TP31 CPU_PWR {1}
TP32 CSYNC* {2,6}
TP33 CUDAVCC {11}
TP34 CUDA_PA1 {11}
TP35 CUDA_PA4 {11}
TP36 CUDA_PA5 {11}
TP37 CUDA_PC0 {11}
TP38 DACK* {2,7}
TP39 DCDA* {7,9}
TP40 DCDB* {7,9}

TP41 DFAC_VCC {10}
TP42 DOTCLK {2}
TP43 DTOE* {2}
TP44 DTRA* {7,9}
TP45 DTRAMINUS {9}
TP46 DTRB* {7,9}
TP47 DTRBMINUS {9}
TP48 EN245* {2}
TP49 EN_RCVR {9}
TP50 FAST_RESET* {11}

TP51 FB {11}
TP52 FCAS1H* {2,4,5}
TP53 FCAS1L* {2,4,5}
TP54 FDOTCLK {2,6}
TP55 FD_WR_DATA {2}
TP56 FRAS1* {2,4}
TP57 FVSC {2,5}
TP58 G {6}
TP59 GPI {2,9}
TP60 HPINL {10}

TP61 HPOUTL {10}
TP62 HPOUTR {10}
TP63 IIC_CLK {10,11}
TP64 IIC_DATA {10,11}
TP65 IOR* {2,7}
TP66 I_REF {6}
TP67 MICPWR {10}
TP68 MMUDIS* {1}
TP69 NMI* {2,11}
TP70 XFC {11}

TP71 VBATT {11}
TP72 MODEM {10}
TP73 TWO_CAPS {10}
TP74 UNUSED_AMP {10}
TP75 OSCO {11}
TP76 PORTA_INT {9}
TP77 PORTB_INT {9}
TP78 QVCC {10}
TP79 QVEE {10}
TP80 R {6}

TP81 RA(0) {2}
TP82 RA(1) {2}
TP83 RA(10) {2}
TP84 RA(2) {2}
TP85 RA(3) {2}
TP86 RA(4) {2}
TP87 RA(5) {2}
TP88 RA(6) {2}
TP89 RA(7) {2}
TP90 RA(8) {2}

TP91 RA(9) {2}
TP92 RAMRW* {2}
TP93 RAS0* {2}
TP94 RAS1* {2}
TP95 ROM* {2}
TP96 RTSA* {7,9}
TP97 RTSB* {7,9}
TP98 RXCA {9}
TP99 RXCB {9}
TP100 RXDA {7,9}

TP101 RXDAMINUS {9}
TP102 RXDAPLUS {9}
TP103 RXDB {7,9}
TP104 RXDBMINUS {9}
TP105 RXDBPLUS {9}
TP106 SCC* {2,7}
TP107 SCCSOFT5 {7,9}
TP108 SCCWREQ* {2,7}
TP109 SCC_CLK {2,7}
TP110 SCSI* {2,7}

TP111 SCSIDRQ {2,7}
TP112 SCSIIRQ {2,7}
TP113 SND* {2,10}
TP114 SNDCE* {2,10}
TP115 SNDCLK {2,10}
TP116 SOUND_MIX {10}
TP117 SPKR_OUT {10}
TP118 STERM* {1}
TP119 TIP* {2,11}
TP120 TREQ* {2,11}

TP121 TRICKLE_DETECT {11}
TP122 TRXCA* {7,9}
TP123 TRXCB* {7,9}
TP124 TXDA {7,9}
TP125 TXDAMINUS {9}
TP126 TXDAPLUS {9}
TP127 TXDB {7,9}
TP128 TXDBMINUS {9}
TP129 TXDBPLUS {9}
TP130 VIACLK {2,11}

TP131 VIA_DATA {2,11}
TP132 VID(0) {5,6}
TP133 VID(1) {5,6}
TP134 VID(10) {5,6}
TP135 VID(11) {5,6}
TP136 VID(12) {5,6}
TP137 VID(13) {5,6}
TP138 VID(14) {5,6}
TP139 VID(15) {5,6}
TP140 VID(2) {5,6}

TP141 VID(3) {5,6}
TP142 VID(4) {5,6}
TP143 VID(5) {5,6}
TP144 VID(6) {5,6}
TP145 VID(7) {5,6}
TP146 VID(8) {5,6}
TP147 VID(9) {5,6}
TP148 VPP1 {3}
TP149 VPP2 {3}
TP150 VPP_ENABLE {2,3}

TP151 VREF {6,11}
TP152 VREF* {10}
TP153 VREF+ {10}
TP154 VSC {2}
TP155 VSC* {2}
TP156 V_REF {6}

TEST POINTS

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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT 15 OF 15	