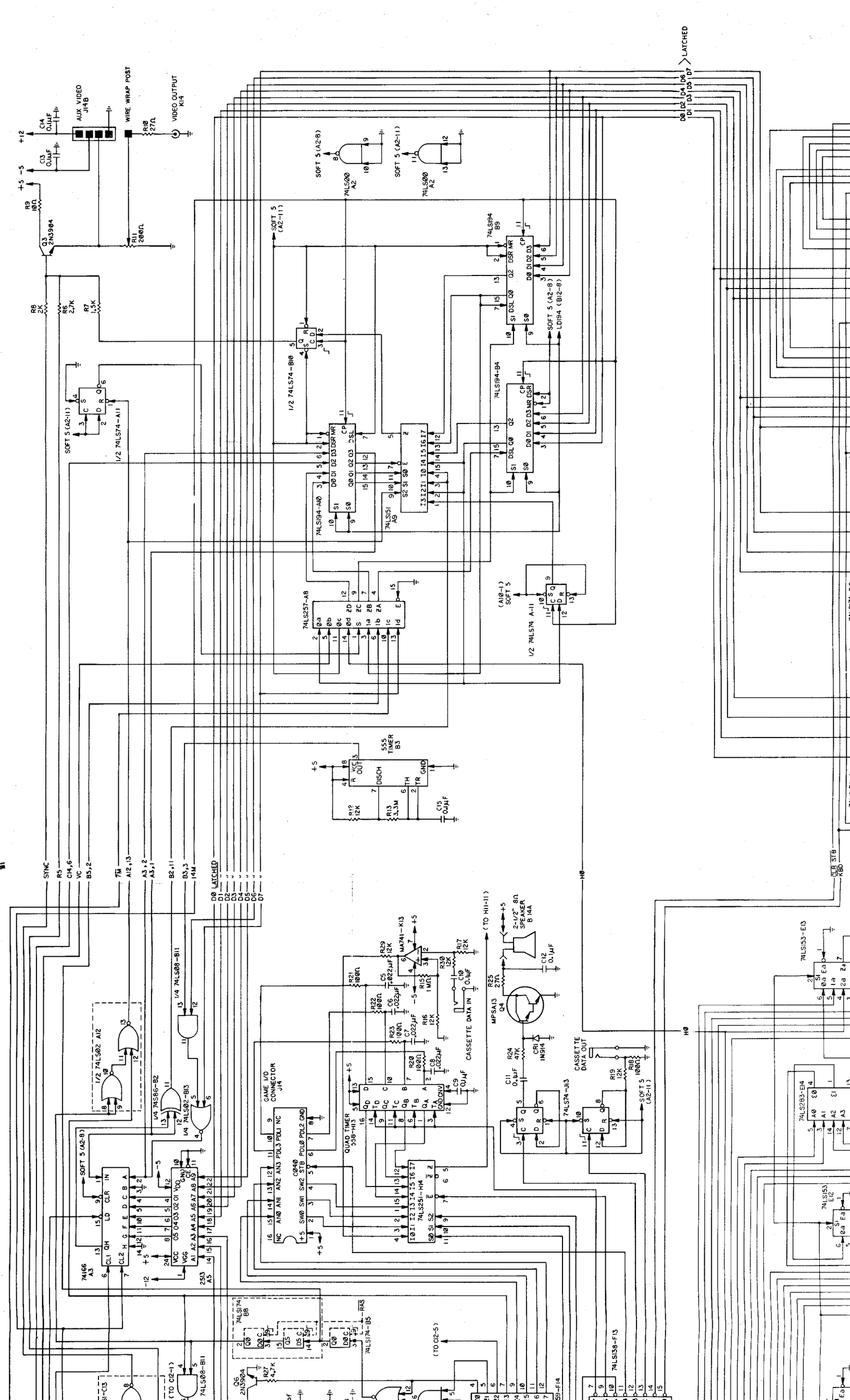
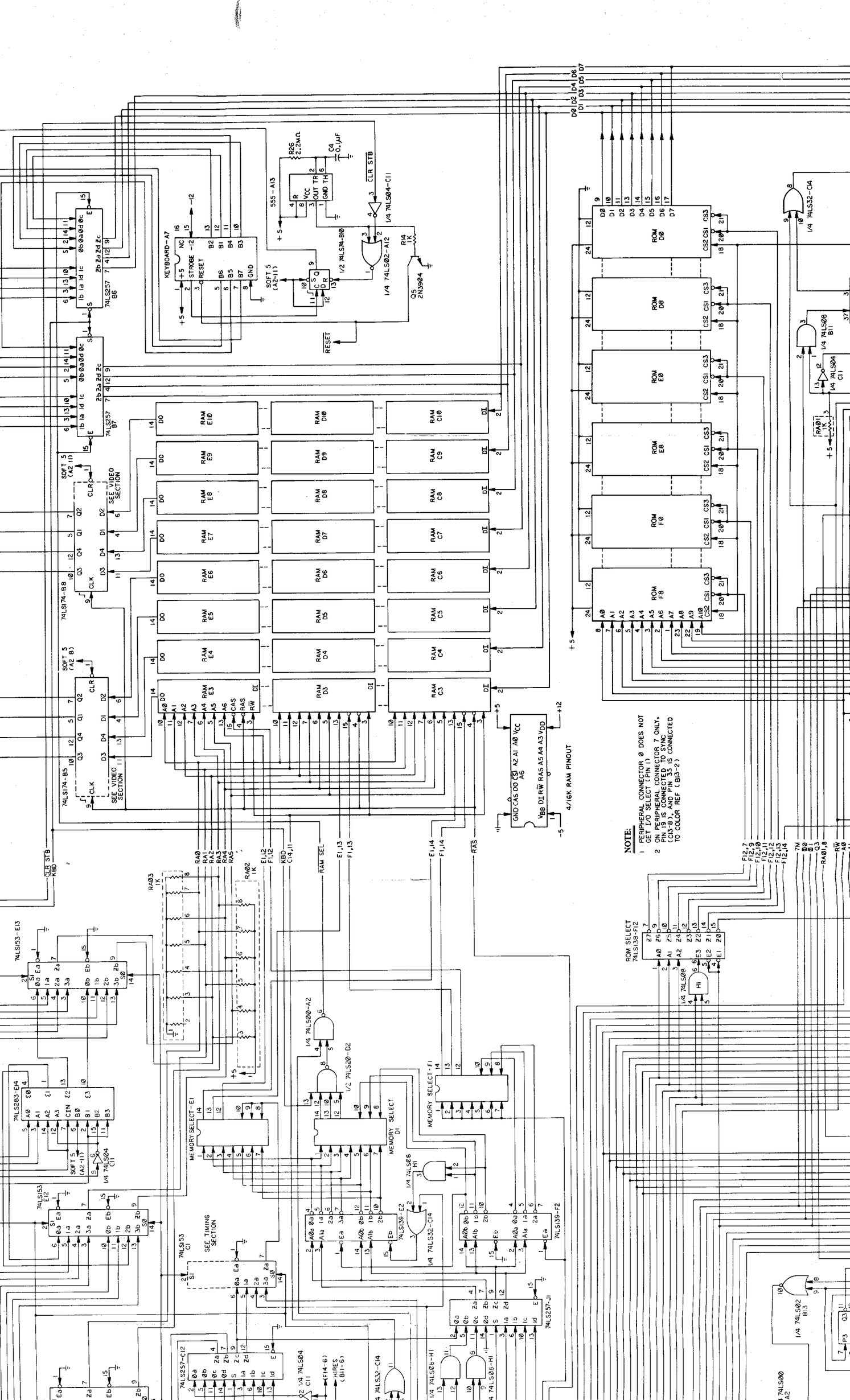
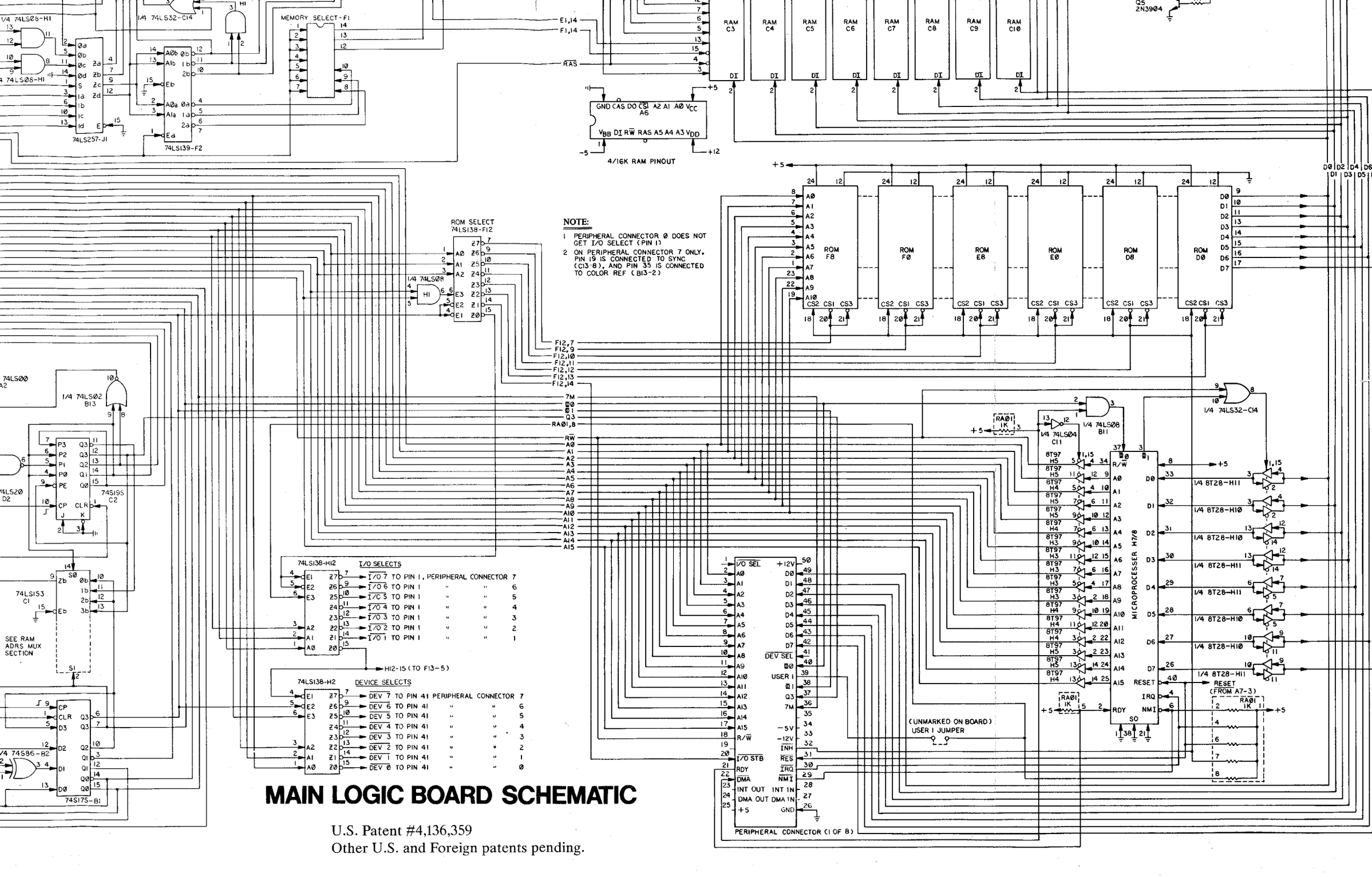
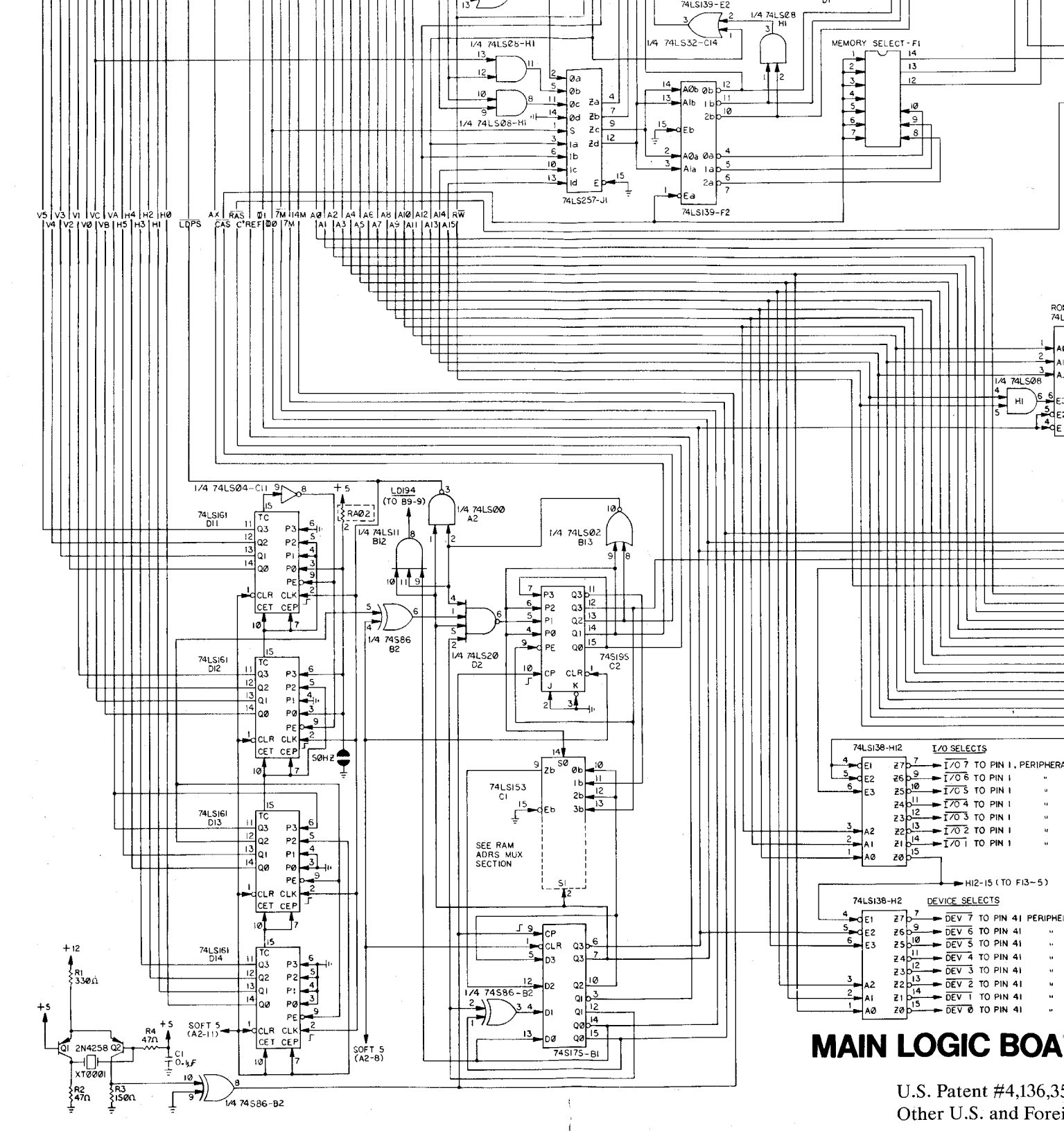

AUX VIDEO J14B
WIRE WRAP POST
VIDEO OUTPUT K14
C14 0.1μF
C13 0.1μF
R10 27Ω
R11 200Ω
R9 10Ω
Q3 2N3904
R8 2K
R6 2.7K
R7 1.5K
+12
+5
-5
LATCHED
D0 D1 D2 D3 D4 D5 D6 D7
SOFT 5 (A2-8)
SOFT 5 (A2-11)
74LS00 A2
74LS194 B9
74LS194-B4
74LS194-A10
74LS151 A9
74LS257-A8
1/2 74LS74-B10
1/2 74LS74-A11
SOFT 5 (A10-1)
555 TIMER B5
SYNC
R5
C14,6
VC
B5,2
7M
A12,13
A3,2
A5,1
B2,11
B3,3
14M
D0 LATCHED
GAME I/O CONNECTOR J14
QUAD TIMER 558-H13
74LS251-H14
74LS08-B11
74LS02-B13
74LS86-B2
74LS02 A12
74166 A3
2513 A5
MA741-K13
MPSA13 Q4
2-1/2" 8Ω SPEAKER B 14A
CASSETTE DATA IN
CASSETTE DATA OUT
1N914
74LS74-J13
74LS283-E14
74LS153-E13
74LS153 E12
74LS138-F13
74LS174 B8
74LS174-B5
(TO C12-5)
(TO C12-1)
(TO H11-11)
Q6 2N3904
R27 4.7K
H0


NOTE:
1 PERIPHERAL CONNECTOR Ø DOES NOT GET I/O SELECT (PIN 1)
2 ON PERIPHERAL CONNECTOR 7 ONLY, PIN 19 IS CONNECTED TO SYNC (C13-8), AND PIN 5 IS CONNECTED TO COLOR REF (B13-2)
4/16K RAM PINOUT
GND CAS DO WE A0 A1 A2 A6 VBB DI RW RAS A5 A4 A3 VDD
ROM SELECT 74LS138-F12
KEYBOARD-A7
555-A13
SOFT 5 (A2-11)
SOFT 5 (A2 8)
SOFT 5 (A2 11)
SEE VIDEO SECTION
SEE TIMING SECTION
RESET
CLR STB
KBD
RAM SEL
RAS
MEMORY SELECT-E1
MEMORY SELECT-F1
MEMORY SELECT D1
74LS257 B6
74LS257 B7
74LS174-B8
74LS174-B5
74LS153-E13
74LS153 E12
74LS153 C1
74LS283-E14
74LS257-C12
74LS257-J1
74LS139-E2
74LS139-F2
74LS08-A12
74LS04-C11
74LS00-A2
74LS20-D2
74LS32-C14
74LS08-H1
74LS02 B13
74LS06 B11
74LS04 C11
74LS08 H1
R26 2.2MΩ
C4 0.1μF
R14 1K
RA01 1K
RA02 1K
RA03 1K
Q5 2N3904
ROM D0
ROM D8
ROM E0
ROM E8
ROM F0
ROM F8
RAM E10
RAM D10
RAM C10
RAM E9
RAM D9
RAM C9
RAM E8
RAM D8
RAM C8
RAM E7
RAM D7
RAM C7
RAM E6
RAM D6
RAM C6
RAM E5
RAM D5
RAM C5
RAM E4
RAM D4
RAM C4
RAM E3
RAM D3
RAM C3
D0 D1 D2 D3 D4 D5 D6 D7
RA0 RA1 RA2 RA3 RA4 RA5
F1,12 F1,13 F1,14
E1,13 E1,14
F12,7 F12,9 F12,10 F12,11 F12,12 F12,13 F12,14
RA01,8
Q3
(F14-6) (B1-6)

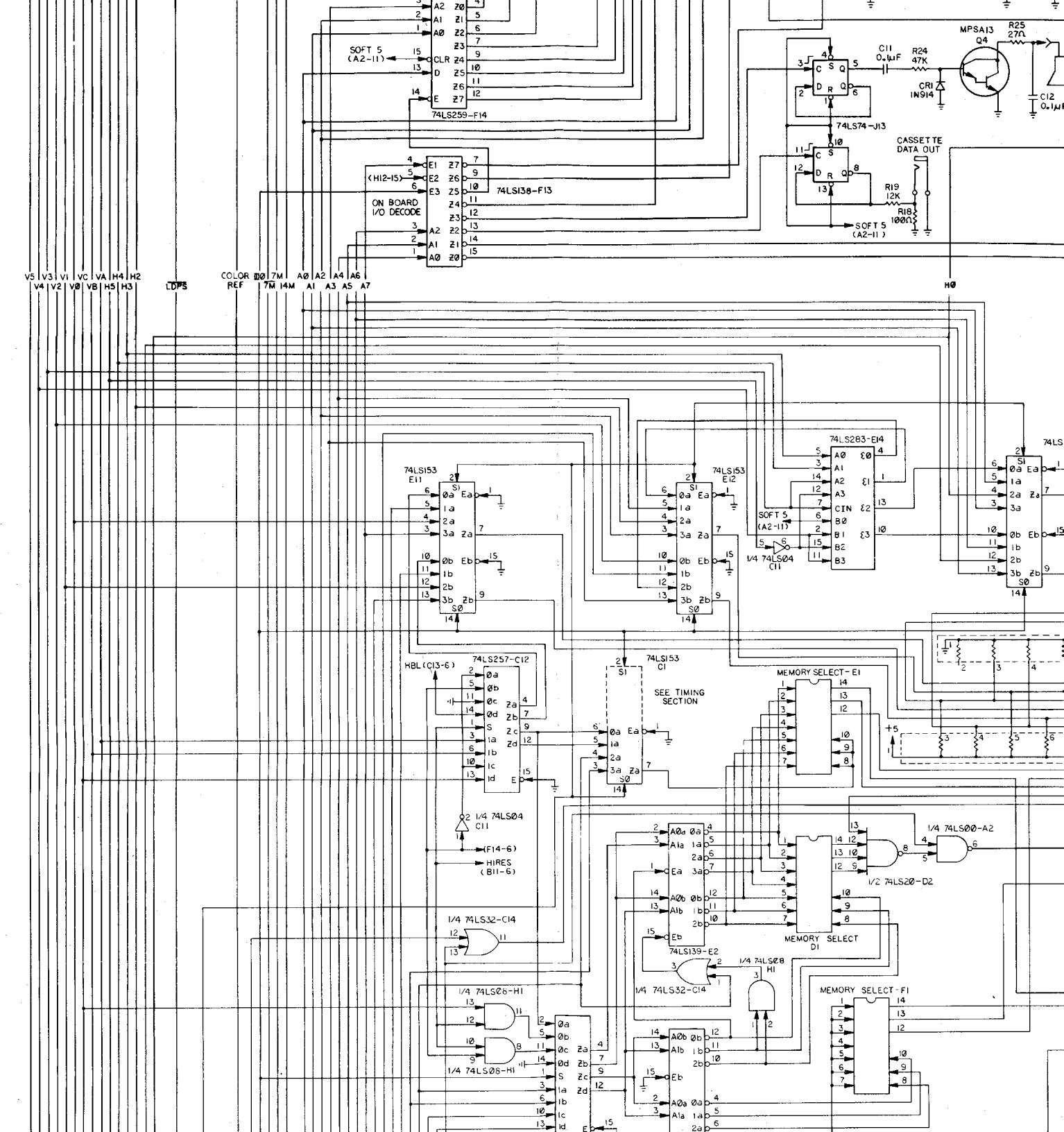


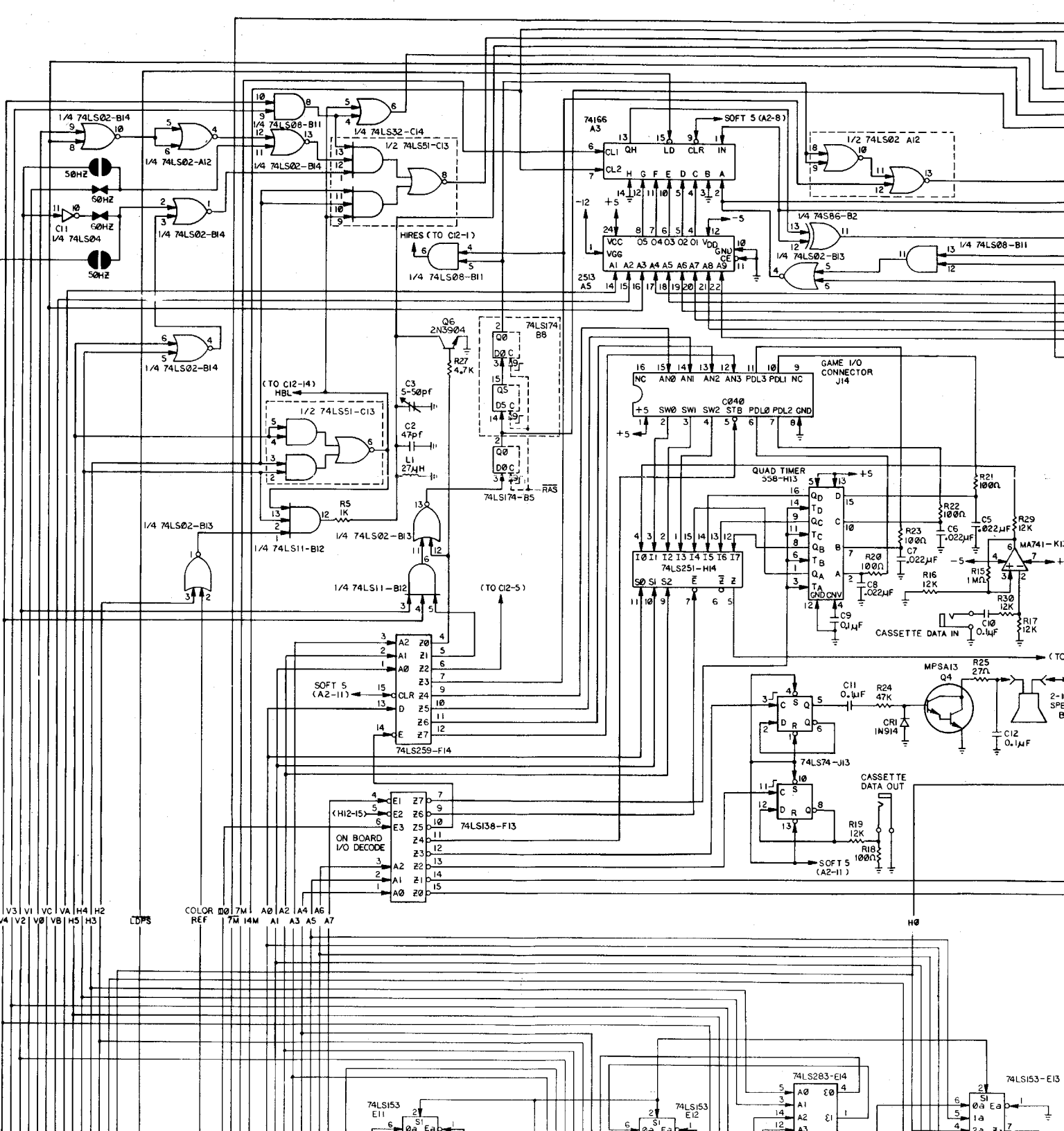
MAIN LOGIC BOARD SCHEMATIC

U.S. Patent #4,136,359
Other U.S. and Foreign patents pending.



MAIN LOGIC BOA


74LS259-F14
SOFT 5 (A2-11)
74LS74-J13
74LS138-F13
ON BOARD I/O DECODE
(HI2-15)
CASSETTE DATA OUT
MPSA13 Q4
R25 27Ω
R24 47K
C11 0.1μF
CR1 IN914
R19 12K
R18 100Ω
C12 0.1μF
V5 V4 V3 V2 V1 V0 VC VB VA H5 H4 H3 H2
LDPS
COLOR REF
ØØ 7M 7M 14M
A0 A1 A2 A3 A4 A5 A6 A7
H0
74LS153 E11
74LS153 E12
74LS283-E14
1/4 74LS04 C11
74LS257-C12
74LS153 C1
SEE TIMING SECTION
HBL(C13-6)
1/4 74LS04 C11
(F14-6)
HIRES (B11-6)
MEMORY SELECT-E1
MEMORY SELECT D1
MEMORY SELECT-F1
1/4 74LSØØ-A2
1/2 74LS20-D2
1/4 74LS32-C14
1/4 74LS08-H1
74LS139-E2
1/4 74LS08 H1
1/4 74LS32-C14
1/4 74LS08-H1


1/4 74LS02-B14
1/4 74LS02-A12
1/4 74LS08-B11
1/4 74LS02-B14
1/4 74LS32-C14
1/2 74LS51-C13
HIRES (TO C12-1)
1/4 74LS08-B11
50HZ
60HZ
C11
1/4 74LS04
74166
A3
SOFT 5 (A2-8)
1/2 74LS02 A12
1/4 74S86-B2
1/4 74LS02-B13
1/4 74LS08-B11
2513
A5
Q6
2N3904
74LS174
B8
R27
4.7K
(TO C12-14)
HBL
C3
5-50pf
C2
47pf
L1
27μH
74LS174-B5
RAS
R5
1K
1/4 74LS11-B12
GAME I/O
CONNECTOR
J14
C040
QUAD TIMER
558-H13
74LS251-H14
R21
100Ω
R22
100Ω
C5
.022μF
R29
12K
R23
100Ω
C6
.022μF
C7
.022μF
R20
100Ω
C8
.022μF
R15
1 MΩ
R16
12K
R30
12K
C9
0.1μF
C10
0.1μF
R17
12K
CASSETTE DATA IN
MA741-K1
(TO C12-5)
74LS259-F14
SOFT 5
(A2-11)
MPSA13
Q4
R25
27Ω
C11
0.1μF
R24
47K
CR1
IN914
C12
0.1μF
74LS74-J13
CASSETTE
DATA OUT
R19
12K
R18
100Ω
SOFT 5
(A2-11)
74LS138-F13
(H12-15)
ON BOARD
I/O DECODE
V3 V4 V1 V2 V0 VC VB VA H5 H4 H3 H2
LDPS
COLOR REF
7M 14M A0 A1 A2 A3 A4 A5 A6
H0
74LS153
E11
74LS153
E12
74LS283-E14
74LS153-E13

Addendum to the

Apple II Reference Manual

The main logic board of your Apple has been modified to reduce electromagnetic interference. This means that it is different from the Apple boards which are described in the Apple II Reference Manual. It will not, however, behave differently in any specific way unless you have changes made to it.

You will know you have a new main board by looking at the white F on the far left side of the board. You'll see there this nine digit number 82Ø-ØØ44-xx, where xx is the revision level.

The major differences in the new main board are described below. Also, the attached schematics show the areas in which this board is different from earlier boards. You may wish to note these differences in your Apple II Reference manual, on the pages which correspond to the schematics here.

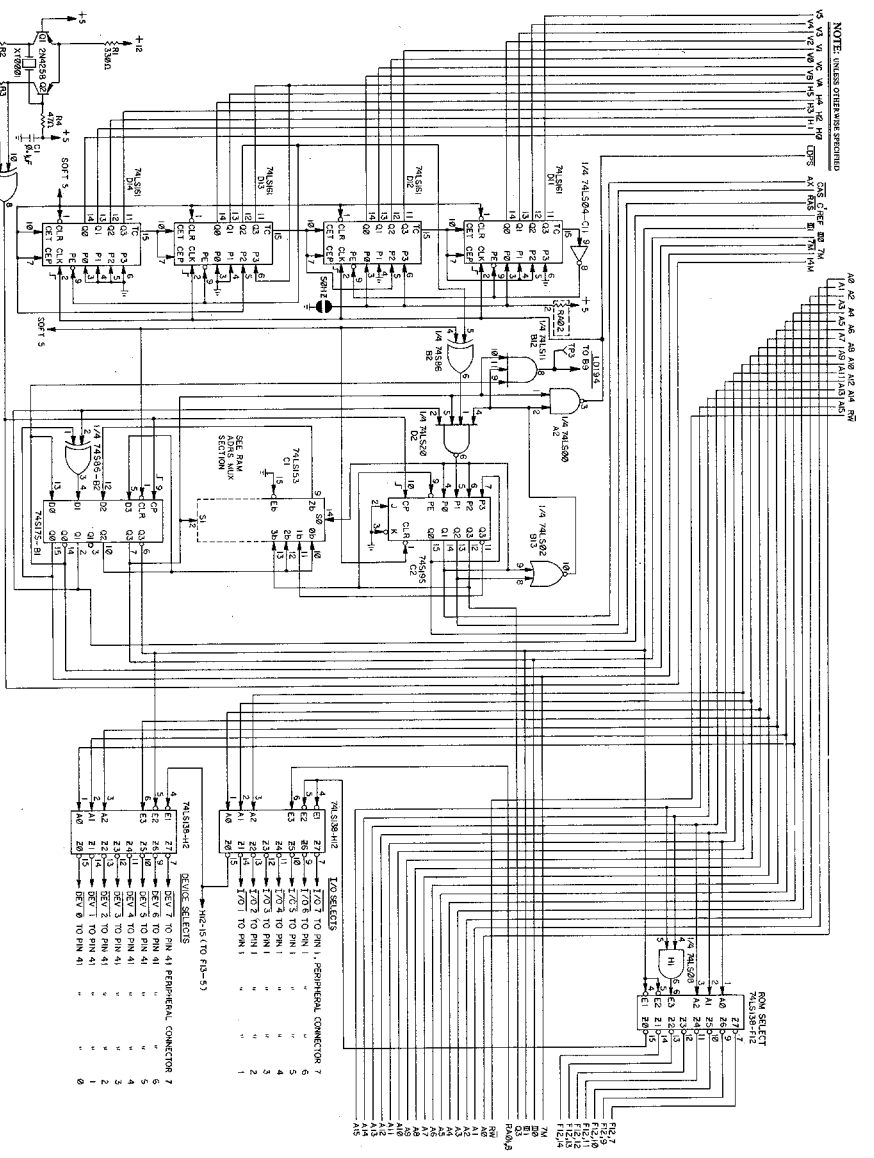
* The new board does not have RAM configuration blocks. This means the RAM Integrated Circuits (ICs) which give your Apple its memory MUST be 16K bit ICs. All of the RAM ICs in your Apple are within the white-outlined box on the board. If you add memory to your Apple, make sure all the ICs you add in this box are 16K Apple RAM.

* The IC which controlled the configuration blocks in the older versions of the Apple II board is no longer there. It was formerly in the E2 position on the Apple board (in the row labeled E, the second IC from the left of the board) and was marked 74LS139.

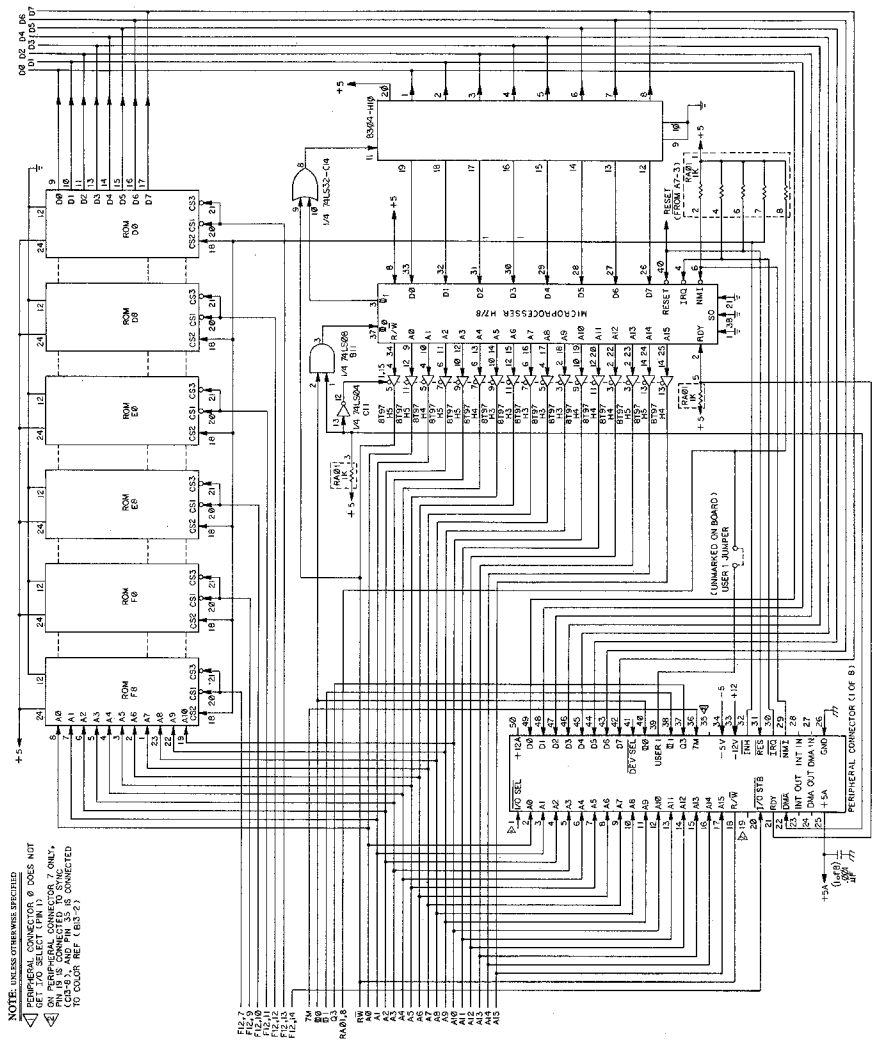
* This new board has a different character generator ROM IC. The character generator ROM IC determines what style of lettering, or character set, you'll see on your monitor or terminal screen. The new character generator ROM is found next to the Keyboard socket on the main board. This 2316B ROM has more space than the former 2513 character generator ROM, so that it's possible to have more than one character set available. The 2316B ROM can also be replaced with a 2716 EPROM, which allows you to program and change your own character sets.

* The color killer circuit, which damps out the color burst when your Apple is in text mode, has an added cutout circuit. The color burst is cut off in the logic circuit before it gets to the tank circuit. This gives you good black and white text, even if your color monitor has a sensitive color burst detector.

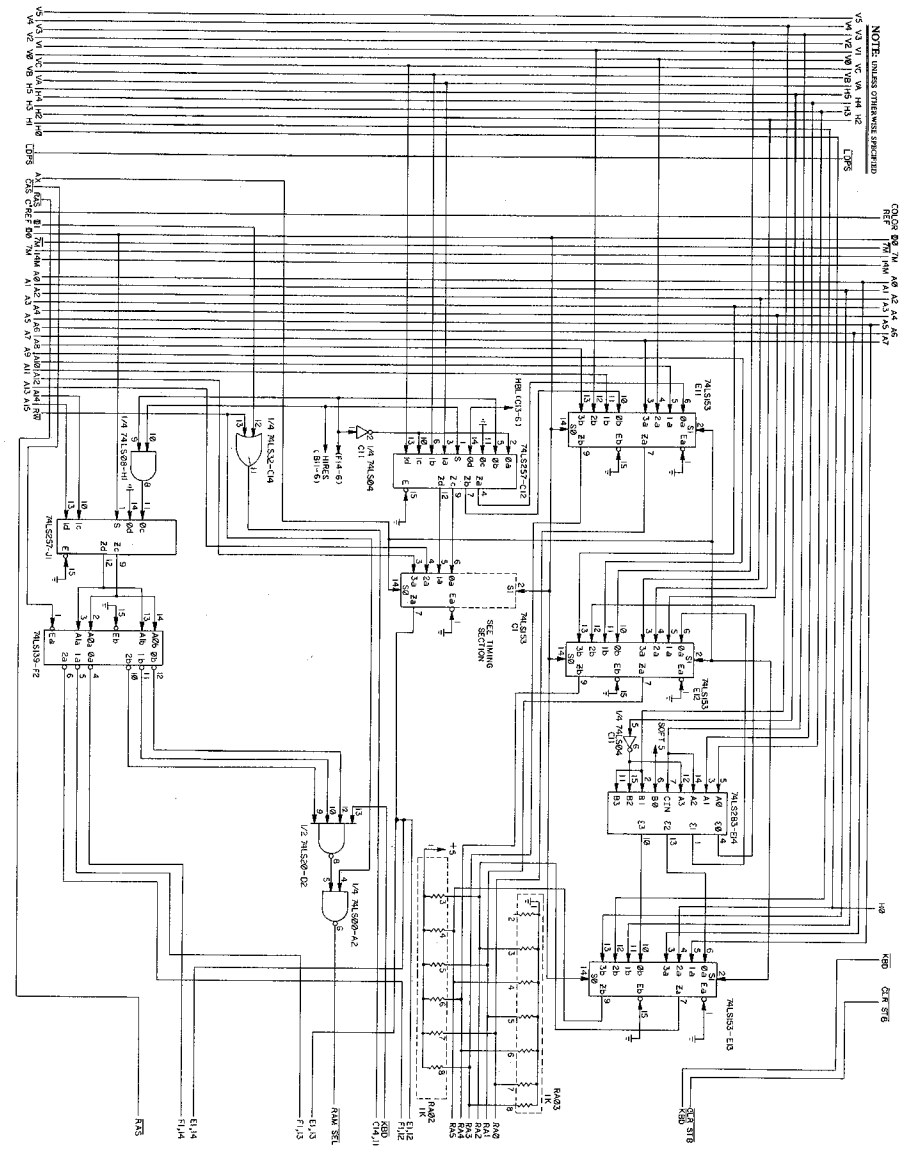
* The power and ground system has been redesigned. The +5V and ground bus on the rear of the board have been interchanged so that the +5V bus is on the top of the board and the ground is on the bottom. A grounding bar has been added under the board to ensure electrical contact between the board and the metal baseplate. Additional filters have been added to further reduce the EMI emission levels.



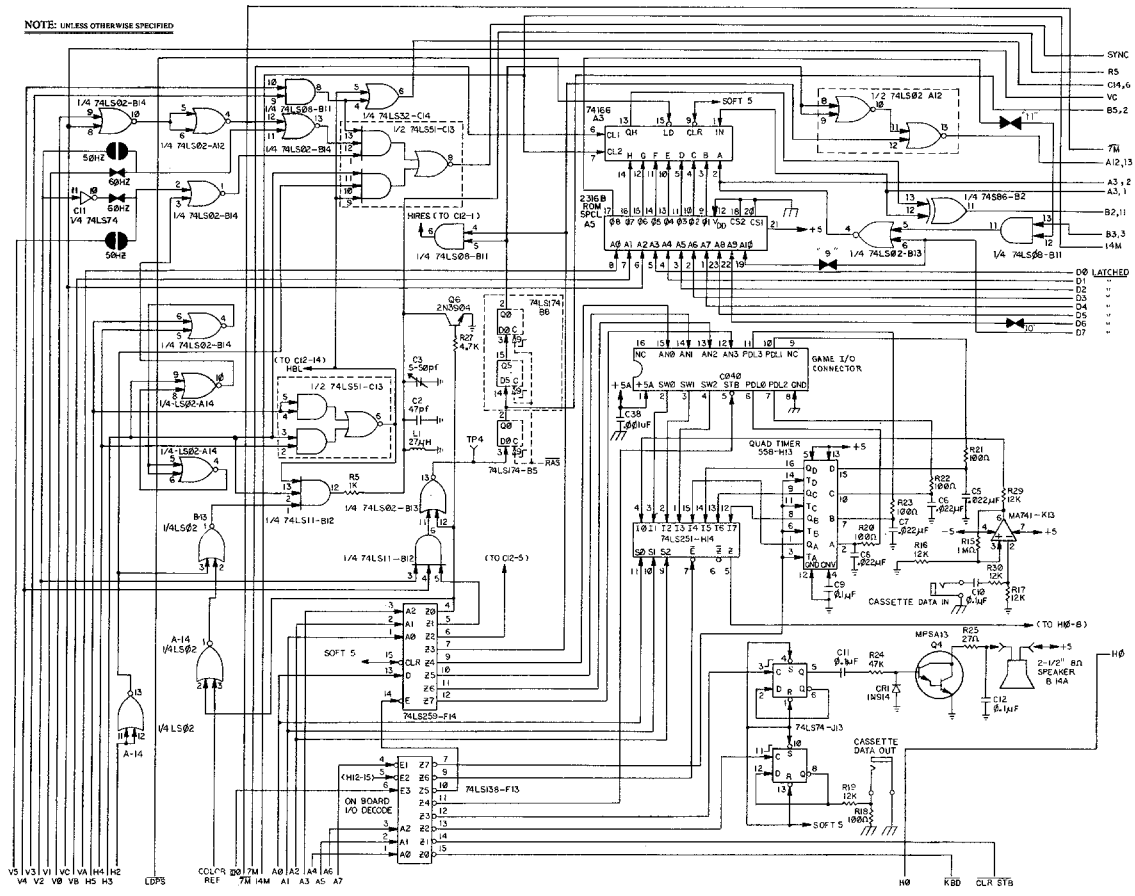
Replaces Figure 22-1. Schematic Diagram of the Apple II



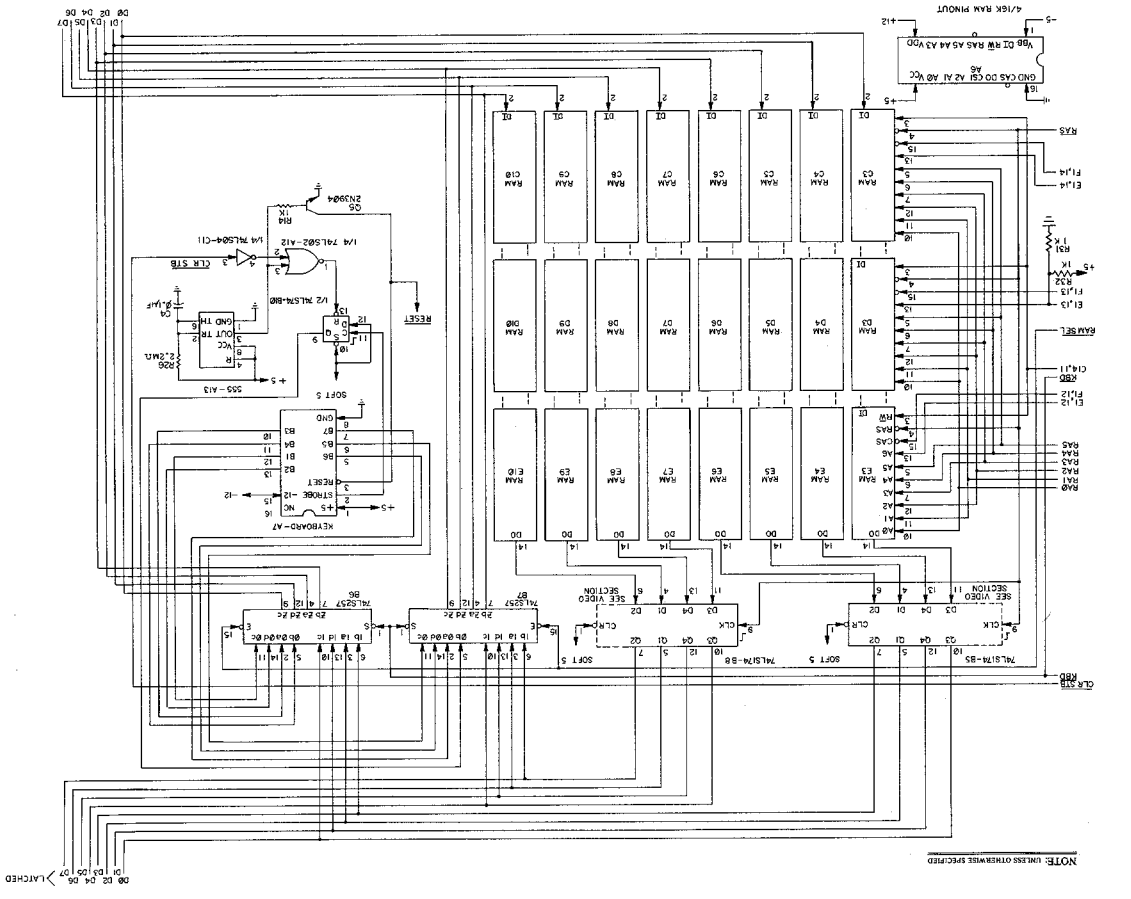
Replaces Figure 22-2. Schematic Diagram of the Apple II



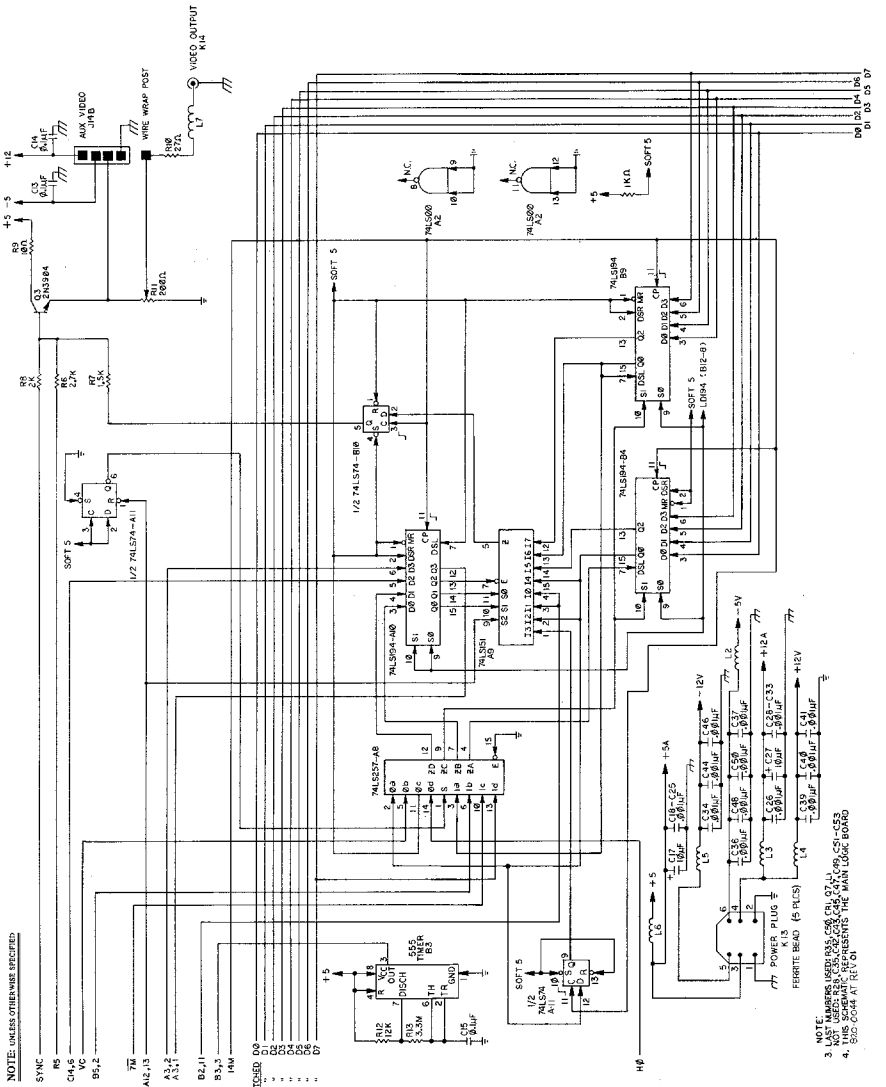
Replaces Figure 22-3. Schematic Diagram of the Apple II



Replaces Figure 22-5. Schematic Diagram of the Apple II



Replaces Figure 22-4. Schematic Diagram of the Apple II



Replaces Figure 22-6. Schematic Diagram of the Apple II