

Macintosh PowerBook 140 and Macintosh PowerBook 170

Developer Note



Developer Note

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Preface

About this note

This developer note describes the Macintosh PowerBook 140 and Macintosh PowerBook 170 computers and emphasizes features that are new and different from those of the Macintosh Portable and the Macintosh PowerBook 100 computers. This note assumes that you are already familiar with both the capabilities and programming requirements of Apple Macintosh computers, in particular the Macintosh Portable computer. If you are unfamiliar with Macintosh computers or would simply like more technical information on the hardware, you may want to obtain copies of related technical manuals. For information on how to obtain these manuals, see the following section.

For more information

To supplement the information in this document, you might wish to obtain related documentation such as *Guide to the Macintosh Family Hardware*, second edition; *Designing Cards and Drivers for the Macintosh Family*, second edition (third edition will soon be available), and *Inside Macintosh*, Volumes I through VI. Copies of these manuals are available through APDA (Apple Programmers and Developers Association). APDA offers convenient worldwide access to over 300 development tools, resources, and training products and to information for anyone interested in developing applications on Apple platforms. Customers receive the quarterly *APDA Tools Catalog*, featuring the most current versions of Apple development tools and the most popular third-party development tools. Ordering is easy; there are no membership fees, and application forms are not required for most of our

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Chapter 1 The Hardware

This chapter describes the major features of the Macintosh PowerBook 140 and Macintosh PowerBook 170 computers, and emphasizes the similarities and differences between these computers, the original Macintosh Portable computer, and other members of the Macintosh computer family.

Introduction

The Macintosh PowerBook 140 and Macintosh PowerBook 170 computers are new laptop, battery-operated, portable Macintosh computers weighing 6.8 pounds. They are smaller and lighter than the current Macintosh Portable, offer improved state-of-the-art CPU performance, are designed to be extremely rugged and portable, and should appeal to anyone wishing to use a Macintosh computer away from its usual environment (office, classroom, laboratory, and so on).

The Macintosh PowerBook 140 has a 68030 microprocessor running at 16 MHz, a backlit Film SuperTwist Nematic (FSTN) display, and a built-in 20 MB hard disk. The more powerful Macintosh PowerBook 170 has a 68030 microprocessor running at 25 MHz, a 68882 FPU (floating-point unit), a backlit active matrix display, and a built-in 40 MB hard disk. The Macintosh PowerBook 140 does not include a 68882 FPU. To enhance the overall capabilities of these portable computers, expansion slots (connectors) are provided for RAM cards and modem cards.

Features

This section lists the major features of the Macintosh PowerBook 140 and the Macintosh PowerBook 170 portable computers.

- Microprocessor: 68030 running at 25 MHz (Macintosh PowerBook 170) and 16 MHz (Macintosh PowerBook 140).
- Coprocessor: 68882 FPU (not available on Macintosh PowerBook 140).
- Read-only memory (ROM): 1 MB.
- Random-access memory (RAM): 2 MB of pseudostatic RAM (PSRAM) on main logic board; in addition, PowerBook 170 includes 2 MB RAM expansion card.
- RAM expansion: RAM expansion card that allows RAM expansion in increments of 2 MB, 4 MB, or 6 MB.

- Video display: Macintosh PowerBook 170 has a flat-panel, transreflective active matrix LCD (liquid crystal display); Macintosh PowerBook 140 has a flat-panel, transmissive mode, FSTN LCD. Both displays are 640 x 400 pixels, with on-demand CCFL (cold cathode fluorescent lamp) backlighting.
- Floppy disk: one internal 20-pin floppy disk connector and one internal 1.4 MB 19-mm Apple SuperDrive with Super Woz Integrated Machine (SWIM) interface. Drive does not have automatic inject feature.
- Hard disk: one 30-pin flex cable with HDI (high-density interface) 30-pin SCSI (Small Computer System Interface) connector for internal hard disk drive. The Macintosh PowerBook 170 has one internal 40 MB, 2.5-inch SCSI hard disk drive; the Macintosh PowerBook 140 has one internal 20 MB, 2.5-inch SCSI hard disk drive.
- I/O (input/output): one HDI-30 SCSI connector for an external device, one mini-DIN, 4-pin Apple Desktop Bus (ADB) port, two mini-DIN 8-pin serial ports, and audio input and stereo output jacks; no connector for an external floppy disk drive.
- Sound: enhanced Apple Sound Chip (ASC) that supports stereo sound out.
- Keyboard: built-in 3.0-mm travel keyboard with centered pointing device (30-mm trackball); no built-in keypad option.
- Modem: internal 20-pin connector for 2400-baud modem card with send fax (modem is standard in Macintosh PowerBook 170, optional in Macintosh PowerBook 140).
- Battery: 2.5 ampere-hour NiCad rechargeable battery; backup provided by 3-V rechargable lithium battery.
- Power jack: external jack that provides the interface for the external wall-mounted recharger/power adapter.
- Weight: 6.8 pounds.
- Size: 11.3 inches wide, 9.3 inches long, and 2.25 inches high.

Design architecture

These new portable computers include many of the Macintosh Portable computer's architectural features such as power management, SWIM, and Versatile Interface Adapter (VIA) functions. The powerful 68030 microprocessor replaces the 68HC000 microprocessor used in the Macintosh Portable. A Combo chip, identical to that used in the Macintosh IIsi and the Macintosh LC computers, combines the functions of SCSI and SCC (Serial Communications Controller). Sound input and output are implemented using an enhanced Apple Sound Chip, low-power discrete audio output circuitry, and the Digitally Filtered Audio Chip (DFAC).

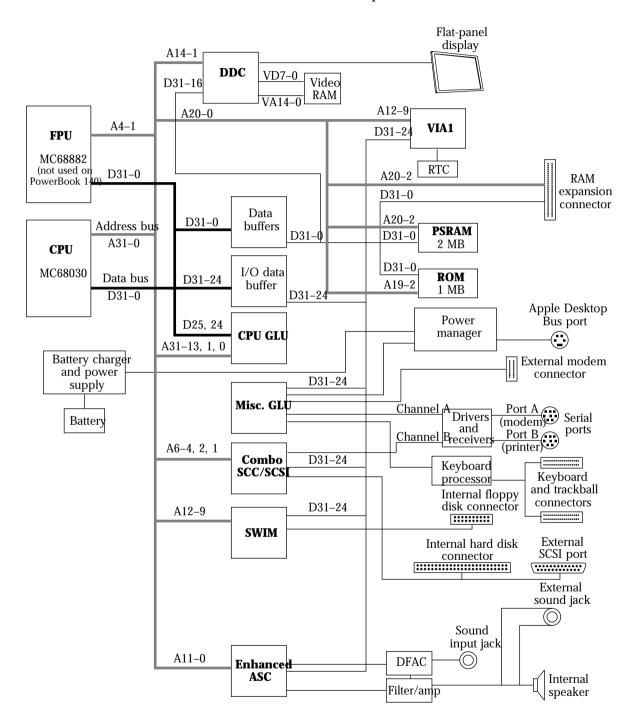
One of the primary considerations in the design was power conservation. A unique power cycling feature turns off the 68030 processor (and the 68882 coprocessor on the Macintosh PowerBook 170) when they are not in use, thus drastically reducing power consumption. PSRAM, the same as used in the backlit version of the Macintosh Portable, replaces the SRAM (static RAM) used in the original version of Macintosh Portable and has the advantage of providing lower sleep current at reduced cost.

The design includes three new custom integrated circuits (ICs): CPU GLU (General Logic Unit), Miscellaneous GLU, and the DDC (Display Driver Chip). The CPU GLU serves as the interface to the circuits that communicate with the main processor, the Miscellaneous GLU provides the random logic functions for circuits that communicate with the Power Manager, and the DDC provides access to a separate SRAM to support the flat-panel display. Figure 1-1 is a block diagram showing the relationships of the major components of the computers.

Machine identification

By using the Gestalt Manager (the successor to SysEnvirons), you can determine whether your application is running on a Macintosh PowerBook 140, a Macintosh PowerBook 170, or another Macintosh model. You should first check for the appropriate machine selector code (21 for both the Macintosh PowerBook 140 and the Macintosh PowerBook 170). Next check for the presence or absence of an FPU, as explained in "On-board Mathematics Coprocessor (FPU)." later in this chapter. If the routine returns a selector code of 21 and also indicates that an FPU is present, then your application is running on a Macintosh PowerBook 170. A selector code of 21 together with the absence of an FPU identifies the machine as a Macintosh PowerBook 140. A selector code other than 21 indicates some other Macintosh model.

• **Figure 1-1** Block diagram of the Macintosh PowerBook 140 and Macintosh PowerBook 170 computers



Compatibility issues

Although the architecture of the new portable computers is based partially on that of the original Macintosh Portable, it also incorporates many new features, resulting in some possible hardware and software compatibility issues. The rest of this section describes those new features and related compatibility issues.

Floppy disks

The Macintosh PowerBook 140 and Macintosh PowerBook 170 computers have only one built-in 1.4 MB SuperDrive and do not have a connector for an external floppy disk drive.

External SCSI connector

An HDI-30 connector provides the SCSI interface for external devices. This connector is smaller and has a different pinout than the DB-25 SCSI connector used on previous Macintosh computers. Electrical information is provided in the section "SCC and SCSI Interfaces" later in this chapter.

SCSI and SCC implementation

The Combo chip combines the functions of SCSI and SCC and is described in the section "SCC and SCSI Interfaces" later in this chapter. Although this chip is software compatible with the previous implementation of these functions, your applications may be inoperable if they attempt to access the hardware directly.

An application should use normal communications calls to talk to the serial driver; it should never attempt to get direct access to the SCC hardware. The serial chip is turned off when not in use; if your application makes normal serial communications calls, the serial driver knows how to turn the serial chip back on. However, an application that attempts to go directly to the serial chip will wind up talking to the chip when it is turned off, resulting in a loss of communication.

Sound input/output hardware

Details on the sound system implementation are provided in the section

"Sound Interface" later in this chapter. The sound interface uses an enhanced version of the Apple Sound Chip (ASC) together with the DFAC to provide compatibility with the overall Macintosh sound input/output strategy. If your application uses the Macintosh Sound Manager calls and does not try to access the ASC hardware directly, it will work as documented.

On-board mathematics coprocessor (FPU)

The 68882 FPU is a standard feature of the Macintosh PowerBook 170 computer but is not supported on the Macintosh PowerBook 140 computer. To ensure that your application is compatible with the Macintosh PowerBook 170, the Macintosh PowerBook 140, and future Macintosh computers that do not have FPUs, use the Gestalt Manager. Using the Gestalt Manager allows you to determine the exact configuration of the machine on which you are running.

If your application is provided in two versions, one that uses SANE (Standard Apple Numerics Environment) software and another that requires the FPU hardware to perform its numeric calculations, or if the application makes a conditional branch to execute floating-point instructions directly, then your application should check first for the presence of an FPU.

Hardware overview

This section provides a functional description of the processor, memory, general logic, and I/O (input/output) interface systems. Emphasis is placed on those systems that are new or different from those of the earlier Macintosh Portable and other members of the Macintosh computer family.

Important Memory sizes, addresses, and other data are specific to each type of Macintosh computer and are provided for informational purposes only. To ensure that your application software maintains compatibility across the Macintosh line and to allow for future hardware changes, you are strongly advised to use the Macintosh Toolbox and Operating System routines wherever provided. In particular, never use absolute addresses to access hardware, because these addresses are different on different models. ◆

Main processor

The 68030 microprocessors used in the Macintosh PowerBook 140 and Macintosh PowerBook 170 run at system clock rates of 16 MHz and 25 MHz, respectively. The 68030 includes a built-in MMU (memory management unit) that performs the necessary memory-mapping functions. Floating-point operations in the Macintosh PowerBook 170 are provided by the 68882 mathematics coprocessor FPU. The Macintosh PowerBook 140 does not include an FPU.

Memory mapping

Two memory address-mapping modes, a 24-bit mode and a 32-bit mode, are implemented. This allows older software to use the 24-bit address space and new software to use the full 32-bit address space. Figure 1-2 shows the main 32-bit memory map and the 32-bit I/O memory map decode of the system I/O address space from \$5000 0000 to \$6000 0000. Figure 1-3 compares the system's main 32-bit memory map with the 24-bit memory map. Notice in Figure 1-3 that video space resides at location \$FEE0 0000 (32-bit mode) or \$E0 0000 (24-bit mode) and not in either RAM or I/O space. Also, you can access the I/O space in 32-bit mode while maintaining a 24-bit mode offset of \$F0 0000 for compatibility. This is because all I/O devices wrap into \$Fx xxxx space.

• **Figure 1-2** 32-bit memory and detailed I/O map

		/	Expansion I/O s	\$6000 0
		/	(no DSACKs)	\$5400 O
		/	Reserv	\$5100 O
A		_ /	Reserv	
\$FFFF FI	Reserv	/	Reserv	\$5010 0 \$500C 0
\$FEFF FFL	Video R/	/	CPU GLU regis	\$5000 0
\$FEE0 0	Video R <i>F</i>	/	Reserv	\$5008 0 \$5004 0
		/	Reserv	\$5003 0
	D	/	Reserv	\$5002 E
	Reserv	/	Reserv	\$5002 C
		/	Reserv	\$5002 A
		[/	Reserv	\$5002 8
\$6000 0	1/0	ľ	Reserv	\$5002 6
\$5000 0	I/O		Reserv	\$5002 4
	Reserv	\ .	Reserv	\$5002 2
\$4400 0	RON	<u> </u>	Reserv	\$5002 0
\$4000 0	ROV	<i>i</i>	Reserv	\$5001 E
		,	Reserv	\$5001 C
	Expansio	1	Reserv Reserv	\$5001 A
	RAM	,		\$5001 8
		\	SWII Sound	\$5001 6
		,	SCSI (non D	\$5001 4
\$0400 0		\	SCSI (normal r	\$5001 2
	(Wrap)	Ì	Reserved (SCSI	\$5001 0
\$0080 0	RAN	\	Reserved (SCC	\$5000 E
	8 MB maximum,	\ \	Reserved (VIA2	\$5000 C
\$0000 0(one continuous b	,	Reserved (VIA1	55000 A
	1	,	SCSI (DMA with	\$5000 8
		, .	SC(\$5000 6 \$5000 4
		/ .	VIA	\$5000 4
		\	VIA	\$5000 2
		4		ι ΨΟΟΟΟ Ο

• **Figure 1-3** 32-bit and 24-bit memory maps

32-bit memory map

24-bit memory map

\$FFFF FF		\$FF FFF[
\$FEFF FF	Reserv	\$F0 FFF	I/O space
\$FEE0 0	Video R <i>i</i>	\$E0 000L	Video R <i>i</i>
ΦΓΕΟ Ο	Reserv	ф <u>го ооог</u> (Reserv
\$6000 0			
\$5000 0	I/O space	\$90 000	
\$4400 0	Reserv		ROM
	RON	\$80 00C	
\$4000 0	Expansio RAM		RAM
\$0400 0			
\$0080 0	(wraț		
\$0000 0	RAN 8 MB maximum, One continuous I	\$00 000L l	

Custom integrated circuits

This section describes the three ASICs (application-specific integrated circuits) that provide the internal logic functions of the computers.

CPU GLU

The CPU GLU is a custom gate array that accommodates 24-bit mode and 32-bit mode address compatibility, interrupt encoding, and full-power cycling logic implementation. The CPU GLU generates the CPU clocks, DSACK (data acknowledgment) signals, and buffer control signals and serves as the interface to system ROM, RAM, SCC, SCSI, VIA, FPU, SWIM, and DDC integrated circuits. The CPU GLU also supports a Macintosh II–style 32-bit memory map, pseudostatic RAM refresh, and the ability to make noncontiguous memory appear contiguous for RAM sizes of 1 and 4 Mbits.

DDC (Display Driver Chip)

The DDC provides the interface to the LCD. Its function is similar to that of the video chip used in the Macintosh Portable, except that the DDC supports FSTN (Film SuperTwist Nematic) displays as well as active matrix (AM) displays. The DDC generates horizontal and vertical synchronization pulses and all other signals necessary to make the flatpanel display work. The DDC also supports its own video 32K x 8-bit SRAM. In addition, the DDC limits the CPU from refreshing the display and thereby allows the CPU to do more useful work.

Miscellaneous GLU

The Miscellaneous GLU is a modified version of the Miscellaneous GLU used in the Macintosh Portable. One of the most significant functions of the Miscellaneous GLU chip is emulating the I/O capabilities of a second VIA in a manner similar to that of a Macintosh IIci computer's RBV (RAM-based video) chip. In addition, the Miscellaneous GLU chip provides random logic functions such as modem/serial port muxing, sound power control, and the clock control logic functions associated with the Power Manager, SWIM, and SCC interfaces.

ROM interface

The new portable computers use a 1 MB 32-bit-clean ROM. This ROM includes some functions similar to those of the Macintosh Portable ROM, such as a new ADB interface and code to support communication with the Power Manager. Backlight control, a true shutdown mode, and improved modem support are all featured in the Power Manager ROM code; however, unlike in the Macintosh Portable, the real-time clock function is not provided by the Power Manager. Instead, these computers use the same serial clock chip and interface logic as are used in the Macintosh Classic computer. These functions are separated from the Power Manager in order to maintain the real-time clock and parameter RAM when the Power Manager chip is off. The ROM also includes 32-bit QuickDraw.

The ROM is implemented as a 256K x 32-bit array consisting physically of two

 $256K \times 16$ -bit 40-pin devices with an access time of 150 ns. The ROM array is located in the system memory map between addresses \$4000 0000 and \$4010 0000.

RAM overlay: Immediately after the system is reset or is taken out of the sleep mode, the RAM overlay process is initiated, causing the starting address of the ROM to be located at \$4000 0000 and overlaying the ROM image in RAM address space starting at \$0000 0000. This overlay allows the 68030 processor to address a standard default set of exception vectors and trap addresses as well as a starting address at which to begin executing code. Following the first access to the normal ROM address range, the ROM image at \$0000 0000 is cleared and replaced by RAM.

ROM wait states: Access to the ROM from the main processor in the Macintosh PowerBook 170 requires three processor wait states (six clock access cycles at 25 MHz). This relates to a bus cycle time of 240 ns. In the Macintosh PowerBook 140, access to the ROM from the main processor requires two processor wait states (five clock access cycles at 16 MHz). This relates to a bus cycle time of 320 ns.

RAM interface

The new portable computers are shipped with 2 MB of PSRAM on the main logic board. The RAM is arranged physically as four 4-Mbit chips of 512K x 8 bits each. In addition, there is an expansion slot that allows RAM to be expanded to a total of 8 MB. The PowerBook 170 is shipped with a 2 MB RAM expansion card in this slot giving that machine a total of 4 MB of RAM. The expansion feature is described in the next section, "RAM Expansion."

RAM is always contiguous because only one size of RAM chip (4 Mbits) is used. As a result, software does not have to size the memory. The RAM array is nominally located in the system memory map between addresses \$0000 0000 and \$0020 0000 (up to \$0080 0000 in an 8 MB system), except following a system reset or sleep cycle, at which time it is overlaid by system ROM. However, the overlay is removed following access to normal ROM space, and the RAM space is then accessible. Both RAM and ROM memory spaces provide DSACK signals to the processor even if memory is not actually installed.

RAM wait states: Access to the RAM from the main processor requires 100 ns PSRAM. The Macintosh PowerBook 170 requires two processor wait states (five clock cycles per RAM access), and the Macintosh PowerBook 170 requires one processor wait state (four clock cycles per RAM access). The PSRAM, unlike the SRAM in the original Macintosh Portable, must be refreshed. The CPU GLU custom chip includes special circuitry that performs the refresh function.

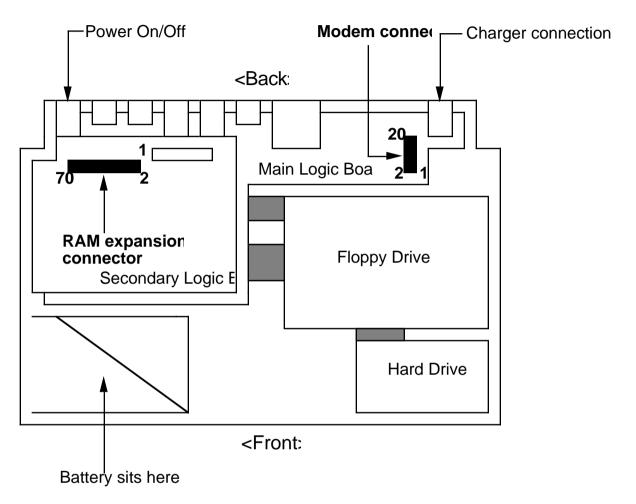
Battery backup: Both main and expansion RAM memories are backed up when the computer is in the sleep mode. This means that when the computer is not in use, the contents of the memory array are retained as long as the battery remains charged.

RAM expansion

The secondary logic board (often referred to as the daughterboard) contains a 70-pin RAM expansion connector (slot) that supports RAM expansion card sizes of 2 MB, 4 MB, and 6 MB. The location and orientation of the connector is shown in Figure 1-4.

• Note: If you design a RAM expansion card correctly, it will also work in the Macintosh PowerBook 100 computer, a new 68HC000-based portable computer. The 68030 processor in the Macintosh PowerBook 140 and the Macintosh PowerBook 170 has a 32-bit data bus, whereas the 68HC000 processor in the Macintosh PowerBook 100 has only a 16-bit data bus. You should design the expansion card as a 32-bit device, but if you correctly partition the data lines and chip select lines on the card, you can use the same card in any of these machines without loss of performance. The card should have 32 data lines coming out to its connector, and the chip select lines for the upper 16 data bits and the lower 16 data bits should be separated to allow for individual selection of either the upper 16 bits or the lower 16 bits of data. The separated chip select lines are necessary for the 68HC000-based machine because it can get access to only 16 bits at a time. A 68030-based machine does not require separated chip select lines because it has a 32-bit data bus; therefore, the lines are tied back together on the computer's main logic board.

• Figure 1-4 Location of modem and RAM expansion connectors



As is the case with the permanent ROM, only 4-Mbit chips are used for expansion RAM. For example, a 4 MB RAM expansion card has eight 4-Mbit PSRAMs (512K x 8-bit chips arranged as two banks of 32 bits), and a 6 MB card has twelve 4-Mbit PSRAMs (512K x 8-bit chips arranged as three banks of 32 bits). Access and cycle times for these devices are 100 ns.

♦ Important If you are designing a RAM expansion card for these computers, you do not have to include logic for address decode or chip select because all of the required signals (address, data, chip select, and control) are available at the RAM expansion connector. Data buffering is also provided to compensate for the extra loading caused by the RAM expansion card chips. •

RAM expansion connector signals

Table 1-1 provides the pin number, name, and description of each of the RAM expansion connector signals.

♦ *Note*: If you are designing a RAM expansion card, you should normally consider pin 49 (/ROM.CS.EXP) as no connection, unless your expansion card includes its own ROM and it is intended to replace system ROM.

•	Table 1-1	RAM	expansion	connector	signals
---	-----------	-----	-----------	-----------	---------

Pin nun	nber Signal name	Signal description	
1	GND	Ground	
2	GND	Ground	
3	A20	Address bit 20 (unbuffered)	
4	A17	Address bit 17 (unbuffered)	
5	A18	Address bit 18 (unbuffered)	
6	A19	Address bit 19 (unbuffered)	
7	A16	Address bit 16 (unbuffered)	
8	/LLW	Lower write byte	
9	A14	Address bit 14 (unbuffered)	
10	/LUW	Lower middle write byte	
11	A9	Address bit 9 (unbuffered)	
			(continued)

• Table 1-1 RAM expansion connector signals (continued)

Pin nu	mber Signal name	Signal description
12	A15	Address bit 15 (unbuffered)
13	A8	Address bit 8 (unbuffered)
14	A10	Address bit 10 (unbuffered)
15	A7	Address bit 7 (unbuffered)
16	A11	Address bit 11 (unbuffered)
17	A6	Address bit 6 (unbuffered)
18	A13	Address bit 13 (unbuffered)
19	A5	Address bit 5 (unbuffered)
20	/RAM.OE	RAM output enable and refresh for 4 MB PSRAMs
21	A4	Address bit 4 (unbuffered)
22	A12	Address bit 12 (unbuffered)
23	A3	Address bit 3 (unbuffered)
24	/RAMACS1	PSRAM bank chip select bit 1
25	A2	Address bit 2 (unbuffered)
26	MDATA23	Bit 23, 32-bit-wide memory data bus (buffered)
27	MDATA16	Bit 16, 32-bit-wide memory data bus (buffered)
28	MDATA22	Bit 22, 32-bit-wide memory data bus (buffered)
29	MDATA17	Bit 17, 32-bit-wide memory data bus (buffered)
30	MDATA21	Bit 21, 32-bit-wide memory data bus (buffered)
31	MDATA18	Bit 18, 32-bit-wide memory data bus (buffered)
32	MDATA20	Bit 20, 32-bit-wide memory data bus (buffered)
33	GND	Ground
34	/RAMACS1	PSRAM bank chip select bit 1
35	MDATA4	Bit 4, 32-bit-wide memory data bus (buffered)
36	MDATA19	Bit 19, 32-bit-wide memory data bus (buffered)
37	MDATA2	Bit 2, 32-bit-wide memory data bus (buffered)
38	MDATA3	Bit 3, 32-bit-wide memory data bus (buffered)
39	MDATA0	Bit 0, 32-bit-wide memory data bus (buffered)
40	MDATA1	Bit 1, 32-bit-wide memory data bus (buffered)
41	MDATA7	Bit 7, 32-bit-wide memory data bus (buffered)
42	MDATA6	Bit 6, 32-bit-wide memory data bus (buffered)
43	+5V.SH	+5 V (RAM power/shutdown plane)
44	MDATA5	Bit 5, 32-bit-wide memory data bus (buffered)
		(continued)

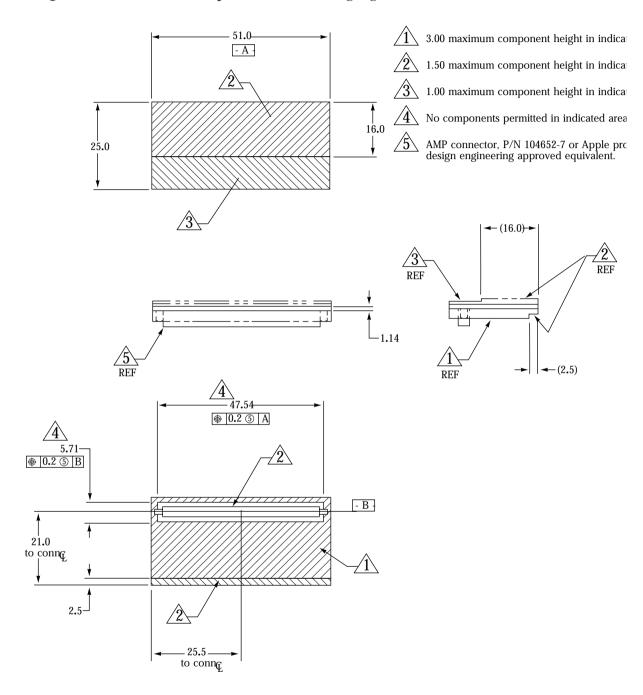
• **Table 1-1** RAM expansion connector signals (continued)

45 /RAMACS3 PSRAM bank chip select bit 3 46 +5V.SH +5 V (RAM power/shutdown plane) 47 /UUW Upper write byte 48 /ULW Upper middle write byte 49 /ROM.CS.EXP ROM chip select 50 /RAMACS2 PSRAM bank chip select bit 2 51 /RAMACS3 PSRAM bank chip select bit 3 52 +5V.SH +5 V (RAM power/shutdown plane) 53 MDATA27 Bit 27, 32-bit-wide memory data bus (buffered) 54 MDATA28 Bit 28, 32-bit-wide memory data bus (buffered) 55 MDATA14 Bit 14, 32-bit-wide memory data bus (buffered) 56 MDATA29 Bit 29, 32-bit-wide memory data bus (buffered) 57 MDATA24 Bit 24, 32-bit-wide memory data bus (buffered) 58 MDATA30 Bit 30, 32-bit-wide memory data bus (buffered) 60 MDATA25 Bit 25, 32-bit-wide memory data bus (buffered) 61 MDATA26 Bit 26, 32-bit-wide memory data bus (buffered) 62 MDATA15 Bit 13, 32-bit-wide memory data bus (buffered) 63 MDATA13 Bit 13, 32-bit-wide memory data bus (buffered) 64 MDATA8 Bit 8, 32-bit-wide memory data bus (buffered) 65 MDATA12 Bit 12, 32-bit-wide memory data bus (buffered) 66 MDATA9 Bit 9, 32-bit-wide memory data bus (buffered) 67 MDATA11 Bit 11, 32-bit-wide memory data bus (buffered) 68 MDATA10 Bit 10, 32-bit-wide memory data bus (buffered) 69 GND Ground 70 /RAMACS2 PSRAM bank chip select bit 2	Pin number	Signal name	Signal description
47 /UUW Upper write byte 48 /ULW Upper middle write byte 49 /ROM.CS.EXP ROM chip select 50 /RAMACS2 PSRAM bank chip select bit 2 51 /RAMACS3 PSRAM bank chip select bit 3 52 +5V.SH +5 V (RAM power/shutdown plane) 53 MDATA27 Bit 27, 32-bit-wide memory data bus (buffered) 54 MDATA28 Bit 28, 32-bit-wide memory data bus (buffered) 55 MDATA14 Bit 14, 32-bit-wide memory data bus (buffered) 56 MDATA29 Bit 29, 32-bit-wide memory data bus (buffered) 57 MDATA24 Bit 24, 32-bit-wide memory data bus (buffered) 58 MDATA30 Bit 30, 32-bit-wide memory data bus (buffered) 59 MDATA25 Bit 25, 32-bit-wide memory data bus (buffered) 60 MDATA31 Bit 31, 32-bit-wide memory data bus (buffered) 61 MDATA26 Bit 26, 32-bit-wide memory data bus (buffered) 62 MDATA15 Bit 15, 32-bit-wide memory data bus (buffered) 63 MDATA13 Bit 13, 32-bit-wide memory data bus (buffered) 64 MDATA8 Bit 8, 32-bit-wide memory data bus (buffered) 65 MDATA12 Bit 12, 32-bit-wide memory data bus (buffered) 66 MDATA9 Bit 9, 32-bit-wide memory data bus (buffered) 67 MDATA11 Bit 11, 32-bit-wide memory data bus (buffered) 68 MDATA10 Bit 10, 32-bit-wide memory data bus (buffered) 69 GND Ground	45	/RAMACS3	PSRAM bank chip select bit 3
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69 GND Ground	67	MDATA11	Bit 11, 32-bit-wide memory data bus (buffered)
	68	MDATA10	Bit 10, 32-bit-wide memory data bus (buffered)
70 /RAMACS2 PSRAM bank chip select bit 2	69	GND	Ground
	70	/RAMACS2	PSRAM bank chip select bit 2

RAM expansion card design guide

Figure 1-5 is a design guide providing the physical information you will need to design a RAM expansion card for the Macintosh PowerBook 140 and Macintosh PowerBook 170 computers.

• Figure 1-5 RAM expansion card design guide



Floppy disk interface

A SWIM chip (the same as that used in other Macintosh computers) controls the single internal 3.5-inch SuperDrive. A 20-pin connector provides the signal interface between the SWIM chip and the drive. Unlike the larger Macintosh computers, the Macintosh PowerBook 140 and the Macintosh PowerBook 170 portable computers do not accommodate an external floppy disk drive. Table 1-2 shows the pinout for the internal floppy disk connector.

• Table 1-2 Pinout for internal floppy disk connector

Pin number	Signal name	Signal description
1	GND	Ground
2	PH0	Phase 0: state control line
3	GND	Ground
4	PH1	Phase 1: state control line
5	GND	Ground
6	PH2	Phase :state control line
7	GND	Ground
8	PH3	Phase 3: register write strobe
9	/SYS.PWR	System power
10	/WREQI	Write data request
11	FD1.+5V/0	+5 V/0 V (awake/sleep)
12	HDSELI	Head select
13	FD1.+5V/0	+5 V/0 V (awake/sleep)
14	/DISK1EN	Drive enable
15	FD1.+5V/0	+5 V/0 V (awake/sleep)
16	RD	Read data
17	FD1.+5V/0	+5 V/0 V (awake/sleep)
18	WRDATA	Write data
19	nc	No connection
20	nc	No connection

SCC and SCSI interfaces

A custom chip called the Combo combines the functions of the SCC and the SCSI controller in a single device. This device is completely software compatible with the SCC (85C30) and SCSI (53C80) chips it replaces.

SCC

The SCC portion of the Combo chip includes two independent ports for serial communication. Each port can be independently programmed for asynchronous, synchronous, or AppleTalk protocols.

Two 8-pin miniature DIN connectors connect the SCC to the external world of printers, modems, and any other standard I/O devices requiring an RS-422 serial interface. The connectors are the same as those currently used on other Macintosh computers. Although the serial ports are identical, the port designated for the modem has a higher interrupt priority and is more suitable for high-speed communications. Table 1-3 shows the pinout for the serial ports.

• Table 1-3 Serial port pinouts

Pin number	Signal name	Signal description
1	HSKo	Handshake output
2	HSKi	Handshake input
3	TxD-	Transmit data –
4	SG	Signal ground
5	RxD-	Receive data –
6	TxD+	Transmit data +
7	GPi	General-purpose input
8	RxD+	Receive data +

SCSI

The SCSI portion of the Combo chip is completely compatible with the SCSI controller chip used on current members of the Macintosh family. It is designed to support the

SCSI interface as defined by the American National Standards Institute (ANSI) X3T9.2 committee. In addition to the SCSI portion of the combined SCC/SCSI device, the interface consists of two HDI-30 SCSI connectors. The internal HDI-30 connector is used for the built-in 2.5-inch hard drive and replaces the 50-pin SCSI connector used on earlier Macintosh computers; the external HDI-30 connector provides the interface for external SCSI devices and replaces the external DB-25 connector used on earlier Macintosh computers. The SCSI portion of the Combo chip connects directly to the internal and external SCSI connectors and can sink up to 48 mA through each of the pins connected to the SCSI bus. The data and control signals on the SCSI bus are active low signals that are driven by open drain outputs. Table 1-4 shows the pinouts for internal and external SCSI connectors.

• Table 1-4 Pinouts for internal and external HDI-30 SCSI connectors

Pin number	HDI-30 (internal)	HDI-30 (external)
1	DISK.+5	/LINK.SEL
2	DISK.+5	/DB0
3	GND	GND
4	GND	/DB1
5	GND	TERMPWR (not used; reserved for future
use)		
6	/DB0	/DB2
7	/DB1	/DB3
8	/DB2	GND
9	/DB3	/ACK
10	/DB4	GND
11	/DB5	/DB4
12	/DB6	GND
13	/DB7	GND
14	/DBP	/DB5
15	DISK.+5	GND
16	/BSY	/DB6
17	/ATN	GND
18	/ACK	/DB7
19	GND	/DBP
20	/MSG	GND
21	/RST	/REQ
22	/SEL	GND
23	/C/D	/BSY
24	/I/O	GND
25	/REQ	/ATN
26	GND	/C/D
27	GND	/RST
28	GND	/MSG
29	DISK.+5	/SEL
30	DISK.+5	/I/O

Internal hard disk drive

The Macintosh PowerBook 170 computer has an internal 2.5-inch, 40 MB hard disk drive that connects to the computer through the HDI-30 internal SCSI connector. The Macintosh PowerBook 140 uses an identical interface for its internal 2.5-inch, 20 MB hard disk drive.

Hard disk drive design considerations

The following information is provided as a general guideline and is based on the specifications for Apple's 2.5-inch, 20 MB and 40 MB hard disk drives. Probably the most important concern when designing an internal SCSI hard drive for these portable computers is the need for a small form factor and low power consumption.

Power requirements: The 20 MB and 40 MB hard disk drives operate on $5 \text{ VDC} \pm 5$ percent. Voltage ripple tolerence is 100 mV peak to peak from DC to 10 MHz.

The following charts show the maximum and mean current drain and power consumption requirements for the various operating modes of the 40 MB and 20 MB hard disk drives. These limits include 1 kilohm pull-up terminator resistors on all signal lines. All mean specification limits are in RMS (root mean square) values.

Power requirements for 40 MB hard disk drive

Mode	Current (Amps)		Power (Watts)		
	Mean	Max	Mean	Max	
Startup		1.110		5.00	
Random operatio	n .450	.540	2.25	2.70	
Idle	.260	.300	1.30	1.50	
Shutdown	.080	.100	0.40	0.50	

♦ Note: Startup power is based on RMS values during a typical startup time of 10 seconds. Maximum peak current allowed during startup time is 1.11 amps for a duration of not more than 5 seconds. Random operation power is based on RMS values during a 40 percent random seek, a 40 percent read/write, and a 20 percent idle mode.

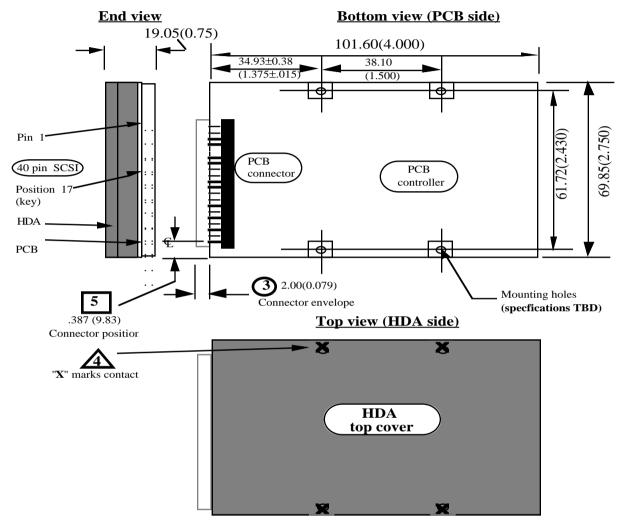
Power requirements for 20 MB hard disk drive

Mode	Curre Mean	nt (Amps) Max	Power (Watts) Mean Max
Startup	.860	1.000	4.30 5.00
Random operation	.540	.600	2.70 3.00
Idle	.300	.400	1.50 2.00
Shutdown	.090	.190	0.45 0.95

• Note: Startup power is based on RMS values during a typical startup time of 10 seconds. Maximum peak current allowed during startup time is 1 amp for a duration of not more than 3 seconds. Random operation power is based on RMS values during a 40 percent random seek, a 40 percent read/write, and a 20 percent idle mode.

Dimensions and mounting requirements: Figure 1-6 shows the drive and connector envelope requirements for the hard disk drive. The drive and its mating connectors are constrained to the envelope shown. The drive is mounted with a spring force bracket that contacts the top cover in four points directly above the mounting posts of the drive chassis.

• **Figure 1-6** Envelope requirement for the 2.5-inch, hard disk drive



Notes:

- **1.** All dimensions in mm(inches in parantheses).
- Tolerances (unless otherwise noted): .XX = +/- .25mm(.XXX = +/- .010inches).
 Connector envelope includes cable routing and is designed for a connector receptacle with flex circuit.
- Denotes mounting bracket contact points on HDA top cover with reference to HDA chassis mounting posts. Top cover must be flat or planar surface of 19.05 mm in contact points areas.
- 5. Connector position from edge of drive to center line of first connector Pin.

Sound interface

The sound system includes a built-in speaker, an external stereo headphone jack that

plays in monaural but to both ears, and a microphone input jack for sound input. A microphone and an RCA adapter plug are shipped with the computer to facilitate the use of the sound input feature. The sound input strategy takes advantage of the enhanced ASC and the DFAC.

♦ Note: The Sound Manager chapter of Inside Macintosh, Volume VI, explains the application-programmer interface for the Sound Input Manager and describes the high-level and low-level calls that you can implement in your application programs to allow users to take advantage of the computer's sound input feature.

Although the ASC has been enhanced, it remains plug compatible with the older ASC. The enhanced ASC no longer supports four voice synthesis (mono) or two-voice synthesis (stereo), but it does support the following features:

- record mode for sound input (together with the DFAC)
- hardware sample rate conversion
- real-time hardware decompression
- 8-bit final amplitude scaling registers
- 16-bit digital serial output
- 10-bit PWM (pulse-width-modulated) signal resolution at 44.1 kHz sample rate

The DFAC is a custom IC that does the analog processing functions for the sound system. The DFAC contains a switched filter capacitor, an analog-to-digital converter, and switching and amplifier circuits. An on-chip register in the DFAC contains 8 bits that control the routing of the analog sound signals through the system. These bits are accessed through the sound volume control outputs from VIA2. The setting of the 8 DFAC control bits determines the mode of sound operation.

VIA interface

The hardware includes a VIA1 and a virtual VIA2. VIA1 provides some I/O control, generates useful interrupts, and ensures compatibility with existing Macintosh software. Although VIA2 is not a physical device, its functions are supplied by the Miscellaneous GLU custom IC in much the same manner as by the RBV (RAM-based video) chip in the Macintosh IIsi. These functions include the necessary register, interrupt, and I/O support that would be provided by a real VIA.

Video interface

The video interface consists of the DDC, which is similar to the video chip in the original Macintosh Portable, and video SRAM. The DDC generates the vertical and horizontal synchronization pulses necessary to make the flat-panel display work.

The 68030 microprocessor views the video interface as a continuous RAM array of 32 KB beginning at \$FEE0 0000 (32-bit mode) or \$E0 0000 (24-bit mode). The video interface is nominally 16 bits wide but is byte addressable similar to main memory. The first pixel displayed on the screen is the most significant bit of the byte found in the upper-left corner, and the last pixel displayed is the least significant bit of the byte found in the lower-right corner. Pixels displayed in between first and last are addressed in a similar manner. You can think of the video display as a linear array of bits.

Flat-panel display and backlighting

The Macintosh PowerBook 170 computer uses an active matrix display that provides a high-quality presentation of alphanumeric and graphics information on a

217-mm x 140-mm active display area. The Macintosh PowerBook 140 computer uses an FSTN display. Both displays are supported by ondemand CCFL backlighting similar to that used on the Macintosh Portable; however, unlike in the Macintosh Portable, display backlighting is not adjusted through the portable CDev but is adjusted manually by the user.who simply slides a mechanical control (potentiometer) to adjust the amount of screen brightness. The Power Manager performs an A/D (analog-to-digital) measurement of the voltage output from the control and sends it to a software driver (called .Backlight). The software driver then tells the Power Manager to adjust its PWM signal. The Power Manager filters the signal to a DC level and sends it to the CCFL inverter to control power to the backlight.

Power Manager

The computers use a modified version of the Macintosh Portable computer's Power Manager. Functions such as the real-time clock (RTC) and the PRAM have been removed from the Power Manager microprocessor and are now provided by a real RTC chip in the same manner as in many other Macintosh computers. The wakeup timer feature has been eliminated.

The Power Manager communicates with the main processor by using an asynchronous handshake mechanism and an 8-bit parallel data bus in conjunction with the second VIA. The Power Manager provides the following functions:

- It performs power management activities (for example, enabling or disabling clocks to I/O devices such as the SWIM chip to reduce power consumption during idle or sleep periods and physically enabling or disabling various power planes).
- It performs the transceiver functions for the Apple Desktop Bus (ADB).
- It generates the brightness level (via the PWM function) for the inverter to control the backlight brightness of the display.
- It monitors the level of the battery charge to warn the user if the voltage becomes too low, or if the computer should shut down in order to preserve its memory contents.
- It monitors whether the system is in sleep or shutdown mode, depending on whether the charger is plugged in, and whether the user has pushed the power on/off button.
- It provides sleep mode control, system reset control, and several signals that support the modem.

Power states

There are three power states: Power On, Sleep, and Power Off (Shutdown). The power on/off button, the reset button, the keyboard, or a Finder command can control the power state of the machine. Table 1-5 lists the starting states, the actions that cause the starting states to change, and the ending states that result from each action.

• Table 1-5 Power states

Starting state	Action	Ending state
Power off	Press power button	Power
on		
Power on	Issue shutdown command	Power off
Power on off	Press power button , no charger attache	ed Power
Power on	Issue sleep command, charger attached	l Sleep
Power on off	Issue sleep command, charger not atta	ched Power
Power on	Press power button, charger attached	Sleep
Power on	Press reset button	Power on
Sleep	Press any key	Power on
Sleep	Press power button	Power on
Sleep	Press reset button	Sleep
Sleep	Detect extremely low power condition	Power off
Power off and	Insert charger	Power off charging

If you are writing an application, such as a smart alarm, that includes software that can put the computer into the sleep state, you must use the Sleep trap rather than directly addressing the Power Manager trap.

◆ *Note:* For a description of the operating system calls associated with the Power Manager's "sleep" function, see the Power Manager section of *Inside Macintosh*, Volume VI.

Shutdown feature

Both the Macintosh PowerBook 170 and the Macintosh PowerBook 140 incorporate a "true" shutdown feature that conserves battery power by allowing the user to turn the computer off to the point where only the real-time clock, parameter RAM, and other essential support circuits remain on. This is unlike the Macintosh Portable, in which the choice provided by the Shut Down menu leaves the Power Manager and other power-consuming devices on.

The main difference between the shutdown and sleep states is the amount of DC current drain. The shutdown state turns off main RAM, all custom integrated circuits, the keyboard processor, the Power Manager, VIA, SWIM, SCC/SCSI, serial driver chips, and many other nonessential devices, resulting in a DC current drain of about 400 μA (or about 4 percent of the DC current drain of the sleep state). In comparison, the sleep state acts about the same on the new portable computers as it does on the Macintosh Portable by leaving these devices on, but in a low power mode, where the total DC current drain is about 5 mA. The result of the shutdown feature is a longer battery storage life (without recharging) compared to the Macintosh Portable, in which shutdown and sleep modes are approximately the same in terms of power drain on the battery.

Power cycling

Power cycling is a new power-saving feature that replaces the idle mode used in the Macintosh Portable computer. When the Macintosh Portable is in the "idle" state, the number of main processor wait states to RAM increases from 1 to 64, saving at best 10 percent of the CPU power (approximately 75 mW for the 68030). Power cycling in the Macintosh PowerBook 140 and Macintosh PowerBook 170 reduces the processor's power up to 90 percent (450 mW for the 68030 and 150 mW for the 68882) during idle periods.

Power cycling works as follows. The registers of the 68030 (and the 68882 of a Macintosh PowerBook 170) are saved, and power to them is turned off if no input activity is detected for approximately 2 seconds. The remaining system is left on, the cursor continues to blink, and the keyboard is still scanned.

The power cycle consists of driving the processor's address and data lines low, disabling the selects to any chips that are on, and then restoring power to the processor no later than 16 milliseconds after power is turned off. When power is back on, the processor registers are restored and the processor monitors the system for activity. If none is detected within 2 microseconds, the power cycle repeats.

Guidelines for developing application software for a power-cycling environment

If you are writing an application to run in the power-cycling environment, follow these guidelines to ensure that your application is power-saving friendly.

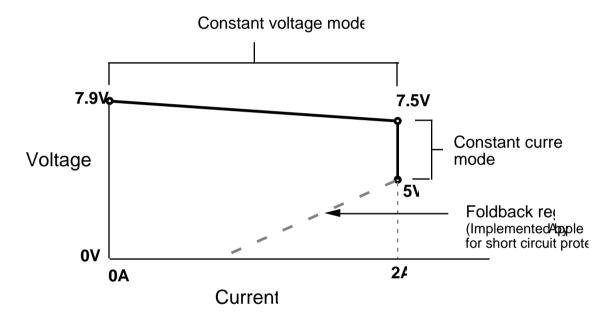
- Whenever your application does not require the system, it should return time to the system by issuing a "wait next event" call. This call initiates a power cycle that saves power and, after a predetermined time, allows the system to run another application.
- An application should not use hard-coded timing loops because power cycling changes the speed of the processor. Instead you should use the low-memory global variables to govern timing loops.
- An application should not automatically open AppleTalk or the serial driver unless the application intends to use them. For example, if your application opens AppleTalk but does not use it, the computer cannot go to sleep because it assumes there is an external network connection, and as a result power cannot be saved.
- An application should bring a hard drive up to speed once, get all its necessary resources, and then turn the drive off rather than continually recycling the drive. A lot of power is wasted by a drive that is running all of the time.

A/C power adapter

The A/C power adapter is designed to operate in a constant current and constant voltage mode. This means that the voltage supplied by the power adapter remains relatively constant and fluctuates only slightly (in the range of 7.9 volts to 7.5 volts) as a result of current supplied by the power adapter. Likewise, the current supplied by the power adapter remains relatively constant and fluctuates only slightly (in the range of 1.8 amps to 2.2 amps) as the result of voltage supplied by the power adapter. As the computer's battery approaches its fully charged state, the power adapter changes from a constant current mode to a constant voltage mode, at which point the voltage supplied by the power adapter slowly increases until the battery reaches its fully charged state. See Figure 1-7 for a typical example of A/C power adapter operation.

The A/C power adapter is designed to draw a maximum of 100 microamps of leakage current at 7 volts when A/C power is not supplied to the adapter (that is, the adapter is not plugged in). This design prevents excessive draining of the battery by constantly maintaining battery voltage at the computer's power adapter terminal, regardless of the state of the A/C power adapter (that is, whether the power adapter is or isn't plugged in).

• **Figure 1-7** Typical A/C power adapter operating range



Modem interface

The main logic board includes a 20-pin modem connector. Refer to Figure 1-4 for the location and pin orientation of the modem connector. The connector accommodates an Apple modem card or a compatible third-party modem card. This section provides the information you will need if you are designing your own modem card and software.

Modem card electrical interface

The modem card connects to the computer through a 20-pin dual inline socket connector. The data is at CMOS levels (that is, $V_{IL} = 0$ to 0.8 V; V_{IH} = 3.5 to V+; I_{OL} = 1.6 mA; and I_{OH} = 25 μ A). Table 1-6 provides the pin number, name, type, and description of each signal available at the modem connector.

• **Table 1-6** Modem connector signals

Pin number	Signal name	Signal type	Signal description		
1 MODEM.N5 to modem or go to ground 500 m		–5 V power co	ontrolled by host and provided circuitry. This Pin 1 may float following		
negation of MODEM.					
This signal is	_				
2 MODEM.PWI see "Modem	R Input	Active high s	ignal from Power Manager; Power-Control Interface"		
later in this chapter.					
3 GND		Electrical gro	und.		
4 /MODEM.BU	SY	Output	Modem busy; active low		
signal asserted by mod	dem	1	and sent to		
Power Manager when		is busy.			
5 US5V		+5 V power;	provides +5 VDC \pm 5 % to		
modem			whenever computer has		
power available.			-		
6 RxD	Output	Receive data;	data received by modem and		
then sent	-		to computer via RxD pin on		
SCC.					
7 /RI.DETECT	Output	Ring detect; a	ctive low signal sent to Power		
Manager			to indicate that ring is		
present. If computer is			"sleep" mode,		
assertion of this signal			computer to		
awake and power up	modem.				
8 TxD	Input	Transmit data	a; data and commands that		
are sent			from computer to modem		
via TxD pin on SCC.					
9 MODEM.SOU		Output	Audio output; analog		
sound high-impedance	e output				
		signal sent by	modem to computer's sound		
circuitry.					
10 /DTR	Input		ready; an active low signal		
whose		behavior depe	ends on state of &D		
command.	_				
11 MS.ENABLE	Output	Modem soun	d enable; active high signal		
that modem			sends to computer's sound		
circuitry whenever			modem's sound monitor is		
on.					

12	/RTS	Input	Request to send; active low signal sent by
compu	ıter		to modem via RTS pin on
SCC.			
13	RESET	Input	Reset; active high signal asserted after
Power		_	Manager switches –5 V power to modem
or any	time		modem needs to be reset.
			(continued)

Table 1-6 Modem connector signals (continued)

Pin number		Signal name	Signal type	Signal description	
14	/CTS	Output	Clear to send	active low signal asserted by	
moden	n as			default option and sent to	
compu	ter via CTS pin				
			on SCC.		
15	/MODEM.INS	SERT	Output	Modem inserted; active low	
signal	continuously		-	asserted by modem and sent	
to Power Manager				whenever modem card is	
installe	ed in computer.				
16	GND		Electrical gro	und.	
17	GND		Electrical gro	und.	
18	MODEM.5V		+5 V power controlled by Power Manager		
and			provided to r	nodem. This pin will float or	
go to			ground 500 m	ns after MODEM.PWR signal	
goes low			(inactive).		
19	/DCD	Output	Data carrier d	letect; active low signal,	
driven by				modem, whose behavior	
depends on state of			&C command.		
20	MODEM.5V		Same as pin 1	18.	

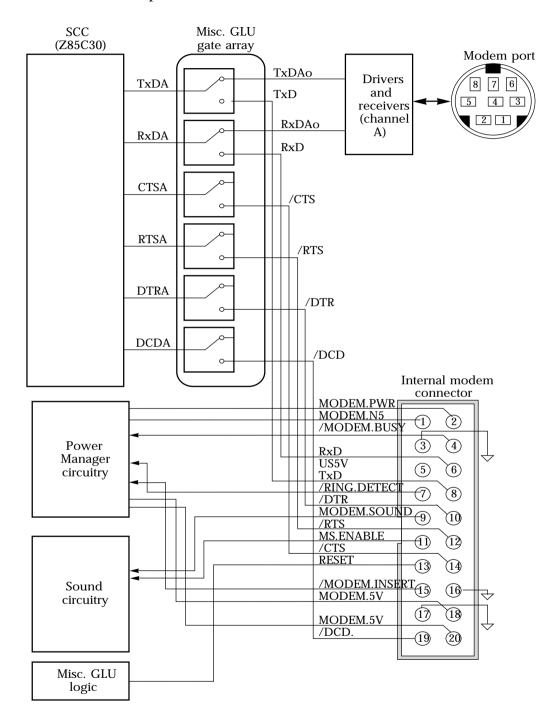
Modem card hardware interface

Figure 1-8 shows the hardware interface between a modem card installed in the modem connector and the computer. Notice that when a modem card is inserted in the modem connector, the card is automatically connected to channel A, the modem port. Although the computer hardware is designed to support operation of the internal modem through either of the two external RS-422 serial ports (modem or printer), the firmware supports operation only through the modem port.

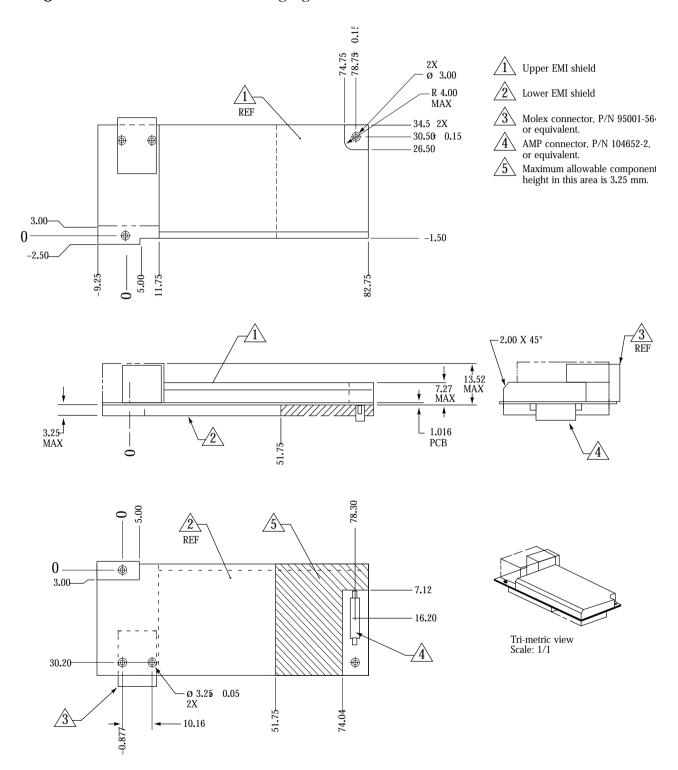
Physical design guide for a modem card

Figure 1-9 is a physical design guide giving you the mechanical specifications you will need, including card size and connector location, to design a compatible modem card for the Macintosh PowerBook 140 and Macintosh PowerBook 170 computers.

• **Figure 1-8** Interface between the modem card and the computer



• **Figure 1-9** Modem card design guide



Modem power-control interface

Two lines from the computer, US5V and MODEM.5V, provide +5 VDC power to the modem. US5V is always present unless there is a hardware shutdown (following a battery failure or if the computer's back-panel switch is turned off). MODEM.5V power is turned on or off depending on the current power mode of the modem and on how the serial port is used. For example, MODEM.5V is turned off when the computer enters the shutdown or sleep mode and when the serial driver is closed. The modem has two power modes: power on and standby.

Power on: This is the normal operating mode.

Standby: In this mode, MODEM.5V is switched off, all modem circuits are turned off, communication parameters are saved in EEPROM, and the only source of power is US5V. This mode has very low power consumption because only leakage current is drawn.

Two signal lines, MODEM.PWR and /MODEM.BUSY, control power to the modem connector from the Power Manager. /MODEM.BUSY is sent to the Power Manager to prevent the computer from removing power to the modem while the modem is using the communication channel to the computer. A modem card uses the /MODEM.BUSY signal to indicate to the computer that any of the following is true:

- The modem is executing its power-up sequence.
- The modem is off hook (for any reason).
- The modem is executing a command, where command execution begins with <CR> at the end of an AT command sequence or the repeat last command sequence ("a/" or "A/").
- ♦ *Note:* If the modem is executing any self-tests, it is considered to be executing a command and therefore busy.

The Power Manager controls the MODEM.PWR signal. If the Power Manager negates MODEM.PWR (signal goes low), it must wait at least 500 ms before turning off MODEM.5V. This gives the modem sufficient time to save the communication parameters in EEPROM before MODEM.5V is switched off. Three of the modem interface signals, /DTR, TxD, and /RTS, go to ground potential within 50 ns of the negation of MODEM.PWR.

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Usually, the Power Manager does not negate MODEM.PWR if the modem has /MODEM.BUSY asserted. There are times, however, when the Power Manager must turn the modem off even though it is busy—for example, when the battery reserve voltage becomes too low. If this occurs, the modem stops its busy activity (for example, goes on hook) and performs the necessary activities for switching to standby. The modem can do one of two things if it is executing a command when MODEM.PWR is negated: either finish executing the command or abort execution and restore the state prior to the command, whichever takes less time.

Modem operation

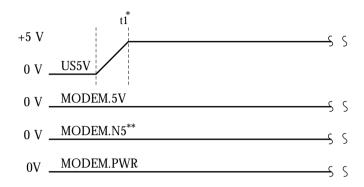
When MODEM.5V power is turned on, the modem leaves the standby mode and enters the power-on sequence. A positive RESET signal from the Power Manager resets the modem's microprocessor and begins the initialization sequence, which includes a memory check, the restoration of communications parameters, and the generation of a beep.

If the modem is in standby and it detects an incoming call (/RI.DETECT is asserted low), the computer acknowledges the call and powers up the modem to check whether the ring is valid. The Power Manager must power up the modem within 5 seconds after /RI.DETECT is asserted. This feature is enabled through the Portable CDev.

Power-up/power-down timing

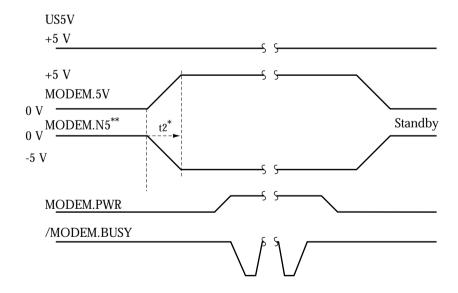
Timing diagrams for the modem's power-up and power-down sequences are shown in Figures 1-10 through 1-12.

• **Figure 1-10** Modem cold-start (initial power-up) timing diagram



^{*} t1 = 2 ms (typical), 30 ms (maximum). After t1, maximum overshoot is less than 50 mV peak to peak.

• Figure 1-11 Modem warm-start timing diagram

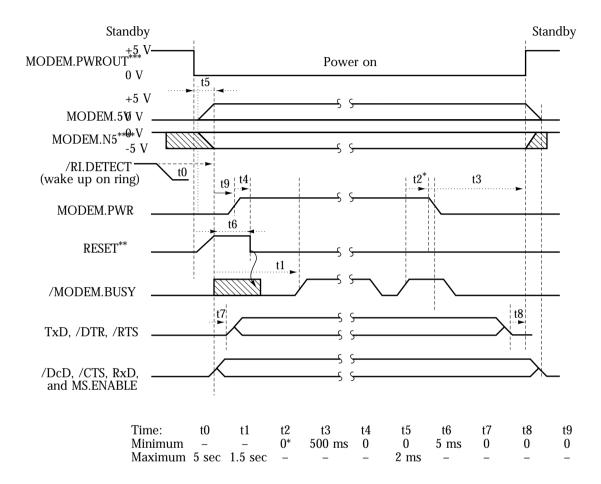


^{*} t2 = 35 ms (typical), 70 ms (maximum). After ?, maximum overshoot is less than 50 mV peak to peak.

^{**}MODEM.N5, although shown in this diagram, is not used by the Apple modem.

^{**} MODEM.N5, although shown in this diagram s not used by the Apple modem.

• **Figure 1-12** Complete power-up/power-down sequence timing diagram



^{*} t2 > 0 may not be obeyed by the CPU.

^{**} RESET may rise with MODEM.5V, but not before.

^{****} MODEM.PWROUT is an external CPU signal that turns MODEM.5V on and off. US5V is always on and is not shown on this diagram.

^{*****} MODEM.N5, although shown in this diagram, is not used by the Apple modem.

Ring detection

The ring detect interrupt signal (/RI.DETECT) is asserted during most of the AC cycle of a ring signal and is used to signal the computer that a ring is taking place. Both ringing and pulsing can trigger the ring detector. The microprocessor in your modem must be capable of distinguishing between ring and pulse dialing by detecting the frequency of the incoming signal. If the modem is turned off, the computer can determine whether the /RI.DETECT signal corresponds to a ring or a pulse by powering up the modem and reading the appropriate register or looking for the RING result code.

Modem card power requirements

A modem card must be able to operate on +5 VDC \pm 5 percent. This voltage is provided through the modem connector by either the battery or a combination of battery and charger. Typically, a fully operational modem card has an optimized power consumption of 450 mW.

Current drawn from the two +5 VDC sources by the modem should not exceed

- 95 mA typical when in full operation (on line)
- 70 mA typical when in command state
- 1 μA when in standby mode and there is no incoming ring signal

Telephone line electrical interface

Your modem card design should include a balanced, two-wire telephone interface that meets U.S. (FCC part 68), DOC, and JATE telephone line interface specifications. The physical interface consists of an RJ-11 phone jack with six slots and four contacts. The two middle contacts are used for the TIP and RING signals; all others are unused.

Modem specifications

The following compilations of signal characteristics are provided for reference only.

Compatibility and modulation

Standard	Full Dup Speed (bps)	olex Modulation	Baud	
CCITT V.22 CCITT V.22 CCITT V.21	1200	2400 DPSK FSK	QAM 600 300/110	600
Bell 212A Bell 103	1200 300/110	DPSK FSK	600 300/110	

Half Duplex			
Standard	Speed (bps)	- Modulation	
CCITT V.2	27ter	4800/2400	Half duplex
CCITT V.29 9600/7200		Half duplex	-

Transmit carrier frequencies

V.22 bis/V.22/2	12A		Transmit carrier	
Originate		1200 Hz		
Answer		2400 Hz		
Bell 103	Mark	Space		
Originate	1270	1070		
Answer	2225	2025		
V.21	Mark	Space		
Originate	980	1180		
Answer	1650	1850		
V.29				
Carrier V.27ter	1700 Hz			

Guard tone frequencies and transmit levels (CCITT only)

 $1800 \text{ Hz} \pm 20 \text{ Hz} @ 6 \pm 1 \text{ dB}$ below transmit carrier level $550 \text{ Hz} \pm 20 \text{ Hz} @ 3 \pm 1 \text{ dB}$ below transmit carrier level

Answer tone frequency

V.22 bis/V.22/V.21 2100 Hz

Bell 103/212A 2225 Hz

Received signal frequency tolerance

Offset frequency $\pm 7 \text{ Hz}$

Calling tone

V.25 13 Hz

Keyboard overview

This section describes the keyboard layouts and the Caps Lock modification.

Keyboard layouts

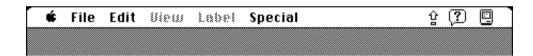
There are two versions of the keyboard, a U.S. (domestic) version with 63 keys and an ISO (international) version with 64 keys. Your application can use the Gestalt Manager to identify the keyboard by checking for a selector identification code of 12. The keyboard layouts are shown in Figure 1-13.

• **Figure 1-13** U.S. and ISO keyboard layouts

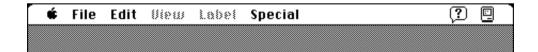
Caps Lock modification

TheCaps Lock key on the keyboard does not have a locking position to let a user know the current state of the key. To compensate for this, system software versions 7.0, and greater, include a Caps Lock INIT that installs a special system menu containing the international Caps Lock icon. Figure 1-14 shows the international Caps Lock icon that appears next to Balloon Help when the caps lock key is in the "down," or engaged, position. When you change the state of the Caps Lock key (Caps Lock "up"), the international Caps Lock icon disappears, as shown in Figure 1-15to let you know that the machine is no longer locked to all capital letters.

• **Figure 1-14** Caps Lock "down"



• **Figure 1-15** Caps Lock "up"



Clicking on the Caps Lock icon, clicking anywhere else in the menu bar, or tracking over the menu with the cursor will have no effect if the Caps Lock key is engaged (down); the icon will never be highlighted, nor will its menu be displayed.

Chapter 2 The Software

This chapter describes the new features of the ROM software in the Macintosh PowerBook 140 and the Macintosh PowerBook 170 computers and defines the system software.

The ROM

The ROM software is based on the universal overpatch ROM used in the Macintosh IIci, Macintosh IIfx, Macintosh IIsi, and Macintosh LC computers.

The size of the ROM has been increased to 1 MB. The first half of the ROM is an

overpatch of the ROM used in other members of the Macintosh II family. The second half of the ROM is new code and resources to support the Macintosh PowerBook 140, the

Macintosh PowerBook 170, and other new members of the Macintosh family.

The ROM incorporates several new features, including

- support for the Power Manager
- support for power cycling (a new method of power saving that replaces the "idle" mode on the Macintosh Portable)
- support for the modem card
- support for backlighting
- support for sound in/sound out

System software

At introduction, the Macintosh PowerBook 140 and the Macintosh PowerBook 170 computers will be supported by system version 7.0.1 software.

THE APPLE PUBLISHING SYSTEM

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Text type and display type are Apple's corporate font, a condensed version of ITC Garamond[®]. Bullets are ITC Zapf Dingbats[®].